FACT[™] Advanced CMOS Logic

Databook



MS WATS 1-800-633-2992 AL WATS 1-800-572-2907





A Corporate Dedication to Quality and Reliability

National Semiconductor is an industry leader in the manufacture of high quality, high reliability integrated circuits. We have been the leading proponent of driving down IC defects and extending product lifetimes. From raw material through product design, manufacturing and shipping, our quality and reliability is second to none.

We are proud of our success . . . it sets a standard for others to achieve. Yet, our quest for perfection is ongoing so that you, our customer, can continue to rely on National Semiconductor Corporation to produce high quality products for your design systems.

Charles E. Sporck

President, Chief Executive Officer National Semiconductor Corporation

Wir fühlen uns zu Qualität und Zuverlässigkeit verpflichtet

National Semiconductor Corporation ist führend bei der Herstellung von integrierten Schaltungen hoher Qualität und hoher Zuverlässigkeit. National Semiconductor war schon immer Vorreiter, wenn es galt, die Zahl von IC Ausfällen zu verringern und die Lebensdauern von Produkten zu verbessern. Vom Rohmaterial über Entwurf und Herstellung bis zur Auslieferung, die Qualität und die Zuverlässigkeit der Produkte von National Semiconductor sind unübertroffen.

Wir sind stolz auf unseren Erfolg, der Standards setzt, die für andere erstrebenswert sind. Auch ihre Ansprüche steigen ständig. Sie als unser Kunde können sich auch weiterhin auf National Semiconductor verlassen.

La Qualité et La Fiabilité:

Une Vocation Commune Chez National Semiconductor Corporation

National Semiconductor Corporation est un des leaders industriels qui fabrique des circuits intégrés d'une très grande qualité et d'une fiabilité exceptionelle. National a été le premier à vouloir faire chuter le nombre de circuits intégrés défectueux et a augmenter la durée de vie des produits. Depuis les matières premières, en passant par la conception du produit sa fabrication et son expédition, partout la qualité et la fiabilité chez National sont sans équivalents.

Nous sommes fiers de notre succès et le standard ainsi défini devrait devenir l'objectif à atteindre par les autres sociétés. Et nous continuons à vouloir faire progresser notre recherche de la perfection; il en résulte que vous, qui êtes notre client, pouvez toujours faire confiance à National Semiconductor Corporation, en produisant des systèmes d'une très grande qualité standard.

Un Impegno Societario di Qualità e Affidabilità

National Semiconductor Corporation è un'industria al vertice nella costruzione di circuiti integrati di altà qualità ed affidabilità. National è stata il principale promotore per l'abbattimento della difettosità dei circuiti integrati e per l'allungamento della vita dei prodotti. Dal materiale grezzo attraverso tutte le fasi di progettazione, costruzione e spedizione, la qualità e affidabilità National non è seconda a nessuno

Noi siamo orgogliosi del nostro successo che fissa per gli altri un traguardo da raggiungere. Il nostro desiderio di perfezione è d'altra parte illimitato e pertanto tu, nostro cliente, puoi continuare ad affidarti a National Semiconductor Corporation per la produzione dei tuoi sistemi con elevati livelli di qualità.

Charles E. Sporck

President, Chief Executive Officer National Semiconductor Corporation

FACTDATABOOK

1989 Edition

Descriptions and Family Characteristics
Ratings, Specifications and Waveforms
Design Considerations
Advanced CMOS Datasheets
Ordering Information/Physical Dimensions

TRADEMARKS

Following is the most current list of National Semiconductor Corporation's trademarks and registered trademarks.

SCXTM Abuseable™ FairtechTM **MSTTM** Naked-8TM Anadig™ FAST® SERIES/800TM ANS-R-TRANTM 5-Star Service™ National® Series 900TM **APPSTM** Series 3000TM GENIXTM National Semiconductor® **ASPECTTM** GNXTM National Semiconductor Series 32000® Auto-Chem Deflasher™ HAMRIM Corp.® Shelf ChekTM ВСРТМ HandiScan™ NAX 800TM SofChekTM BI-FETTM **HEX 3000TM** Nitride PlusTM SPIRETM BI-FET IITM **HPCTM** Nitride Plus Oxide™ **STARTM** 13L® **NMLTM** StarlinkTM **BI-LINETM** NOBUSTM STARPLEXTM. **BIPLANTM ICMTM** BLCTM INFOCHEXTM NSC800TM Super-Block™ BLXTM Integral ISETM **NSCISETM** SuperChipTM SuperScriptTM Brite-Lite™ IntelisplayTM NSX-16TM BTLTM ISETM NS-XC-16TM SYS32TM NTERCOMTM TapePak® ISE/06TM CheckTrack™ TDSTM СІМТМ ISE/08TM **NURAMTM CIMBUSTM** ISE/16TM OXISSTM TeleGate™ P2CMOSTM The National Anthem® **CLASICTM** ISE32TM Clock ChekTM **ISOPLANARTM** PC Master™ Timer Chek™ СОМВОТМ ISOPLANAR-ZTM Perfect Watch™ TINATM TLCTM COMBO ITM KeyScanTM Pharma ChekTM COMBO IITM **LMCMOSTM PLANTM** TrapezoidalTM COPS™ microcontrollers M2CMOSTM **PLANARTM** TRI-CODETM TRI-POLYTM Datachecker® MacrobusTM Plus-2TM DENSPAKTM Polycraft™ TRI-SAFETM MacrocomponentTM DIBTM MAXI-ROM® POSilinkTM TRI-STATE® Digitalker® Meat/ChekTM POSitalkerTM TURBOTRANSCEIVER™ VIPTM DISCERNTM MenuMasterTM Power + ControlTM DISTILLIM Microbus™ data bus POWERplanarTM VR32TM QUAD3000TM **WATCHDOG™ DNR®** MICRO-DACTM **DPVMTM** μtalker™ QUIKLOOKTM **XMOSTM ELSTARTM** MicrotalkerTM RATTM **XPUTM** E-Z-LINKTM MICROWIRETM . RTX16™ Z STARTM SABRTM **FACTTM** MICROWIRE/PLUSTM 883B/RETSTM FAIRCADTM MOLETM Script ChekTM 883S/RETSTM

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

- 1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
- A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation 2900 Semiconductor Drive, P.O. Box 58090, Santa Clara, California 95052-8090 (408) 721-5000 TWX (910) 339-9240

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied, and National reserves the right, at any time without notice, to change said circuitry or specifications.



Introduction

FACTTM (Fairchild Advanced CMOS Technology) is a very high-speed, low power CMOS Logic family utilizing a 1.3 μM Isoplanar silicon gate CMOS process. FACT logic functions can attain speeds similar to that of Advanced Low Power Schottky while retaining the advantages of CMOS logic: Ultra low static power and high noise immunity. FACT offers the system designer the added benefit of superior line driving characteristics and excellent ESD and Latch-up immunity.

The FACT family consists of devices in two categories:

- AC—standard logic functions with CMOS compatible inputs and TTL and MOS compatible outputs;
- ACT—standard logic functions with TTL compatible inputs and TTL and MOS compatible outputs.

Product Index and Selection Guide

Lists 54AC/74AC and 54ACT/74ACT circuits currently available, in design or planned. The selection guide groups the circuits by function.

Packaging Outlines and Ordering Information

products.

Section 5



Product Status Definitions

Definition of Terms

| Data Sheet Identification | Product Status | Definition | | |
|-------------------------------|---------------------------|--|--|--|
| Advance Information | Formative or In Design | This data sheet contains the design specifications for product development. Specifications may change in any manner without notice. | | |
| Preliminary | First Production | This data sheet contains preliminary data, and supplementary data will be published at a later date. National Semiconductor Corporation reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. | | |
| No Identification Noted | Full Production | This data sheet contains final specifications. National Semiconductor Corporation reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. | | |

National Semiconductor Corporation reserves the right to make changes without further notice to any products herein to improve reliability, function or design. National does not assume any liability arising out of the application or use of any product or circuit described herein; neither does it convey any license under its patent rights, nor the rights of others.

Alpha-Numeric Index some xsbnl pinsmuM-eriqlA

| 54AC/74AC00 Quad 2-Input NAND Gate |
|---|
| 54AC/74AC02 Quad 2-Input NOR Gate |
| 54AC/74AC04 Hex Inverter |
| 54AC/74AC08 Quad 2-Input AND Gate4-15 |
| 54AC/74AC10 Triple 3-Input NAND Gate4-18 |
| 54AC/74AC11 Triple 3-Input AND Gate4-21 |
| 54AC/74AC14 Hex Inverter with Schmitt Trigger Input4-24 |
| 54AC/74AC20 Dual 4-Input NAND Gate |
| 54AC/74AC32 Quad 2-Input OR Gate |
| 54AC/74AC74 Dual D Positive Edge-Triggered Flip-Flop |
| 54AC/74AC85 4-Bit Magnitude Comparator |
| 54AC/74AC86 Quad 2-Input Exclusive-OR Gate4-40 |
| 54AC/74AC109 Dual JK Positive Edge-Triggered Flip-Flop |
| 54AC/74AC112 Dual JK Negative Edge-Triggered Flip-Flop |
| 54AC/74AC138 1-of-8 Decoder/Demultiplexer |
| 54AC/74AC139 Dual 1-of-4 Decoder/Demultiplexer |
| 54AC/74AC151 8-Input Multiplexer |
| 54AC/74AC153 Dual 4-Input Multiplexer |
| 54AC/74AC157 Quad 2-Input Multiplexer4-73 |
| 54AC/74AC158 Quad 2-Input Multiplexer4-78 |
| 54AC/74AC161 Synchronous Presettable Binary Counter |
| 54AC/74AC163 Synchronous Presettable Binary Counter4-91 |
| 54AC/74AC164 Serial-In, Parallel-Out Shift Register |
| 54AC/74AC169 4-Stage Synchronous Bidirectional Counter |
| 54AC/74AC174 Hex D Flip-Flop with Master Reset |
| 54AC/74AC175 Quad D Flip-Flop |
| 54AC/74AC191 Up/Down Counter with Preset and Ripple Clock |
| 54AC/74AC240 Octal Buffer/Line Driver with TRI-STATE Outputs |
| 54AC/74AC241 Octal Buffer/Line Driver with TRI-STATE Outputs |
| 54AC/74AC244 Octal Buffer/Line Driver with TRI-STATE Outputs |
| 54AC/74AC245 Octal Bidirectional Transceiver with TRI-STATE Inputs/Outputs |
| 54AC/74AC251 8-Input Multiplexer with TRI-STATE Output |
| 54AC/74AC253 Dual 4-Input Multiplexer with TRI-STATE Outputs |
| 54AC/74AC257 Quad 2-Input Multiplexer with TRI-STATE Outputs |
| 54AC/74AC258 Quad 2-Input Multiplexer with TRI-STATE Outputs |
| 54AC/74AC269 8-Bit Bidirectional Binary Counter4-164 |
| 54AC/74AC273 Octal D Flip-Flop4-165 |
| 54AC/74AC280 9-Bit Parity Generator/Checker4-170 |
| 54AC/74AC283 4-Bit Binary Full Adder with Fast Carry 4-174 |
| 54AC/74AC299 8-Input Universal Shift/Storage Register with Common Parallel I/O Pins 4-175 |
| 54AC/74AC350 4-Bit Shifter with TRI-STATE Outputs4-187 |
| 54AC/74AC373 Octal Transparent Latch with TRI-STATE Outputs |
| 54AC/74AC374 Octal D Flip-Flop with TRI-STATE Outputs |
| 54AC/74AC377 Octal D Flip-Flop with Clock Enable |
| 54AC/74AC520 8-Bit Identity Comparator |
| 54AC/74AC521 8-Bit Identity Comparator |
| 54AC/74AC540 Octal Buffer/Line Driver with TRI-STATE Outputs |
| 54AC/74AC541 Octal Buffer/Line Driver with TRI-STATE Outputs |
| 54AC/74AC574 Octal D Flip-Flop with TRI-STATE Outputs |
| 54AC/74AC646 Octal Transceiver/Register with TRI-STATE Outputs |
| 54AC/74AC648 Octal Transceiver/Register with TRI-STATE Outputs |

Alpha-Numeric Index (Continued)

| 54AC/74AC821 10-Bit D Flip-Flop with TRI-STATE Outputs | |
|---|-----|
| 54AC/74AC823 9-Bit D Flip-Flop | 85 |
| 54AC/74AC825 8-Bit D Flip-Flop | 89 |
| 54AC/74AC843 9-Bit Transparent Latch 4-29 | |
| 54AC/74AC845 8-Bit Transparent Latch with TRI-STATE Outputs | 07 |
| 54AC/74AC2708 64 x 9 First-In, First-Out Memory | |
| 54AC/74AC4024 7-Stage Binary Ripple Counter | 40 |
| 54ACT/74ACT00 Quad 2-Input NAND Gate | 1-5 |
| 54ACT/74ACT04 Hex Inverter | 12 |
| 54ACT/74ACT08 Quad 2-Input AND Gate | |
| 54ACT/74ACT14 Hex Inverter with Schmitt Trigger Input | 24 |
| 54ACT/74ACT32 Quad 2-Input OR Gate | 30 |
| 54ACT/74ACT74 Dual D Positive Edge-Triggered Flip-Flop | 33 |
| 54ACT/74ACT85 4-Bit Magnitude Comparator | |
| 54ACT/74ACT109 Dual JK Positive Edge-Triggered Flip-Flop | |
| 54ACT/74ACT112 Dual JK Negative Edge-Triggered Flip-Flop | 49 |
| 54ACT/74ACT138 1-of-8 Decoder/Demultiplexer | 50 |
| 54ACT/74ACT139 Dual 1-of-4 Decoder/Demultiplexer | 57 |
| 54ACT/74ACT151 8-Input Multiplexer | |
| 54ACT/74ACT153 Dual 4-Input Multiplexer | |
| 54ACT/74ACT157 Quad 2-Input Multiplexer | |
| 54ACT/74ACT158 Quad 2-Input Multiplexer | |
| 54ACT/74ACT136 Quad 2-input Multiplexer 4- | |
| 54ACT/74ACT161 Synchronous Presettable Binary Counter | |
| 54ACT/74ACT163 Synchronous Presentable Binary Counter 54ACT/74ACT164 Serial-In, Parallel-Out Shift Register | |
| 54ACT/74ACT174 Hex D Flip-Flop with Master Reset | |
| 54ACT/74ACT174 Hex D Flip-Flop with waster Heset. 4-10 | |
| 54ACT/74ACT173 Quad D Filip-Filop 4-1 | 17 |
| 54ACT/74ACT181 4-Bit Antiffield Logic Offic 4-1 54ACT/74ACT182 Carry Look-Ahead Generator 4-1 | 10 |
| 54ACT/74ACT162 Carry Look-Arlead Generator 4-1 54ACT/74ACT240 Octal Buffer/Line Driver with TRI-STATE Outputs | |
| | |
| 54ACT/74ACT241 Octal Buffer/Line Driver with TRI-STATE Outputs | |
| 54ACT/74ACT244 Octal Buffer/Line Driver with TRI-STATE Outputs | |
| 54ACT/74ACT245 Octal Bidirectional Transceiver with TRI-STATE Inputs/Outputs | |
| 54ACT/74ACT251 8-Input Multiplexer with TRI-STATE Output | 42 |
| 54ACT/74ACT253 Dual 4-Input Multiplexer with TRI-STATE Outputs | |
| 54ACT/74ACT257 Quad 2-Input Multiplexer with TRI-STATE Outputs | |
| 54ACT/74ACT258 Quad 2-Input Multiplexer with TRI-STATE Outputs | 59 |
| 54ACT/74ACT273 Octal D Flip-Flop | 65 |
| 54ACT/74ACT280 9-Bit Parity Generator/Checker | |
| 54ACT/74ACT283 4-Bit Binary Full Adder with Fast Carry | |
| 54ACT/74ACT299 8-Input Universal Shift/Storage Register with Common Parallel I/O Pins 4-1 | |
| 54ACT/74ACT323 8-Bit Universal Shift/Storage Register with Synchronous Reset and Common I/O Pins | 82 |
| 54ACT/74ACT350 4-Bit Shifter with TRI-STATE Outputs | |
| 54ACT/74ACT373 Octal Transparent Latch with TRI-STATE Outputs | |
| 54ACT/74ACT374 Octal D Flip-Flop with TRI-STATE Outputs | |
| 54ACT/74ACT377 Octal D Flip-Flop with Clock Enable | |
| 54ACT/74ACT381 4-Bit Arithmetic Logic Unit | |
| 54ACT/74ACT399 Quad 2-Port Register | |
| 54ACT/74ACT520 8-Bit Identity Comparator | |
| 54ACT/74ACT521 8-Bit Identity Comparator | |
| 04/01/74/01021 0-Dit Idollity Colliparatol | 17 |

Alpha-Numeric Index (Continued)

| 54ACT/74ACT534 Octal D Flip-Flop with TRI-STATE Outputs4 | 1-223 |
|--|-------|
| 54ACT/74ACT540 Octal Buffer/Line Driver with TRI-STATE Outputs | 1-228 |
| 54ACT/74ACT541 Octal Buffer/Line Driver with TRI-STATE Outputs | 1-231 |
| 54ACT/74ACT543 Octal Registered Transceiver | 1-234 |
| 54ACT/74ACT544 Octal Registered Transceiver | 1-235 |
| 54ACT/74ACT563 Octal Latch with TRI-STATE Outputs | 1-236 |
| 54ACT/74ACT564 Octal D Flip-Flop with TRI-STATE Outputs | 1-241 |
| 54ACT/74ACT573 Octal Latch with TRI-STATE Outputs | 1-244 |
| 54ACT/74ACT574 Octal D Flip-Flop with TRI-STATE Outputs | 1-249 |
| 54ACT/74ACT646 Octal Transceiver/Register with TRI-STATE Outputs | 1-255 |
| 54ACT/74ACT657 Octal Bidirectional Transceiver with 8-Bit Parity Generator/Checker and | |
| TRI-STATE Outputs | 1-269 |
| 54ACT/74ACT705 Arithmetic Logic Unit for Digital Signal Processing Applications | 4-270 |
| 54ACT/74ACT715 Programmable Video Sync Generator | 1-271 |
| 54ACT/74ACT725 512 x 9 First In, First Out Memory (FIFO) | 1-272 |
| 54ACT/74ACT818 8-Bit Diagnostic Register | 1-273 |
| 54ACT/74ACT821 10-Bit D Flip-Flop with TRI-STATE Outputs | |
| 54ACT/74ACT823 9-Bit D Flip-Flop | 1-285 |
| 54ACT/74ACT825 8-Bit D Flip-Flop | 1-289 |
| 54ACT/74ACT827 10-Bit Buffer/Line Driver with TRI-STATE Outputs | 1-293 |
| 54ACT/74ACT841 10-Bit Transparent Latch with TRI-STATE Outputs | 4-294 |
| 54ACT/74ACT843 9-Bit Transparent Latch | 1-299 |
| 54ACT/74ACT845 8-Bit Transparent Latch with TRI-STATE Outputs | |
| 54ACT/74ACT1016 16 x 16 Parallel Multiplier | 1-312 |
| 54ACT/74ACT1110 Single Port 16 x 16 Bit Multiplier/Accumulator | 1-322 |
| 54ACT/74ACT2708 64 x 9 First-In, First-Out Memory | 1-324 |
| | |



FACT™ Selection Guide

Gates

| SANP. | Function | Device |
|-------|------------------------------|--|
| | NAND | Vianuliari, iskisosimi importeo i vasti i vais |
| | Quad 2-Input | 54AC/74AC00 |
| | Quad 2-Input | 54ACT/74ACT00 |
| | Triple 3-Input | 54AC/74AC10 |
| | Triple 3-Input | 54ACT/74ACT10 |
| | Dual 4-Input | 54AC/74AC20 |
| | AND | |
| | Quad 2-Input | 54AC/74AC08 |
| | Quad 2-Input | 54ACT/74ACT08 |
| | Triple 3-Input | 54AC/74AC11 |
| | OR/NOR/Exclusive-OR | Min value of the North of ASLAT TO 27 TAILTNAN |
| | Quad 2-Input OR | 54AC/74AC32 |
| | Quad 2-Input OR | 54ACT/74ACT32 |
| | Quad 2-Input NOR | 54AC/74AC02 |
| | Quad 2-Input Exclusive-OR | 54AC/74AC86 |
| | Quad 2-Input Exclusive-OR | 54ACT/74ACT86 |
| | Inverter | |
| | Hex Inverter | 54AC/74AC04 |
| | Hex Inverter | 54ACT/74ACT04 |
| | Hex Schmitt Trigger Inverter | 54AC/74AC14 |
| | Hex Schmitt Trigger Inverter | 54ACT/74ACT14 |

Registers

| Function | Device | Clock Inputs |
|----------------------------------|----------------|-----------------|
| Quad 2-Port Register | 54ACT/74ACT399 | 1(|
| Diagnostic and Pipeline Register | 54ACT/74ACT818 | 2 |

Parity Generator/Checkers

| Function | Device |
|--------------------------|----------------|
| Parity Generator/Checker | 54AC/74AC280 |
| Parity Generator/Checker | 54ACT/74ACT280 |
| Video Sync Generator | 54ACT/74ACT715 |

Flip-Flops

| Function | Device | TRI-STATE® Outputs | Master Reset |
|----------|----------------|--------------------|-----------------|
| Dual D | 54AC/74AC74 | No | Yes |
| Dual D | 54ACT/74ACT74 | No | Yes |
| Dual JK | 54AC/74AC109 | No | Yes |
| Dual JK | 54ACT/74ACT109 | No | Yes |
| Dual JK | 54AC/74AC112 | No | No |
| Dual JK | 54ACT/74ACT112 | No | No |
| Quad D | 54AC/74AC175 | No | Yes |
| Quad D | 54ACT/74ACT175 | No | Yes |
| Hex D | 54AC/74AC174 | No | Yes |
| Hex D | 54ACT/74ACT174 | No | Yes |
| Octal D | 54AC/74AC273 | No | Yes |
| Octal D | 54ACT/74ACT273 | No | Yes |
| Octal D | 54AC/74AC374 | Yes | No So |
| Octal D | 54ACT/74ACT374 | Yes | No Solo |
| Octal D | 54AC/74AC377 | No | No |
| Octal D | 54ACT/74ACT377 | No | No |
| Octal D | 54ACT/74ACT534 | Yes | No |
| Octal D | 54ACT/74ACT564 | Yes | No |
| Octal D | 54AC/74AC574 | Yes | No |
| Octal D | 54ACT/74ACT574 | Yes | No |
| Octal D | 54ACT/74ACT825 | Yes | Yes |
| 9-Bit D | 54ACT/74ACT823 | Yes | Yes |
| 10-Bit D | 54ACT/74ACT821 | Yes | Yes |

ALUs

| Function | Device Device | No. of Bits | Arithmetic Functions | Logic Functions |
|---|----------------------------------|----------------|----------------------|--------------------|
| Arithmetic Logic Unit Arithmetic Logic Unit | 54ACT/74ACT181 54ACT/74ACT381 | 4 | 16 3 | 16 |

Latches

| Function WO | Device | TRI-STATE Outputs | Broadside Pinout |
|--------------------|----------------|----------------------|---------------------|
| Octal | 54AC/74AC373 | Yes | No |
| Octal | 54ACT/74ACT373 | Yes | No |
| Octal D | 54ACT/74ACT563 | Yes | Yes |
| Octal D | 54AC/74AC573 | Yes | Yes |
| Octal D | 54ACT/74ACT573 | Yes | Yes |
| Octal Transparent | 54AC/74AC845 | Yes | Yes |
| Octal Transparent | 54ACT/74ACT845 | Yes | Yes |
| 9-Bit Transparent | 54AC/74AC843 | Yes | Yes |
| 9-Bit Transparent | 54ACT/74ACT843 | Yes | Yes |
| 10-Bit Transparent | 54AC/74AC841 | Yes | Yes |
| 10-Bit Transparent | 54ACT/74ACT841 | Yes | Yes |

Counters

| Function | Device | Parallel Entry | Reset | U/D | TRI-STATE Outputs |
|-----------------------|----------------|----------------|-------|-----|----------------------|
| 4-Bit Binary | 54AC/74AC161 | S | Α | No | No |
| 4-Bit Binary | 54ACT/74ACT161 | S | A | No | No |
| 4-Bit Binary | 54AC/74AC163 | S | S | No | No |
| 4-Bit Binary | 54ACT/74ACT163 | S | S | No | No |
| 4-Bit Binary | 54AC/74AC169 | S | _ | Yes | No |
| 4-Bit Binary | 54AC/74AC191 | A | _ | Yes | No |
| 8-Bit Binary | 54ACT/74ACT269 | S | _ | Yes | No |
| 7-Stage Binary Ripple | 54AC/74AC4024 | _ | A | No | No |

S = Synchronous A = Asynchronous

ALU Support

| Function | Device | No. of Bits |
|-----------------|----------------|-------------|
| Carry Lookahead | 54ACT/74ACT182 | 4 |

Buffers/Line Drivers

| Function | Device OM | Enable Inputs (Level) | Inverting/ Non-Inverting | Broadside Pinout |
|----------|----------------|-----------------------------|--|---------------------|
| Octal | 54AC/74AC240 | 2(L) | CARTITOARE I | No |
| Octal | 54ACT/74ACT240 | 2(L) | THE CONTROL OF THE CO | No |
| Octal | 54AC/74AC241 | 1(H) & 1(L) | N N | No |
| Octal | 54ACT/74ACT241 | 1(H) & 1(L) | AASSTOAAE N | No |
| Octal | 54AC/74AC244 | 2(L) | N SAAGYZAAGST | No |
| Octal | 54ACT/74ACT244 | 2(L) | N SEACHTEAN | No |
| Octal | 54AC/74AC540 | 2(L) | 54AQ/76AC81 | Yes |
| Octal | 54ACT/74ACT540 | 2(L) | SAAGTYTAA | Yes |
| Octal | 54AC/74AC541 | 1(H) & 1(L) | N N | Yes |
| Octal | 54ACT/74ACT541 | 1(H) & 1(L) | N N | Yes |
| 10-Bit | 54ACT/74ACT827 | 2(L) | N | Yes |

L = LOW H = HIGH

FIFOs

| Function | Device | Input | Output | TRI-STATE Outputs |
|------------------------------------|-----------------------------------|----------------------|-------------------|-------------------|
| 64 x 9 FIFO Memory | 54AC/74AC2708 | Parallel | Parallel | Yes |
| 64 x 9 FIFO Memory 512 x 9 FIFO | 54ACT/74ACT2708 54ACT/74ACT725 | Parallel Parallel | Parallel Parallel | Yes Yes |

Decoders/Demultiplexers

| Function | Device Device | LOW Enable | Active- HIGH Enable | Active- LOW Outputs | Active- Address Inputs |
|-------------|----------------|---------------|---------------------------|---------------------------|------------------------------|
| 1-of-8 | 54AC/74AC138 | 2 | productive DMAC | 8 | 3 |
| 1-of-8 | 54ACT/74ACT138 | 2 | Canal Dasa | 8 | 3 |
| Dual 1-of-4 | 54AC/74AC139 | 1 & 1 | No No | 4 & 4 | 2 & 2 |
| Dual 1-of-4 | 54ACT/74ACT139 | 1 & 1 | No No | 4 & 4 | 2&2 |

Arithmetic Functions

| Function | Device | Features |
|-------------------------------|-----------------|--|
| 16 x 16 Multiplier | 54ACT/74ACT1016 | 2s Complement & Unsigned Arithmetic |
| Arithmetic Logic Unit for DSP | 54ACT/74ACT705 | 16-Bit ALU and 8 x 8 Parallel Multiplier/Accumulator |
| 16-Bit Single Port Multiplier | 54ACT/74ACT1110 | Pipeline Capability |

Shift Registers

| STAT Function elds | Device | No. of Bits | Reset | Serial Inputs | TRI-STATE Outputs |
|-------------------------|----------------|----------------|--------|-------------------|-------------------|
| Octal Shift/Storage | 54AC/74AC299 | 8 | A | 2 | Yes |
| Octal Shift/Storage | 54ACT/74ACT299 | 8:5044 | A | 2 2 2 3 1 3 1 | Yes Yes |
| Octal Shift/Storage | 54AC/74AC323 | 8 | TOAMS | 2 2 2 | Yes |
| Octal Shift/Storage | 54ACT/74ACT323 | 8 | NOAMS | 2 8 9 | Yes O |
| Serial In, Parallel-Out | 54AC/74AC164 | 8 8 AA | TOARCA | etallo 2 sove | No |
| Serial In, Parallel-Out | 54ACT/74ACT164 | 8 80A | ASAACA | netalo 2 l anavis | censul a No soc |

A = Asynchronous S = Synchronous

Multiplexers

| Function | Device | Enable Inputs (Level) | True Output | Complement Output |
|-----------------|----------------|-----------------------------|----------------|----------------------|
| 8-Input | 54AC/74AC151 | 1(L) | Yes | Yes |
| 8-Input | 54ACT/74ACT151 | 1(L) | Yes | Yes |
| 8-Input | 54AC/74AC251 | 1(L) | Yes | Yes |
| 8-Input | 54ACT/74ACT251 | 1(L) | Yes | Yes |
| Dual 4-Input | 54AC/74AC153 | 2(L) | Yes | No |
| Dual 4-Input | 54ACT/74ACT153 | 2(L) | Yes | No |
| Dual 4-Input | 54AC/74AC253 | 2(L) | Yes | No |
| Dual 4-Input | 54ACT/74ACT253 | 2(L) | Yes | No |
| Quad 2-Input | 54AC/74AC157 | 1(L) | Yes | No |
| Quad 2-Input | 54ACT/74ACT157 | 1(L) | Yes | No |
| Quad 2-Input | 54AC/74AC158 | 1(L) | No | Yes |
| Quad 2-Input | 54ACT/74ACT158 | 1(L) | No | Yes |
| Quad 2-Input | 54AC/74AC257 | 1(L) | Yes | No |
| Quad 2-Input | 54ACT/74ACT257 | 1(L) | Yes | No |
| Quad 2-Input | 54AC/74AC258 | 1(L) | No | Yes |
| Quad 2-Input | 54ACT/74ACT258 | 1(L) | No | Yes |
| 4 Input w/Shift | 54AC/74AC350 | 1(L) | Yes | No |
| 4 Input w/Shift | 54ACT/74ACT350 | 1(L) | Yes | No |

Comparators

| Function | Device | Features |
|----------------------------|----------------|------------|
| Octal Identity Comparator | 54AC/74AC520 | Expandable |
| Octal Identity Comparator | 54ACT/74ACT520 | Expandable |
| Octal Identity Comparator | 54AC/74AC521 | Expandable |
| Octal Identity Comparator | 54ACT/74ACT521 | Expandable |
| 4-Bit Magnitude Comparator | 54AC/74AC85 | |
| 4-Bit Magnitude Comparator | 54ACT/74ACT85 | |

Adders

| Function | Device | No. of Bits | Carry Lookahead |
|-------------------|----------------|----------------|--------------------|
| Binary Full Adder | 54AC/74AC283 | 4 | Yes |
| Binary Full Adder | 54ACT/74ACT283 | 4 | Yes |

Transceivers/Registered Transceivers

| Function | Device | Registered | Enable Inputs (Level) | TRI-STATE Output |
|------------------------------------|----------------|------------|-----------------------------|---------------------|
| Octal Bidirectional Transceiver | 54AC/74AC245 | No | 1(L) | Yes |
| Octal Bidirectional Transceiver | 54ACT/74ACT245 | No | 1(L) | Yes |
| Octal Bus Transceiver & Register | 54AC/74AC646 | Yes | 1(L) & 1(H) | Yes |
| Octal Bus Transceiver and Register | 54ACT/74ACT646 | Yes | I(L) & I(H) | Yes |
| Octal Bus Transceiver & Register | 54AC/74AC648 | Yes | 1(L) & 1(H) | Yes |
| Octal Register Transceiver | 54ACT/74ACT543 | Yes | 2(L) | Yes |
| Octal Register Transceiver | 54ACT/74ACT544 | Yes | 2(L) | Yes |
| Octal Bus Transceiver | 54ACT/74ACT657 | | 1(L) & 1(H) | Laure Carlotte |



Section 1

Descriptions and

Family Characteristics



Section 1 Contents

| Introduction | 1-3 |
|---|------|
| Low Power CMOS Operation | 1-3 |
| AC Performance | 1-4 |
| Multiple Output Switching | 1-4 |
| Noise Immunity | 1-4 |
| Output Characteristics | 1-4 |
| Dynamic Output Drive | 1-4 |
| Choice of Voltage Specifications | 1-6 |
| Power Dissipation | 1-8 |
| Specification Derivation | 1-10 |
| Capacitive Loading Effects | 1-11 |
| Latch-Up Immunity | 1-13 |
| Electrostatic Discharge (ESD) Sensitivity | 1-14 |
| Radiation Tolerance | 1-15 |

FACT™ Descriptions and Family Characteristics

National Semiconductor Advanced CMOS Technology—FACT™— Logic

Fairchild Semiconductor introduced FACT (Fairchild Advanced CMOS Technology) logic, a family of high speed advanced CMOS circuits, in 1985.

FACT logic offers a unique combination of high speed, low power dissipation, high noise immunity, wide fanout capability, extended power supply range and high reliability.

This data book describes the product line with device specifications as well as material discussing design considerations and comparing the FACT family to predecessor technologies.

The 1.3-micron silicon gate CMOS process utilized in this family has been proven in the field of high performance gate arrays, CMOS ASIC, and FACT. It has been further enhanced to meet and exceed the JEDEC standards for 74ACXX logic.

For direct replacement of LS, ALS and other TTL devices, the 'ACT circuits with TTL-type input thresholds are included in the FACT family. These include the more popular bus drivers/transceivers as well as many other 54ACTXXX/74ACTXXX devices.

Characteristics

- Full Logic Product Line
- Industry Standard Functions and Pinouts for SSI, MSI and LSI
- Meets or Exceeds JEDEC Standards for 74ACXX Family
- TTL Inputs on Selected Circuits
- High Performance Outputs
 - Common Output Structure for Standard and Buffer Drivers
 - Output Sink/Source Current of 24 mA
 - Transmission Line Driving 50Ω (Commercial)/ 75Ω (Military) Guaranteed
- Operation from 2V-6V Guaranteed
- Temperature Range
 - Commercial

-40°C to +85°C

Military

-55°C to +125°C

- Improved ESD Protection Network
- High Current Latch-Up Immunity

Interfacing

FACT devices have a wide operating voltage range ($V_{CC} = 2 V_{DC}$ to 6 V_{DC}) and sufficient current drive to interface with most other logic families available today.

Device designators are as follows:

- 'AC— This is a high speed CMOS device with CMOS input switching levels and buffered CMOS outputs that can drive ± 24 mA of I_{OH} and I_{OL} current. Industry standard 'AC nomenclature and pinouts are used.
- 'ACT— This is a high speed CMOS device with a TTL-to-CMOS input buffer stage. These device inputs are designed to interface with TTL outputs operating with a V_{CC} = 5V ±0.5V with V_{OH} = 2.4V and V_{OL} = 0.4V, but are functional over the entire FACT operating voltage range of 2.0 V_{DC} to 5.5 V_{DC}. These devices have buffered outputs that will drive CMOS or TTL devices with no additional interface circuitry. 'ACT devices have the same output structures as 'AC devices.

Low Power CMOS Operation

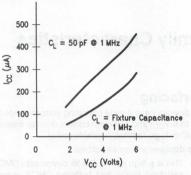
If there is one single characteristic that justifies the existence of CMOS, it is low power dissipation. In the quiescent state, FACT draws 1000 times less power than the equivalent LS or ALS TTL device. This enhances system reliability; because costly regulated high current power supplies, heat sinks and fans are eliminated, FACT logic devices are ideal for portable systems such as laptop computers and backpack communications systems. Operating power is also very low for FACT logic. Power consumption of various technologies with a clock frequency of 1 MHz is shown below.

FACT = 0.1 mW/Gate ALS = 1.2 mW/Gate LS = 2.0 mW/Gate

HC = 0.1 mW/Gate

П

Low Power CMOS Operation (Continued)



TL/F/10158-1

FIGURE 1-1. ICC VS VCC

Figure 1-1 illustrates the effects of I_{CC} versus power supply voltage (V_{CC}) for two load capacitance values: 50 pF and stray capacitance. The clock frequency was 1 MHz for the measurements.

AC Performance

In comparison to LS, ALS and HC families, FACT devices have faster internal gate delays as well as the basic gate delays. Additionally, as the level of integration increases, FACT logic leads the way to very high-speed systems.

The example below describes typical values for a 74XX138, 3-to-8 line decoder.

FACT = 6.0 ns @ C_L = 50 pF ALS = 12.0 ns @ C_L = 50 pF LS = 22.0 ns @ C_L = 15 pF HC = 17.5 ns @ C_L = 50 pF

AC performance specifications are guaranteed at 5.0V ± 0.5 V and 3.3V ± 0.3 V. For worst case design at 2.0V V_{CC} on all device types, the formula below can be used to determine AC performance.

AC performance at 2.0V $\rm V_{CC} = 1.9 \times AC$ specification at 3.3V.

Multiple Output Switching

Propagation delay is affected by the number of outputs switching simultaneously. Typically, devices with more than one output will follow the rule: for each output switching, derate the databook specification by 250 ps. This effect typically is not significant on an octal device unless more than four outputs are switching simultaneously. This derating is valid for the entire temperature range and 5.0V $\pm\,10\%$ VCC.

Noise Immunity

The noise immunity of a logic family is also an important equipment cost factor in terms of decoupling components, power supply dynamic resistance and regulation as well as layout rules for PC boards and signal cables.

The comparisons shown describe the difference between the input threshold of a device and the output voltage, $|V_{IL}-V_{OL}|/|V_{IH}-V_{OH}|$ at 4.5V V_{CC}.

FACT = 1.25V/1.25V ALS = 0.4V/0.7V LS = 0.3V/0.7V @ 4.75V V_{CC} HC = 0.8V/1.25V

Output Characteristics

All FACT outputs are buffered to ensure consistent output voltage and current specifications across the family. Both 'AC and 'ACT device types have the same output structures. Two clamp diodes are internally connected to the output pin to suppress voltage overshoot and undershoot in noisy system applications which can result from impedance mismatching. The balanced output design allows for controlled edge rates and equal rise and fall times.

All SSI and MSI devices ('AC or 'ACT) are guaranteed to source and sink 24 mA. Commercial devices, 74AC/ACTXXX, are capable of driving 50Ω transmission lines, while military grade devices, 54AC/ACTXXX, can drive 75Ω transmission lines.

I_{OL}/I_{OH} Characteristics

FACT = 24 mA/-24 mA ALS = 24 mA/-15 mA LS = 8 mA/-0.4 mA @ 4.75V V_{CC} HC = 4 mA/-4 mA

Dynamic Output Drive

Traditionally, in order to predict what incident wave voltages would occur in a system, the designer was required to do an output analysis using a Bergeron diagram. Not only is this a long and time consuming operation, but the designer needed to depend upon the accuracy and reliability of the manufacturer-supplied "typical" output I/V curve. Additionally, there was no way to guarantee that any supplied device would meet these "typical" performance values across the operating voltage and temperature limits. Fortunately for the system designers, FACT has taken the necessary steps to guarantee incident wave switching on transmission lines with impedances as low as 50Ω for the commercial temperature range and 75Ω for the military temperature range.

Figure 1-2 shows a Bergeron diagram for switching both HIGH-to-LOW and LOW-to-HIGH. On the right side of the graph ($I_{OUT} > 0$), are the V_{OH} and I_{IH} curves for FACT logic while on the left side ($I_{OUT} < 0$), are the curves for V_{OL} and I_{IL} . Although we will only discuss here the LOW-to-HIGH transition, the information presented may be applied to a HIGH-to-LOW transition.

Dynamic Output Drive (Continued)

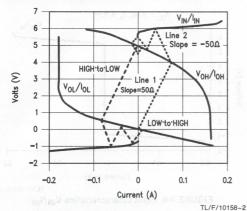


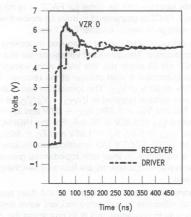
FIGURE 1-2. Gate Driving 50Ω Line
Reflection Diagram

Begin analysis at the VOL (quiescent) point. This is the intersection of the V_{OL}/I_{OL} curve for the output and the V_{IN}/I_{IN} curve for the input. For CMOS inputs and outputs, this point will be approximately 100 mV. Then draw a 50Ω load line from this intersection to the VOH/IOH curve as shown by Line 1. This intersection is the voltage that the incident wave will have. Here it occurs at approximately 3.95V. Then draw a line with a slope of -50Ω from this first intersection point to the VIN/IIN curve as shown by Line 2. This second intersection will be the first reflection back from the input gate. Continue this process of drawing the load lines from each intersection to the next. Lines terminating on the VOH/IOH curve should have positive slopes while lines terminating on the V_{IN}/I_{IN} curve should have negative slopes. Each intersection point predicts the voltage of each reflected wave on the transmission line. Intersection points on the V_{OH}/I_{OH} curve will be waves travelling from the driver to the receiver while intersection points on the VIN/IIN curve will be waves travelling from the receiver to the driver.

Figures 1-3a and 1-3b show the resultant waveforms. Each division on the time scale represents the propagation delay of the transmission line.



FIGURE 1-3a. Resultant Waveforms Driving
50Ω Line—Theoretical



TL/F/10158-4
FIGURE 1-3a. Resultant Waveforms Driving
500 Line—Actual

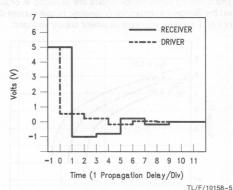


FIGURE 1-3b. Resultant Waveforms Driving 50Ω Line—Theoretical

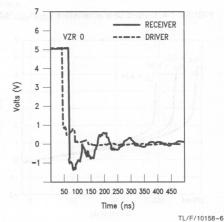


FIGURE 1-3b. Resultant Waveforms Driving 50Ω Line—Actual

1-5

Dynamic Output Drive (Continued)

While this exercise can be done for FACT, it is no longer necessary. FACT is guaranteed to drive an incident wave of enough voltage to switch another FACT input.

We can calculate what current is required by looking at the Bergeron diagram. The quiescent voltage on the line will be within 100 mV of either rail. We know what voltage is required to guarantee a valid voltage at the receiver. This is either 70% or 30% of V $_{CC}$. The formula for calculating the current and voltage required is $\left|(V_{OQ}-V_{I})/Z_{O}\right|$ at V_{I} . For $V_{OQ}=100$ mV, $V_{IH}=3.85$ V, $V_{CC}=5.5$ V and $Z_{O}=50\Omega$, the required I_{OH} at 3.85V is 75 mA. For the HIGH-to-LOW transition, $V_{OQ}=5.4$ V, $V_{IL}=1.35$ V and $Z_{O}=50\Omega$, I_{OL} is 75 mA at 1.65V. FACT's I/O specifications include these limits. For transmission lines with impedances greater than 50Ω , the current requirements are less and switching is still guaranteed.

It is important to note that the typical 24 mA drive specification is not adequate to guarantee incident wave switching. The only way to guarantee this is to guarantee the current required to switch a transmission line from the output quiescent point to the valid $V_{\rm IN}$ level.

The following performance charts are provided in order to aid the designer in determining dynamic output current drive of FACT devices with various power supply voltages.

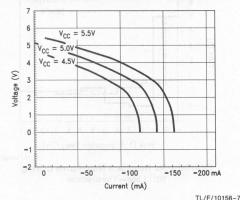


FIGURE 1-4. Output Characteristics V_{OH}/I_{OH}, 'AC00

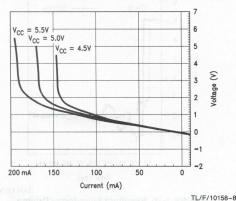


FIGURE 1-5. Output Characteristics V_{OL}/I_{OL}, 'AC00

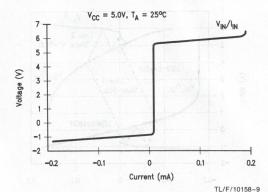


FIGURE 1-6. Input Characteristics V_{IN}/I_{IN}

Choice of Voltage Specifications

To obtain better performance and higher density, semiconductor technologies are reducing the vertical and horizontal dimensions of integrated device structures. Due to a number of electrical limitations in the manufacture of VLSI devices and the need for low voltage operation in memory cards, it was decided by the JEDEC committee to establish interface standards for devices operating at $3.3V\pm0.3V.$ To this end, National Semiconductor guarantees all of its devices operational at $3.3V\pm0.3V.$ Note also that AC and DC specifications are guaranteed between 3.0V and 5.5V. Operation of FACT logic is also guaranteed from 2.0V to 6.0V on VCC.

Operating Voltage Ranges

| FACT | = 2.0V to 6.0V analysis amon not assessed and |
|------|---|
| ALS | = 5.0V ±10% |
| LS | $= 5.0V \pm 5\%$ |
| HC | = 2.0V to 6.0V |

FACT Replaces Existing Logic

National Semiconductor's Advanced CMOS family is specifically designed to outperform existing CMOS and Bipolar logic families. *Figure 1-7* shows the relative position of various logic families in speed/power performance. FACT exhibits 1 ns internal propagation delays while consuming 1 μ W of power.

The Logic Family Comparisons table below summarizes the key performance specifications for various competitive technology logic families.

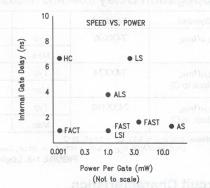


FIGURE 1-7. Internal Gate Delays

General Characteristics (All Max Ratings)

| (| | | | | | | |
|--|---|-------------------------|-------------------------|------------------------------|-----------------------------|-----------------------------|---------------|
| Symbol | Characteristics | LS | ALS | HCMOS | and sawingsm to FA | СТ | Unite |
| ya becelq | at so that eater ame | e uni ave oov | bna sV | war consumption | OA 'AC | 'ACT | V °C V V V μA |
| V _{CC/EE/DD} | Operating Voltage Range | 5±5% | 5±10% | 2.0 to 6.0 | 2.0 to 6.0 | 2.0 to 6.0 | ٧ |
| T _A 74 Series T _A 54 Series | Operating Temperature Range | 0 to +70 -55 to +125 | 0 to +70 -55 to +125 | -40 to +85 -55 to +125 | -40 to +85 -55 to +125 | -40 to +85 -55 to +125 | °C |
| V _{IH} (Min) | Input Voltage | 2.0 | 2.0 | 3.15 | 3.85 | 2.0 | ٧ |
| V _{IL} (Max) | (Limits) | 0.8 | 0.8 | 0.9 | 1.65 | 0.8 | ٧ |
| V _{OH} (Min) | Output Voltage (Limits) | 2.7 | 2.7 | V _{CC} - 0.1 | V _{CC} - 0.1 | V _{CC} - 0.1 | ٧ |
| V _{OL} (Max) | | 0.5 | 0.5 | 0.1 | 0.1 | 0.1 | ٧ |
| IH-ni eni es | Input Current | 20 | 20 | +1.0 | 9081 + 1.0 QUE 18 | +1.0 | μΑ |
| IIL juging pri | noy, Also 98 is similar to A in the case of internal | -400 | -200 | -1.0 | -1.0 | -1.0 | μΑ |
| ГОН | Output Current | -0.4 | -0.4 | -4.0 @ V _{CC} - 0.8 | -24 @ V _{CC} - 0.8 | -24 @ V _{CC} - 0.8 | mA |
| loL | at V ₀ (Limit) | 8.0 | 8.0 | 4.0 @ 0.4V | 24 @ 0.44V | 24 @ 0.44V | mA |
| DCM o mu | DC Noise Margin LOW/HIGH | 0.3/0.7 | 0.4/0.7 | 0.8/1.25 | 1.55/1.55 | 0.7/2.4 | ٧ |

Note: All DC parameters are specified over the commercial temperature range.

Speed/Power Characteristics (All Typical Ratings)

| Symbol | Characteristics | LS | ALS | HCMOS | FACT | Units | |
|------------------|-------------------------------|-----|-----|--------|--------|-------|--|
| IG | Quiescent Supply Current/Gate | 0.4 | 0.2 | 0.0005 | 0.0005 | mA | |
| P _G | Power/Gate (Quiescent) | 2.0 | 1.2 | 0.0025 | 0.0025 | mW | |
| tp | Propagation Delay | 7.0 | 5.0 | 8.0 | 5.0 | ns | |
| | Speed Power Product | 14 | 6.0 | 0.02 | 0.01 | pJ | |
| f _{max} | Clock Frequency D/FF | 33 | 50 | 50 | 160 | MHz | |

FIGURE 1-8. Logic Family Comparisons

Propagation Delay (Commercial Temperature Range)

| Symbol | Product | 0 | LS | ALS | HCMOS | FACT | Units |
|--|---------|-----|------|------|-------|------|-------|
| t _{PLH} /t _{PHL} | 74XX00 | Тур | 10.0 | 5.0 | 8.0 | 5.0 | ns |
| | | Max | _ | 11.0 | 23.0 | 8.5 | ns |
| t _{PLH} /t _{PHL} (Clock to Q) | 74XX74 | Тур | 30.0 | 12.0 | 12.0 | 8.0 | ns |
| | 2.04.00 | Max | _ | 18.0 | 44.0 | 10.5 | ns |
| t _{PLH} /t _{PHL} (Clock to Q) | 74XX163 | Тур | 27.0 | 10.0 | 20.0 | 5.0 | ns |
| | 10 1841 | Max | _ | 20.0 | 52.0 | 10.0 | ns |

Conditions: (LS) $V_{CC} = 5.0V$, $C_L = 15 pF$, 25°C;

(ALS/HC/FACT) V_{CC} = 5.0V ±10%, C_L = 50 pF, Over Temp, Max values at 0°C to +70°C for ALS, -40°C to +85°C for HC/FACT.

FIGURE 1-8. Logic Family Comparisons (Continued)

Circuit Characteristics

POWER DISSIPATION

One advantage to using CMOS logic is its extremely low power consumption. During quiescent conditions, FACT will consume several orders of magnitude less current than its bipolar counterparts. But DC power consumption is not the whole picture. Any circuit will have AC power consumption, whether it is built with CMOS or bipolar technologies.

Total power dissipation of FACT device under AC conditions is a function of three basic sources, quiescent power, internal dynamic power, and output dynamic power dissipation. Firstly, a FACT device will dissipate power in the quiescent or static condition. This can be calculated by using the formula:

PDO = Quiescent Power Dissipation

I_{CC} = Quiescent Power Supply Current Drain

V_{CC} = Power Supply Voltage

Secondly, a FACT device will dissipate power dynamically by charging and discharging internal capacitance. This can be calculated by using the formula:

PDINT = Internal Dynamic Power Dissipation

C_{PD} = Device Power Dissipation Capacitance

V_S = Output Voltage Swing

f = Internal Frequency of Operation

V_{CC} = Power Supply Voltage

 C_{PD} values are specified for each FACT device and are measured per JEDEC standards as described later on in Section 2. On FACT device data sheets, C_{PD} is a typical value and is given either for the package or for the individual stages with the device. See Section 2. For FACT devices, V_{S} and V_{CC} are the same value and can be replaced by $V_{CC}{}^{2}$ in the above formula.

Thirdly, a FACT device will dissipate power dynamically by charging and discharging any load capacitance. This can be calculated by using the following formula:

Eq. 3
$$PD_{OUT} = (C_L \cdot V_S \cdot f) \cdot V_{CC}$$

PD_{OUT} = Output Power Dissipation

C_L = Load Capacitance

V_S = Output Voltage Swing

f = Output Operating Frequency V_{CC} = Power Supply Voltage

In many cases the output frequency is the same as the internal operation frequency. Also V_S is similar to V_{CC} and can be replaced by V_{CC}^2 . In the case of internal and output frequencies being identical Eq. 2 and Eq. 3 may be combined as follows:

Eq. 4 PD =
$$(C_L + C_{PD}) \cdot V_{CC}^2 \cdot f$$

The total FACT device power dissipation is the sum of the quiescent power and all of the dynamic power dissipation. This is best described as:

Eq. 5
$$PD_{TOTAL} = PD_Q + PD_{DYNAMIC}$$
 or $PD_{TOTAL} = PD_Q + PD_{INT} + PD_{OUT}$

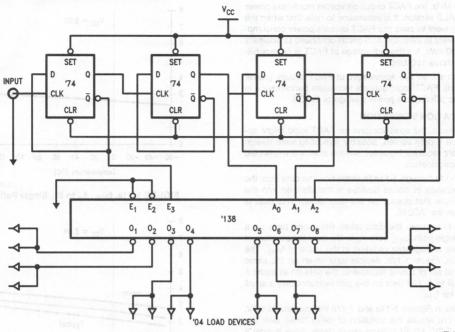


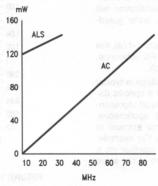
FIGURE 1-9. Power Demonstration Circuit Schematic

TL/F/10158-11

The circuit shown in *Figure 1-9* was used to compare the power consumption of FACT versus ALS devices.

Two identical circuits were built on the same board and driven from the same input. In the circuit, the input signal was driven into four D-type flip-flops which act as divide-by-2 frequency dividers. The outputs from the flip-flops were con-

nected to the inputs of a '138 decoder. This generated eight non-overlapping clock pulses on the outputs of the '138, which were then connected to an '04 inverter. The input frequency was then varied and the power consumption was measured. Figure 1-10 illustrates the results of these measurements.



TL/F/10158-12

FIGURE 1-10. FACT vs ALS Circuit Power

Below 40 MHz, the FACT circuit dissipates much less power than the ALS version. It is interesting to note that when the frequency went to zero, the FACT circuit's power consumption also went to zero; the ALS circuit continued to dissipate almost 100 mW. Another advantage of FACT is its capabilities well above 100 MHz.

This graph shows two advantages of FACT circuits (power and speed). FACT logic delivers increased performance in addition to offering the power savings of CMOS.

SPECIFICATION DERIVATION

At first glance, the specifications for FACT logic might appear to be widely spread, possibly indicating wide design margins are required. However, several effects are reflected in each specification.

Figures 1-11a through 1-11e illustrate how the data from the characterization of actual devices is transformed into the specifications that appear on the data sheet. This data is taken from the 'AC245.

Figure 1-11a shows the data taken (from one part) on a typical, single path, t_{PHL} from A_{n} to B_{n} , over temperature at 5.0V; there is negligible variation in the value of t_{PHL} . The next graph, Figure 1-11b, depicts data taken on the same device; this set of curves represents the data on all paths A to B and B to A. The data on this plot indicates only a small variation for t_{PHL} .

The graphs in Figures 1-11a and 1-11b include data at 5.0V; Figure 1-11c shows the variation of delay times over the standard 5.0V \pm 0.5V voltage range. Note there is only a \pm 6% variation in delay time due to voltage effects.

Now refer to Figure 1-11d which illustrates the process effects on delay time. This graph indicates that the process effects contribute to the spread in specifications more than any other factor in that the effects of the theoretical process spread can increase or decrease specification times by 30%. Because this 30% spread represents considerably more than ± 3 standard deviations, this guarantees an increase in the manufacturability and the quality level of FACT product. To further ensure parts within specification will pass on testers at the limits of calibration, tester guard-bands are incorporated.

With voltage and process effects added (Figure 1-11e), the full range of the specification can be seen. For reference, the data sheet values are shown on the graph.

This linear behavior with temperature and voltage is typical of CMOS. Although the graphs are drawn for a specific device, other part types have very similar graphical representations. Therefore, for performance-critical applications, where not all variables need to be taken into account at once, the user can narrow the specifications. For example, all parts in a critically timed subcircuit are together on a board, so it may be assumed the devices are at the same supply and temperature.

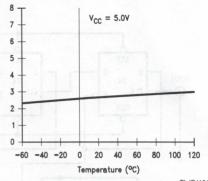


FIGURE 1-11a. t_{PHL}, A_n to B_n, Single Path

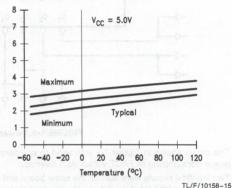
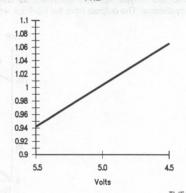


FIGURE 1-11b. tpHL A to B, All Paths

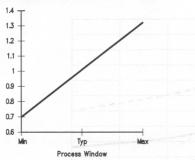


TL/F/10158-16
FIGURE 1-11c. Voltage Effects on Delay Times

1-10

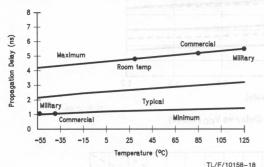
2

Circuit Characteristics (Continued)



TL/F/10158-17

FIGURE 1-11d. FACT Process Effects on Delay Times



TL/F/10158-1

FIGURE 1-11e. t_{PHL}, A to B, with Voltage and Process Variation

The same reasoning can be applied to setup and hold times. Consider the 'AC74. The setup time is 3.0 ns while the hold time is 0 ns. Theoretically, if these numbers were violated, the device would malfunction; however, in actuality, the device probably will not malfunction. Looking at the typical setup and hold times gives a better understanding of the device operation.

At 25°C and 5.0V, the setup time is 1.5 ns while the hold time is -1.5 ns. They are the same; a positive setup time means the control signal to be valid before the clock edge, a positive hold time indicates the control signal will be held valid after the clock edge for the specified time, and a negative hold time means the control signal can transition before the clock edge. FACT devices were designed to be as immune to metastability as possible. This is reflected in the typical specifications. The true "critical" time where the input is actually sampled is extremely short: less than 50 ps. By applying the same reasoning as we did to the propagation delays to the setup and hold times, it becomes obvious that the spread from setup to hold time (3 ns worst-case) really covers devices across the entire process/temperature/voltage spread. The real difference between the setup and hold times for any single device, at a specified temperature and voltage, is negligible.

CAPACITIVE LOADING EFFECTS

In addition to temperature and power supply effects, capacitive loading effects for loads greater than 50 pF should be taken into account for propagation delays of FACT devices. Minimum delay numbers may be determined from the table below. Propagation delay are measured to the 50% point of the output waveform.

| Parameter | enia , | Units | | |
|------------------|--------|-------|------|--------|
| rarameter | 3.0 | 4.5 | 5.5 | Ullits |
| t _{PLH} | 31 | 22 | 19 | ps/pF |
| t _{PHL} | 18 | 13 | 12.5 | ps/pF |

 $T_A = 25^{\circ}C$

The two graphs following, Figures 1-12 and 1-13, describe propagation delays on FACT devices as affected by variations in power supply voltage ($V_{\rm CC}$) and lumped load capacitance ($C_{\rm L}$). Figures 1-14 and 1-15 show the effects of lumped load capacitance on rise and fall times for FACT devices.

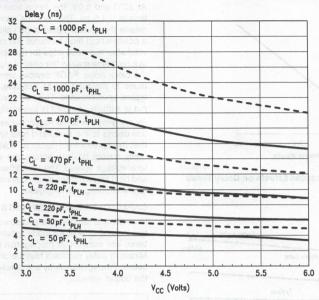


FIGURE 1-12. Propagation Delay vs V_{CC} ('AC00)

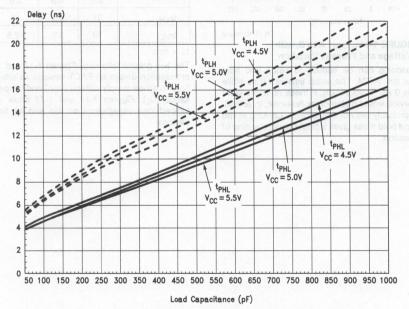


FIGURE 1-13. Propagation Delay vs C_L ('AC00)

TL/F/10158-20

TL/F/10158-19

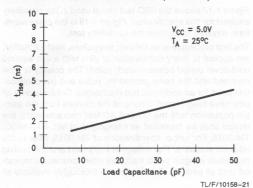


FIGURE 1-14. t_{rise} vs Capacitance

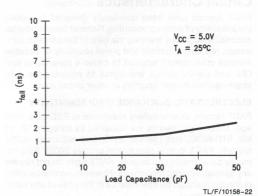


FIGURE 1-15. t_{fall} vs Capacitance

LATCH-UP

A major problem with CMOS has been its sensitivity to latch-up, usually attributed to high parasitic gains and high input impedance. FACT logic is guaranteed not to latch-up with dynamic currents of 100 mA forced into or out of the inputs or the outputs under worst case conditions ($T_A = 125^{\circ}\text{C}$ and $V_{CC} = 5.5 \, V_{DC}$). At room temperature the parts can typically withstand dynamic currents of over 450 mA. For most designs, latch-up will not be a problem, but the designer should be aware of its causes and how to prevent it.

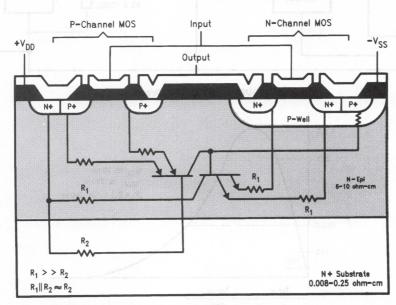


FIGURE 1-16. FACT EPI Process Cross Section with Latch-up Circuit Model

TL/F/10158-23

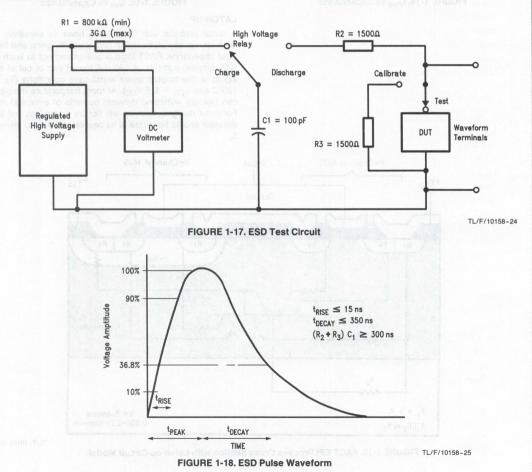
FACT devices have been specifically designed to reduce the possibility of latch-up occurring; National Semiconductor accomplished this by lowering the gain of the parasitic transistors, reducing substrate and p-well resistivity to increase external drive current required to cause a parasitic to turn ON, and careful design and layout to minimize the substrate-injected current coupling to other circuit areas.

ELECTROSTATIC DISCHARGE (ESD) SENSITIVITY

FACT circuits show excellent resistance to ESD-type damage. These logic devices are classified as category "B" of MIL-STD-883C, test method 3015, and withstand 4000V typically. FACT logic is guaranteed to have 2000V ESD immunity on all inputs and outputs. FACT parts do not require any special handling procedures. However, normal handling precautions should be observed as in the case of any semi-conductor device.

Figure 1-17 shows the ESD test circuit used in the sensitivity analysis for this specification. Figure 1-18 is the pulse waveform required to perform the sensitivity test.

The test procedure is as follows; five pulses, each of 2000V, are applied to every combination of pins with a five second cool-down period between each pulse. The polarity is then reversed and the same procedure, pulse and pin combination used for an additional five discharges. Continue until all pins have been tested. If none of the devices from the sample population fails the DC and AC test characteristics, the device shall be classified as category B of MIL-STD-883C, TM-3015. For further specifications of TM-3015, refer to the relevant standard. The voltage is increased and the testing procedure is again performed; this entire process is repeated until all pins fail. This is done to thoroughly evaluate all pins.



RADIATION TOLERANCE

Semiconductors subjected to radiation environments undergo degradation in operating life as their exposure to radiation increases. As technology advances, so does the demand for radiation-tolerant devices. National is meeting this challenge by developing the FACT family into a comprehensive radiation tolerant product for present and future radhard needs. Such applications include:

- Space
- Satellites
- Space Stations
- Airborne and Military
- Fighters/Bombers
- Missile Systems
- Ground Based Systems
- Navigation & Communications
- Commercial
- Power Stations
- Medical
- Food and Bacterial Control

Radiation tolerant semiconductors increase the useful life of the product in which they are incorporated. Additionally, radiation tolerant devices reduce shielding requirements and improve stabilization of parametric performance, resulting in cost reductions for shielding and weight, reduce power consumption and size.

RADIATION TEST LIMITS

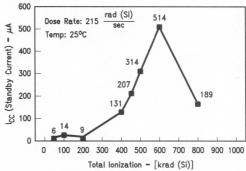
Listed below are National proposed procedures to test and guarantee FACT devices for radiation exposure limits:

- Total Dose
- Method 1019 per MIL-STD-883
- Individual limits per FACT radiation tolerant data sheet specification
- No functional failures
- Gamma rays
- Transient Dose/Latchup
- Methods 1020, 1021 per MIL-STD-883
- Minimum transient upset threshold specification
- Minimum latchup threshold specification
- Device burnout specification
- Gamma rays/Flash X-ray
- Neutron
- Test not required for CMOS product
- Single Event Upset
- To be announced in the future

SUMMARY OF TESTING

To demonstrate and verify FACT's radiation tolerance, we have characterized several standard FACT device types in a "total dose" irradiation test environment. Standard manufacturing techniques were used in the production of all circuits. Devices of the same type were manufactured from the same wafer.

Test results offer an indication of how various radiation environments affect specific standard FACT product. In most instances the standard FACT devices that were exposed to varying levels of total dose radiation showed reduced power consumption over functionally similar FAST and Schottky device types in non-radiation environments. *Figure 1-19* shows a FACT device's 54AC245 power consumption at various dose levels.



TL/F/10158-26

FIGURE 1-19. Total Dose Response (54AC245)

Total dose irradiation is presently performed "in-house" using a AECL Gamma Cell 220, Cobalt-60, source (National Bureau of Standards certified). Step-stress radiation testing is performed on each part-type. After each total dose level, a complete parametric test (DC and AC) is done and the parametric values evaluated. Because of circuit design and layout differences, each part type has its own unique radiation response.

FACT IS RADIATION TOLERANT

FACT logic employs the use of thin gate oxides, oxidation cycles, and annealing steps that enhance the tolerance of the standard FACT product line.

We are conducting additional testing and are evaluating further design enhancements for increased radiation tolerance levels of our FACT devices. Our current goal is a radiation tolerant FACT product line which exceeds the U.S. Government's VHSIC Phase II radiation requirements. At that time, National radiation tested products are guaranteed at various total dose tolerance levels ranging between 50 krads(Si) and 1 Mrad(Si).







Section 2

Ratings, Specifications
and Waveforms



Section 2 Contents

| Introduction | 2-3 |
|---|-----|
| Power Dissipation—Test Philosophy | 2-3 |
| AC Loading and Waveforms | |
| Test Conditions | |
| Rise and Fall Times | 2-5 |
| Propagation Delays, f _{max} , Set and Hold Times | 2-6 |
| Enable and Disable Times | |
| Electrostatic Discharge | 2-6 |
| Noise Characteristics | |

2-2



Ratings, Specifications and Waveforms

Specifying FACTTM Devices

Traditionally, when a semiconductor manufacturer completed a new device for introduction, specifications were based on the characterization of just a few parts. While these specifications were appealing to the designer, they were often too tight and, over time, the IC manufacturers had difficulty producing devices to the original specs. This forced the manufacturer to relax circuit specifications to reflect the actual performance of the device.

As a result, designers were required to review system designs to ensure the system would remain reliable with the new specifications. National Semiconductor realized and understood the problems associated with characterizing devices too aggressively.

To provide more realistic and manufacturable specs, National Semiconductor devised a systematic and thorough process to generate specifications. Devices are selected from multiple wafer lots to ensure process variations are taken into account. In addition, the process parameters are measured and compared to the known process limits. With more than three years of experience manufacturing FACT logic, National Semiconductor can accurately predict how these wafer lots compare with the best and worse case lots that can possibly be expected.

This method of characterizing parts more accurately represents the product across time, voltage, temperature and process rather than portraying the fastest possible device.

These specification guidelines allow designers to design systems more efficiently since the devices used will behave as documented. Unspecified guardbands no longer need to be added by the designer to ensure system reliability.

Power Dissipation—Test Philosophy

In an effort to reduce confusion about measuring power dissipation capacitance, C_{PD} , a JEDEC standard test procedure (7A Appendix E) has been adopted which specifies the test setup for each type of device. This allows a device to be exercised in a consistent manner for the purpose of specification comparison.

The following is a list of different types of logic functions, along with the input setup conditions under which the C_{PD} was measured for each type of device. By understanding how the device was exercised during C_{PD} measurements, the designer can understand whether the C_{PD} specified for that particular device reflects the total power dissipation ca-

pacitance for either the entire device or for just a certain stage of that device. For example, from the following list, it is apparent that the C_{PD} value specified for a counter reflects the internal capacitance for the entire device, since the entire device is being exercised during measurement. On the other hand, the C_{PD} value specified for an octal line driver reflects the internal capacitance for only one of eight stages, since only one input was being switched during test. Therefore the octal's overall power dissipation should be calculated for each of the eight stages, individually.

During the C_{PD} measurements, each output that is being switched should be loaded with the standard 50 pF and 500Ω load. All device measurements are made with $V_{CC} = 5.0V$ at 25°C. with TRI-STATE® outputs enabled.

Gates/Buffers/ Switch one input. Bias the remaining inputs such that one output switches.

Latches: Switch the Enable and D inputs such

that the latch toggles.

Flip-Flops: Switch the clock pin while changing D
(or bias J and K) such that the output(s) change each clock cycle. For parts with a common clock, exercise

only one flip-flop.

Decoders: Switch one address pin which chang-

es two outputs.

Multiplexers: Switch one address pin with the corresponding data inputs at opposite logic

levels so that the output switches.

Counters: Switch the clock pin with other inputs biased such that the device counts.

Switch the clock pin with other inputs

biased such that the device counts.

Transceivers: Switch one data input. For bidirection-

al devices enable only one direction.

Parity Generator: Switch one input.

Priority Encoders: Switch the lowest priority input.

AC Loading and Waveforms

LOADING CIRCUIT

Shift Registers:

Figure 1 shows the AC loading circuit used in characterizing and specifying propagation delays of all FACT devices ('AC and 'ACT) unless otherwise specified in the data sheet of a specific device.

AC Loading and Waveforms (Continued)

The use of this load, which is equivalent to the FASTTM (Fairchild Advanced Schottky TTL) test iig, differs somewhat from previous (HCMOS) practice. This provides more meaningful information and minimizes problems of instrumentation and customer correlation. In the past, +25°C propagation delays for TTL devices were specified with a load of 15 pF to ground; this required great care in building test jigs to minimize stray capacitance and implied the use of high impedance, high frequency scope probes. FAST circuits changed to 50 pF of capacitance, allowing more leeway in stray capacitance and also loading the device during rising or falling output transitions. This more closely resembles the inloading to be expected in avarage applications and thus gives the designer more useful delay figures. We have incorporated this scheme into the FACT product line. The net effect of the change in AC load is to increase the average observed propagation delay by about 1 ns.

The 500Ω resistor to ground can be a high frequency passive probe for a sampling oscilloscope, which costs much less than the equivalent high impedance probe. Alternately, the 500Ω resistor to ground can simply be a 450Ω resistor feeding into a 50Ω coaxial cable leading to a sampling scope input connector, with the internal 50Ω termination of the scope completing the path to ground. This is the preferred scheme for correlation. (See *Figure 1*.) With this scheme there should be a matching cable from the device input pin to the other input of the sampling scope; this also serves as a 50Ω termination for the pulse generator that supplies the input signal.

Shown in *Figure 1* is a second 500Ω resistor from the device output to a switch. For most measurements this switch is open; it is closed for measuring one set of the Enable/

Disable parameters (LOW-to-OFF and OFF-to-LOW) of a TRI-STATE output. With the switch closed, the pair of 500Ω resistors and the 2 \times V_{CC} supply voltage establish a quiescent HIGH level.

Test Conditions

Figures 2a and 2b describe the input signal voltage levels to be used when testing FACT circuits. The AC test conditions follow industry convention requiring $V_{\rm IN}$ to range from 0V for a logic LOW to 3.0V for a logic HIGH for 'ACT devices and 0V to $V_{\rm CC}$ for 'AC devices. The DC parameters are normally tested with $V_{\rm IN}$ at guaranteed input levels, that is $V_{\rm IH}$ to $V_{\rm IL}$ (see data tables for details). Care must be taken to adequately decouple these high performance parts and to protect the test signals from electrical noise. In an electrically noisy environment, (e.g., a tester and handler not specifically designed for high speed work), DC input levels may need to be adjusted to increase the noise margin to allow for the extra noise in the tester which would not be seen in a system.

Noise immunity testing is performed by raising V_{IN} to the nominal supply voltage of 5.0V then dropping to a level corresponding to V_{IH} characteristics, and then raising again to the 5.0V level. Noise tests can also be performed on the V_{IL} characteristics by raising V_{IN} from 0V to V_{IL} , then returning to 0V. Both V_{IH} and V_{IL} noise immunity tests should not induce a switch condition on the appropriate outputs of the FACT device.

Good high frequency wiring practices should be used in constructing test jigs. Leads on the load capacitor should be as short as possible to minimize ripples on the output wave-

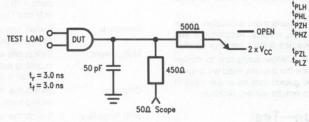


FIGURE 1. AC Loading Circuit

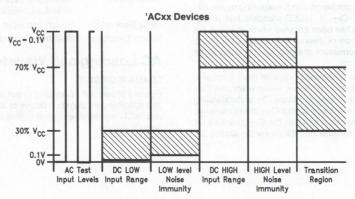


FIGURE 2a. Test Input Signal Levels

TL/F/10159-2

TL/F/10159-1





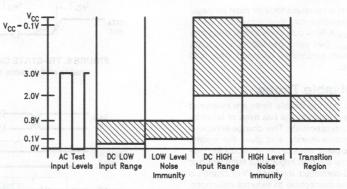


FIGURE 2b. Test Input Signal Levels

TL/F/10159-3

form transitions and to minimize undershoot. Generous ground metal (preferably a ground plane) should be used for the same reasons. A V_{CC} bypass capacitor should be provided at the test socket, also with minimum lead lengths.

Rise and Fall Times

Input signals should have rise and fall times of 3.0 ns and signal swing of 0V to 3.0V V_{CC} for 'ACT devices or 0V to V_{CC} for 'AC devices. Rise and fall times less than or equal to 1 ns should be used for testing f_{max} or pulse widths.

CMOS devices, including 4000 Series CMOS, HC, HCT and FACT families, tend to oscillate when the input rise and fall times become lengthy. As a direct result of its increased performance, FACT devices can be more sensitive to slow input rise and fall times than other lower performance technologies.

It is important to understand why this oscillation occurs. Consider the outputs, where the problem is initiated. Usually, CMOS outputs drive capacitive loads with low DC leakage. When the output changes from a HIGH level to a LOW level, or from a LOW level to a HIGH level, this capacitance has to be charged or discharged. With the present high performance technologies, this charging or discharging takes place in a very short time, typically 2–3 ns. The requirement to charge or discharge the capacitive loads quickly creates a condition where the instantaneous current change through the output structure is quite high. A voltage is generated across the V_{CC} or ground leads inside the package due to the inductance of these leads. The internal ground of the chip will change in reference to the outside world because of this induced voltage.

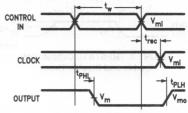
TL/F/10159-4
FIGURE 3. Waveform for Inverting

and Non-Inverting Functions

 $^*V_{mi} = 50\%~V_{CC}$ for 'AC devices; 1.5V for 'ACT devices $V_{mo} = 50\%~V_{CC}$ for 'AC/'ACT devices

Consider the input. If the internal ground changes, the input voltage level appears to change to the DUT. If the input rise time is slow enough, its level might still be in the device threshold region, or very close to it, when the output switches. If the internally-induced voltage is large enough, it is possible to shift the threshold region enough so that it recrosses the input level. If the gain of the device is sufficient and the input rise or fall time is slow enough, then the device may go into oscillation. As device propagation delays become shorter, the inputs will have less time to rise or fall through the threshold region. As device gains increase, the outputs will swing more, creating more induced voltage. Instantaneous current change will be greater as outputs become quicker, generating more induced voltage.

Package-related causes of output oscillation are not entirely to blame for problems with input rise and fall time measurements. All testers have $V_{\rm CC}$ and ground leads with a finite inductance. This inductance needs to be added to the inductance in the package to determine the overall voltage which will be induced when the outputs change. As the reference for the input signals moves further away from the pin under test, the test will be more susceptible to problems caused by the inductance of the leads and stray noise. Any noise on the input signal will also cause problems. With FACT logic having gains as high as 100, it merely takes a 50 mV change in the input to generate a full 5V swing on the output.



TL/F/10159-5

FIGURE 4. Propagation Delay, Pulse Width and t_{rec} Waveforms

Propagation Delays, f_{max}, Set and Hold Times

A 1.0 MHz square wave is recommended for most propagation delay tests. The repetition rate must necessarily be increased for testing $f_{\text{max}}.$ A 50% duty cycle should always be used when testing $f_{\text{max}}.$ Two pulse generators are usually required for testing such parameters as setup time, hold time, recovery time, etc.

Enable and Disable Times

Figures 5 and 6 show that the disable times are measured at the point where the output voltage has risen or fallen by 0.3V from VOI or VOH, respectively. This change enhances the repeatability of measurements, and gives the system designer more realistic delay times to use in calculating minimum cycle times. Since the high impedance state rising or falling waveform is RC-controlled, the first 0.3V of change is more linear and is less susceptible to external influences. More importantly, perhaps from the system designer's point of view, a change in voltage of 0.3V is adequate to ensure that a device output has turned OFF. Measuring to a larger change in voltage merely exaggerates the apparent Disable times and thus penalizes system performance since the designer must use the Enable and Disable times to devise worst case timing signals to ensure that the output of one device is disabled before that of another device is enabled. Note that the measurement points have been changed from the previous 10% and 90% points. This better reflects actual test points and does not change specification limits.

Electrostatic Discharge

Precautions should be taken to prevent damage to devices by electrostatic discharge. Static charge tends to accumulate on insulated surfaces such as synthetic fabrics or carpeting, plastic sheets, trays, foam, tubes or bags, and on ungrounded electrical tools or appliances. The problem is much worse in a dry atmosphere. In general, it is recommended that individuals take the precaution of touching a known ground before handling devices. To effectively avoid electrostatic damage to FACT devices, it is recommended that individuals wear a grounded wrist strap when handling devices. More often, handling equipment, which is not properly grounded, causes damage to parts. Ensure that all plastic parts of the tester, which are near the device, are conductive and connected to ground.

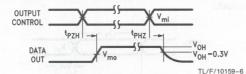


FIGURE 5. TRI-STATE Output High Enable and Disable Times

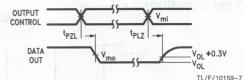
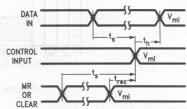


FIGURE 6. TRI-STATE Output Low Enable and Disable Times



TL/F/10159-8

FIGURE 7. Setup Time, Hold Time and Recovery Time

 $^*V_{mi} = 50\% \ V_{CC}$ for 'AC devices; 1.5V for 'ACT devices $V_{mo} = 50\% \ V_{CC}$ for 'AC/'ACT devices

FACT Noise Characteristics

The setup of a noise characteristics measurement is critical to the accuracy and repeatability of the tests. The following is a brief description of the setup used to measure the noise characteristics of FACT.

Equipment:

Hewlett Packard Model 8180A Word Generator PC-163A Test Fixture

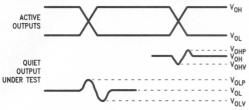
Tektronics Model 7854 Oscilloscope

Procedure:

- 1. Verify Test Fixture Loading: Standard Load 50 pF, 500Ω.
- 2. Deskew the word generator so that no two channels have greater than 150 ps skew between them. This requires that the oscilloscope be deskewed first. Swap out the channels that have more than 150 ps of skew until all channels being used are within 150 ps. It is important to deskew the word generator channels before testing. This will ensure that the outputs switch simultaneously.
- Terminate all inputs and outputs to ensure proper loading of the outputs and that the input levels are at the correct voltage.
- 4. Set V_{CC} to 5.0V.

FACT Noise Characteristics (Continued)

Set the word generator to toggle all but one output at a frequency of 1 MHz. Greater frequencies will increase DUT heating and affect the results of the measurement.



TL/F/10159-9

FIGURE 8. Quiet Output Noise Voltage Waveforms

Note A. V_{OHV} and V_{OLP} are measured with respect to ground reference. **Note B.** Input pulses have the following characteristics: f=1 MHz, $t_f=3$ ns, $t_f=3$ ns, skew < 150 ps.

 Set the word generator input levels at 0V LOW and 3V HIGH for ACT devices and 0V LOW and 5V HIGH for AC devices. Verify levels with a digital volt meter.

VOLP/VOLV and VOHP/VOHV:

 Determine the quiet output pin that demonstrates the greatest noise levels. The worst case pin will usually be the furthest from the ground pin. Monitor the output voltages using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.

- Measure V_{OLP} and V_{OLV} on the quiet output during the HL transition. Measure V_{OHP} and V_{OHV} on the quiet output during the LH transition.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

VILD and VIHD:

- Monitor one of the switching outputs using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- First increase the input LOW voltage level, V_{IL}, until the output begins to oscillate. Oscillation is defined as noise on the output LOW level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input LOW voltage level at which oscillation occurs is defined as V_{ILD}.
- Next increase the input HIGH voltage level on the word generator, V_{IH} until the output begins to oscillate. Oscillation is defined as noise on the output LOW level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input HIGH voltage level at which oscillation occurs is defined as V_{IHD}.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

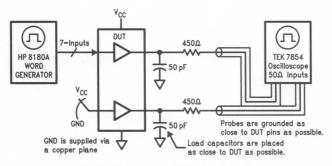


FIGURE 9. Simultaneous Switching Test Circuit

TL/F/10159-10

FACT Voice Characteristics (Common)

Set the word generator to roggle all but one output it a fractionary of 1 MHz. Greater frequencies will increase DUT beating and affect the results of the measurement.



9-931011

Figurit S. Opiet Output Notes Voltage Way forms

Bote A. Voyy and Voy platé maken et win caped to ground not underes. Audit A. A. Andrew Miller to form pulses have the following elementaristics (to a tight of the plate to a single bound of the plate to a single boun

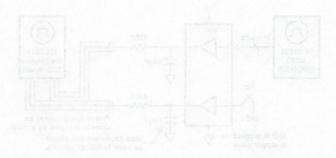
Verby and Vibrary ray variety

 Determine the quiet dupput pin that demonstrates the general horse levels. The worst pass pin will usually be the furthest from the ground pin. Monifor the output workting using a 500 coaxial cable plugged into a standard state type connector on the test fixture. Do not use an across EFT across.

- Monsure V_{DLP} and V_{DLV} on the quiet output during the 14L transition. Measure V_{DLV} and V_{DLV} on the quiet out pur during the LLL analten.
- Verify that they CNU reterence renorded on the oscillon scope has not deliber to ensure the accuracy and reject ext. Ryrof the measurements.
 - OHIV DAS OLI
- Monitor one of the switching outputs using a 50Ω coaxiet on collection on state subget connector on the rest tilture. Eon not use an active EET processing the rest tilture.

First increase the local LOV validate level. V_E until the current begins to esculate Cociliation is defined as noise on the oxident LOW jevel that excepts V_E limits, or on output AIGH revels that except V_E units. The input output except as the level of the cocoliation occurs is defined to.

- Next increase the input HIGH voltage level on the word obtainers, ye until the output pegins to defillate. Certifue increases we are not on the output NOW level that exceeds V_H inmits or on output HIGH level that exceed V_H lemits 1 not input HIGH voltage level or writer osmits ton occurs is defined as v_{HP}.
- Wines, editino begiocen appender CVID, edit Jafit vinov.
 desperbita y eruppa edit equene pi pedibbitor sall'appendente pi pedibbito villos.



recembership

FRUET 9, Simultanaous Switching 1 set Croud





Section 3 **Design Considerations**



Section 3 Contents

| Introduction | 3-3 |
|---|------|
| Interfacing | 3-3 |
| Line Driving and Termination | 3-4 |
| Crosstalk | 3-7 |
| Ground Bounce | 3-10 |
| Decoupling Requirements | 3-15 |
| Electromagnetic Interference | 3-16 |
| TTL-Compatible CMOS Designs Require I _{CC} Consideration | 3-20 |
| Testing Advanced CMOS with I/O Pins | 3-21 |
| Testing Disable Times of TRI-STATE Outputs in a Transmission Line Environment | 3-22 |
| Understanding Latch-Up in Advanced CMOS Logic | 3-24 |



Design Considerations

Today's system designer is faced with the problem of keeping ahead when addressing system performance and reliability. National Semiconductor's CMOS helps designers achieve these goals.

FACTTM (Fairchild Advanced CMOS Technology) logic was designed to alleviate many of the drawbacks that are common to current technology logic circuits. FACT logic combines the low static power consumption and the high noise margins of CMOS with a high fan-out, low input loading and a 50Ω transmission line drive capability (comparable to National Semiconductor's FAST bipolar technology family) to offer a complete family of 1.3-micron SSI, MSI and LSI devices.

Performance features such as advanced Schottky speeds at CMOS power levels, advanced Schottky drive, excellent noise, ESD and latch-up immunity are characteristics that designers of state-of-the-art systems require. FACT logic answers all of these concerns in one family of products. To fully utilize the advantages provided by FACT, the system designer should have an understanding of the flexibility as well as the trade-offs of CMOS design. The following section discusses common design concerns relative to the performance and requirements of FACT.

There are six items of interest which need to be evaluated when implementing FACT devices in new designs:

- Interfacing—interboard and technology interfaces, battery backup and power down or live insert/extract systems require some special thought.
- Transmission Line Driving—FACT has line driving capabilities superior to all CMOS families and most TTL families.
- Noise effects—As edge rates increase, the probability of crosstalk and ground bounce problems increases. The enhanced noise immunity and high threshold levels improve FACT's resistance to crosstalk problems.
- Board Layout—Prudent board layout will ensure that most noise effects are minimized.
- Power Supplies and Decoupling—Maximize ground and V_{CC} traces to keep V_{CC}/ground impedance as low as possible; full ground/V_{CC} planes are best. Decouple any device driving a transmission line; otherwise add one capacitor for every package.
- Electromagnetic Interference

Interfacing

FACT devices have outputs which combine balanced CMOS outputs with high current line driving capability. Each standard output is guaranteed to source or sink 24 mA of current at worst case conditions. This allows FACT circuits to drive more loads than standard advanced Schottky parts; FACT can directly drive FAST®, ALS, AS, LS, HC and HCT devices.

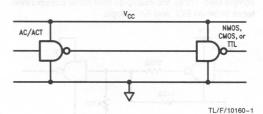
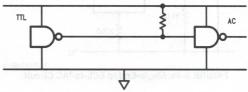


FIGURE 3-1. Interfacing FACT to NMOS, CMOS and TTL

FACT devices can be directly driven by both NMOS and CMOS families, as shown in *Figure 3-1*, operating at the same rail potential without special considerations. This is possible due to the low input loading of FACT product, guaranteed to be less than 1 μ A per input.

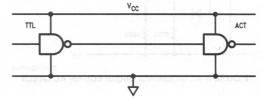
Some older technologies, including all existing TTL families, will not be able to drive FACT circuits directly; this is due to inadequate high level capability, which is guaranteed to 2.4V. There are two simple approaches to the TTL-to-FACT interface problem. A TTL-to-CMOS converter can be constructed employing a resistor pull-up to $V_{\rm CC}$ of approximately 4.7 $k\Omega$, which is depicted in $\it Figure~3-2$. The correct HIGH level is seen by the CMOS device while not loading down the TTL driver.



TL/F/10160-2

FIGURE 3-2. VIH Pull-Up on TTL Outputs

Unfortunately, there will be designs where including a pullup resistor will not be acceptable. In these cases, such as a terminated TTL bus, National Semiconductor has designed devices which offer thresholds that are TTL-compatible (Figure 3-3). These interfaces tend to be slightly slower than their CMOS-level counterparts due to an extra buffer stage required for level conversion.



TI /F/10160-3

FIGURE 3-3. TTL Interfacing to 'ACT

Interfacing (Continued)

ECL devices cannot directly drive FACT devices. Interfacing FACT-to-ECL can be accomplished by using TTL-to-ECL translators and 10125 ECL-to-TTL translators in addition to following the same rules on the TTL outputs to CMOS inputs (i.e., a resistor pull-up to V_{CC} of approximately 4.7 kΩ). The translation can also be accomplished by a resistive network. A three-resistor interface between FACT and ECL logic is illustrated in *Figure 3-4a*. *Figures 3-4b* and *3-4c* show the translation from ECL-to-FACT, which is somewhat more complicated. These two examples offer some possible interfaces between ECL and FACT logic.

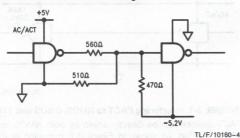


FIGURE 3-4a. Resistive FACT-to-ECL Translation

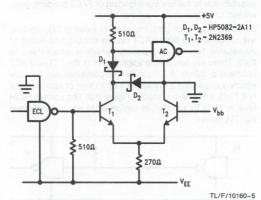


FIGURE 3-4b. Single-Ended ECL-to-'AC Circuit

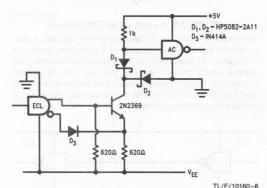


FIGURE 3-4c. Differential Output ECL-to-'AC Circuit

It should be understood that for FACT, as with other CMOS technologies, input levels that are between specified input values will cause both transistors in the CMOS structure to be conducting. This will cause a low resistive path from the supply rail to ground, increasing the power consumption by several orders of magnitude. It is important that CMOS inputs are always driven as close as possible to the rail.

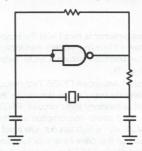


FIGURE 3-5. Crystal Oscillator Circuit
Implemented with FACT 'AC00

TL/F/10160-7

Line Driving and Termination

With the available high-speed logic families, designers can reach new heights in system performance. Yet, these faster devices require a closer look at transmission line effects.

Although all circuit conductors have transmission line properties, these characteristics become significant when the edge rates of the drivers are equal to or less than three times the propagation delay of the line. Significant transmission line properties may be exhibited in an example where devices have edge rates of 3 ns and lines of 8 inches or greater, assuming propagation delays of 1.7 ns/ft for an unloaded printed circuit trace.

Of the many properties of transmission lines, two are of major interest to the system designer: Z_{Oe} , the effective equivalent impedance of the line, and t_{pde} , the effective propagation delay down the line. It should be noted that the intrinsic values of line impedance and propagation delay, Z_{O} and t_{pd} , are geometry-dependent. Once the intrinsic values are known, the effects of gate loading can be calculated. The loaded values for Z_{Oe} and t_{pde} can be calculated with:

$$Z_{\text{oe}} = \frac{Z_0}{\sqrt{1 + C_t/C_l}}$$

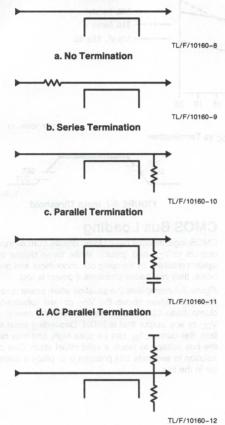
$$t_{\text{pde}} = t_{\text{pd}}\sqrt{1 + C_t/C_l}$$

where $C_l=$ intrinsic line capacitance and $C_t=$ additional capacitance due to gate loading.

The formulas indicate that the loading of lines decreases the effective impedance of the line and increases the propagation delay. Lines that have a propagation delay greater than one third the rise time of the signal driver should be evaluated for transmission line effects. When performing transmission line analysis on a bus, only the longest, most heavily loaded and the shortest, least loaded lines need to be analyzed. All lines in a bus should be terminated equally; if one line requires termination, all lines in the bus should be terminated. This will ensure similar signals on all of the lines.

Line Driving and Termination (Continued)

There are several termination schemes which may be used. Included are series, parallel, AC parallel and Thevenin terminations. AC parallel and series terminations are the most useful for low power applications since they do not consume any DC power. Parallel and Thevenin terminations experience high DC power consumption.



e. Thevenin Termination
FIGURE 3-6a. Termination Schemes

SERIES TERMINATIONS

Series terminations are most useful in high-speed applications where most of the loads are at the far end of the line. Loads that are between the driver and the end of the line will receive a two-step waveform. The first wave will be the incident wave. The amplitude is dependent upon the output impedance of the driver, the value of the series resistor and the impedance of the line according to the formula

$$V_W = V_{CC} \cdot Z_{oe} / (Z_{oe} + R_S + Z_S)$$

The amplitude will be one-half the voltage swing if R_S (the series resistor) plus the output impedance (Z_S) of the driver is equal to the line impedance. The second step of the waveform is the reflection from the end of the line and will have an amplitude equal to that of the first step. All devices on the line will receive a valid level only after the wave has propagated down the line and returned to the driver. Therefore, all inputs will see the full voltage swing within two times the delay of the line.

PARALLEL TERMINATION

Parallel terminations are not generally recommended for CMOS circuits due to their power consumption, which can exceed the power consumption of the logic itself. The power consumption of parallel terminations is a function of the resistor value and the duty cycle of the signal. In addition, parallel termination tends to bias the output levels of the driver towards either V_{CC} or ground. While this feature is not desirable for driving CMOS inputs, it can be useful for driving TTL inputs.

AC PARALLEL TERMINATION

AC parallel terminations work well for applications where the delays caused by series terminations are unacceptable. The effects of AC parallel terminations are similar to the effects of standard parallel terminations. The major difference is that the capacitor blocks any DC current path and helps to reduce power consumption.

Thevenin Termination

Thevenin terminations are also not generally recommended due to their power consumption. Like parallel termination, a DC path to ground is created by the terminating resistors. The power consumption of a Thevenin termination, though, will generally not be a function of the signal duty cycle. Thevenin terminations are more applicable for driving CMOS inputs because they do not bias the output levels as paralleled terminations do. It should be noted that lines with Thevenin terminations should not be left floating since this will cause the input levels to float between $V_{\rm CC}$ or ground, increasing power consumption.

| ■ Parallel: | Resistor = Z _o |
|-------------|-------------------------------------|
| ■ Thevenin: | Resistor = $2 \times Z_0$ |
| Series: | Resistor = $Z_0 - Z_{out}$ |
| AC: | Resistor = Z _o |
| | Capacitor = $C \ge \frac{3td}{Z_0}$ |
| Active: | Resistor = $2 \times Z_0$ |

Figure 3-6b. Suggested Termination Values

Thevenin Termination (Continued)

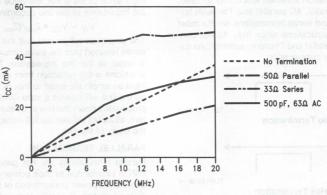


FIGURE 4-6c. FACT I_{CC} vs Termination

TL/F/10160-13

FACT circuits have been designed to drive 50Ω transmission lines over the full commercial temperature range and 75Ω transmission lines over the military temperature range. This is guaranteed by the FACT family's specified dynamic drive capability of 86 mA sink and 75 mA source current. This ensures incident wave switching on 50Ω transmission lines and is consistent with the 3 ns rated edge transition time.

FACT devices also feature balanced output totem pole structures to allow equal source and sink current capability. This gives rise to balanced edge rates and equal rise and fall times. Balanced drive capability and transition times eliminate both the need to calculate two different delay times for each signal path and the requirement to correct signal polarity for the shortest delay time.

FACT product inputs have been created to take full advantage of high output levels to deliver the maximum noise immunity to the system designer. V_{IH} and V_{IL} are specified at 70% and 30% of V_{CC} respectively. The corresponding output levels, V_{OH} and V_{OL} , are specified to be within 0.1V of the rails, of which the output is sourcing or sinking 50 μA or less. These noise margins are outlined in Figure 3-7.

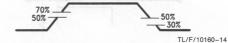


FIGURE 3-7. Input Threshold

CMOS Bus Loading

CMOS logic devices have clamp diodes from all inputs and outputs to V_{CC} and ground. While these diodes increase system reliability by damping out undershoot and overshoot noise, they can cause problems if power is lost.

Figure 3-8 exemplifies the situation when power is removed. Any input driven above the $V_{\rm CC}$ pin will forward-bias the clamp diode. Current can then flow into the device, and out $V_{\rm CC}$ or any output that is HIGH. Depending upon the system, this current, $I_{\rm IN}$, can be quite high, and may not allow the bus voltage to reach a valid HIGH state. One possible solution to eliminate this problem is to place a series resistor in the line.

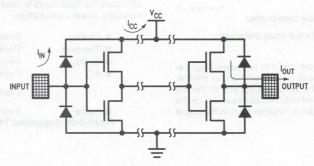


FIGURE 3-8. Noise Effects

FACT offers the best noise immunity of any competing technology available today. With input thresholds specified at 30% and 70% of V_{CC} and outputs that drive to within 100 mV of the rails, FACT devices offer noise margins approaching 30% of V_{CC} . At 5V V_{CC} , FACT's specified input and output levels give almost 1.5V of noise margin for both ground- and V_{CC} -born noise. With realistic input thresholds closer to 50% of V_{CC} , the actual margins approach 2.5V.

However, even the most advanced technology cannot alone eliminate noise problems. Good circuit board layout techniques are essential to take full advantage of the superior performance of FACT circuits.

Well-designed circuit boards also help eliminate manufacturing and testing problems.

Another recommended practice is to segment the board into a high-speed area, a medium-speed area and a low-speed area. The circuit areas with high current requirements (i.e., buffer circuits and high-speed logic) should be as close to the power supplies as possible; low-speed circuit areas can be furthest away.

Decoupling capacitors should be adjacent to all buffer chips; they should be distributed throughout the logic: one capacitor per chip. Transmission lines need to be terminated to keep reflections minimal. To minimize crosstalk, long signal lines should not be close together.

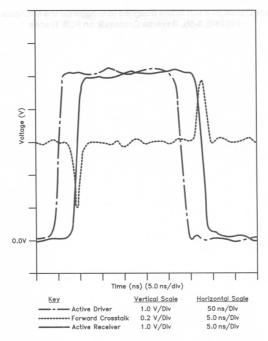
Crosstalk

The problem of crosstalk and how to deal with it is becoming more important as system performance and board densities increase. Crosstalk is the capacitive coupling of signals from one line to another. The amplitude of the noise generated on the inactive line is directly related to the edge rates of the signal on the active line, the proximity of the two lines and the distance that the two lines are adjacent.

Crosstalk has two basic causes. Forward crosstalk, Figure 3-9a, is caused by the wavefront propagating down the printed circuit trace at two different velocities. This difference in velocities is due to the difference in the dielectric constants of air ($\epsilon_{\rm f}=1.0$) and epoxy glass ($\epsilon_{\rm f}=4.7$). As the wave propagates down the trace, this difference in velocities will cause one edge to reach the end before the other. This delay is the cause of forward crosstalk; it increases with longer trace length, so consequently the magnitude of forward crosstalk will increase with distance.

Reverse crosstalk, *Figure 3-9b*, is caused by the mutual inductance and capacitance between the lines which is a transformer action. Reverse crosstalk increases linearly with distance up to a critical length. This critical length is the distance that the signal can travel during its rise or fall time.

Although crosstalk cannot be totally eliminated, there are some design techniques that can reduce system problems resulting from crosstalk. FACT's industry-leading noise margins make systems immune to crosstalk-related problems easier to design. FACT's AC noise margins, shown in Figures 3-10a and 3-10b, exemplify the outstanding immunity to everyday noise which can effect system reliability.



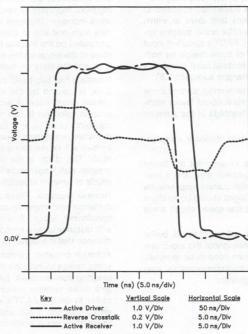
TL/F/10160-16

This figure shows traces taken on a test fixture designed to exaggerate the amplitude of crosstalk pulses.

FIGURE 3-9a, Forward Crosstalk on PCB Traces

3

Crosstalk (Continued)



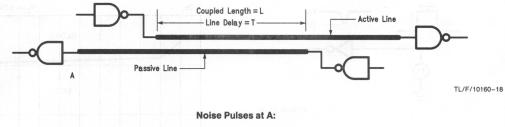
TL/F/10160-17

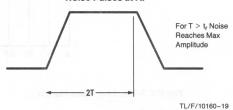
This figure shows traces taken on a test fixture designed to exaggerate the amplitude of crosstalk pulses.

FIGURE 3-9b. Reverse Crosstalk on PCB Traces



Crosstalk (Continued)



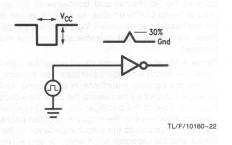




For T < 0.5 t_r
Noise Never
Reaches Full
Amplitude

TL/F/10160-21

FIGURE 3-9c. Partially Coupled Lines



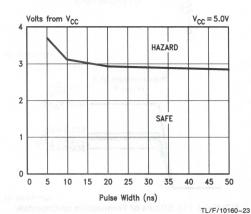
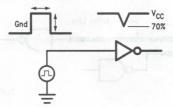
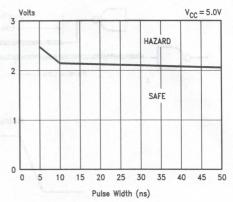


FIGURE 3-10a. High Noise Margin

Crosstalk (Continued)



TL/F/10160-24



TL/F/10160-25

FIGURE 3-10b. Low Noise Margin

With over 2.0V of noise margins, the FACT family offers better noise rejection than any other comparable technology.

In any design, the distance that lines run adjacent to each other should be kept as short as possible. The best situation is when the lines are perpendicular to each other. For those situations where lines must run parallel, the effects of crosstalk can be minimized by line termination. Terminating a line in its characteristic impedance reduces the amplitude of an initial crosstalk pulse by 50%. Terminating the line will also reduce the amount of ringing. Crosstalk problems can also be reduced by moving lines further apart or by inserting ground lines or planes between them.

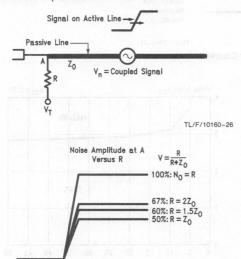
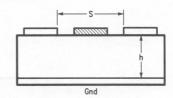


FIGURE 3-11a. Effects of Termination on Crosstalk



- Minimize parallel trace lengths
- Maximize distance "S" between traces to minimize crosstalk
- Add ground trace
 between signal traces
- Minimize distance h to keep line impedance low

TL/F/10160-32

FIGURE 3-11b. PCB Layout Tips for Crosstalk Avoidance

Ground Bounce

Ground bounce occurs as a result of the intrinsic characteristics of the leadframes and bondwires of the packages used to house CMOS devices. As edge rates and drive capability increase in advanced logic families, the effects of these intrinsic electrical characteristics become more pronounced.

Figure 3-12a shows a simple circuit model for a device in a leadframe driving a standard test load. The inductor L1 represents the parasitic inductance in the ground lead of the package; inductor L2 represents the parasitic inductance in the power lead of the package; inductor L3 represents the parasitic inductance in the output lead of the package; the resistor R1 represents the output impedance of the device output, and the capacitor and resistor C_L and R_L represent the standard test load on the ouput of the device.

Ground Bounce (Continued)

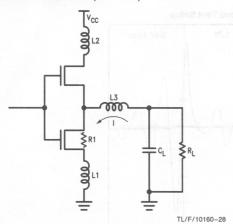


FIGURE 3-12a. Output Model

TL/F/10160-29

FIGURE 3-12b. Output Voltage

FIGURE 3-12c. Output Current

TL/F/10160-31
FIGURE 3-12d. Inductor Voltage

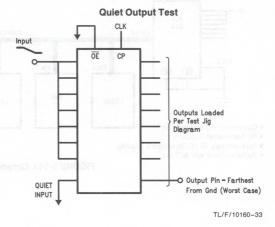
The three waveforms shown in Figures 3-12b, c and d, depict how ground bounce is generated. The first waveform shows the voltage (V) across the load as it is switched from a logic HIGH to a logic LOW. The output slew rate is dependent upon the characteristics of the output transistor, the inductors L1 and L3, and C_L, the load capacitance. The second waveform shows the current that is generated as the capacitor discharges [I = C_L • dV/dt]. The third wave-

form shows the voltage that is induced across the inductance in the ground lead due to the changing currents [V_gb = $-L \bullet (dI/dt)$].

Note: These models are included in order to assist in generating an understanding of where Ground Bounce originates. They are not intended to be used to predict the amplitude or duration of Ground Bounce noise. To use them as such will give inaccurate results. If all factors are taken into account, highly complex equations will result. Since these models are so complex, we shall use empirical results to develop an understanding of Ground Bounce.

There are many factors which affect the amplitude of the ground bounce. Included are:

- Number of outputs switching simultaneously: more outputs results in more ground bounce.
- Type of output load: capacitive loads generate two to three times more ground bounce than typical system traces. Increasing the capacitive load to approximately 60 pF-70 pF increases ground noise. Beyond 70 pF, ground noise drops off due to the filtering effect of the load. Moving the load away from the output reduces the ground bounce.
- Location of the output pin: outputs closer to the ground pin exhibit less ground bounce than those further away.
- Voltage: lowering V_{CC} reduces ground bounce.
- Test fixtures: standard test fixtures generate 30% to 50% more ground bounce than a typical system since they use capacitive loads which both increase the AC load and form LCR tank circuits that oscillate.



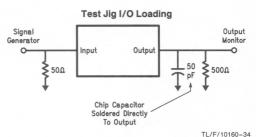
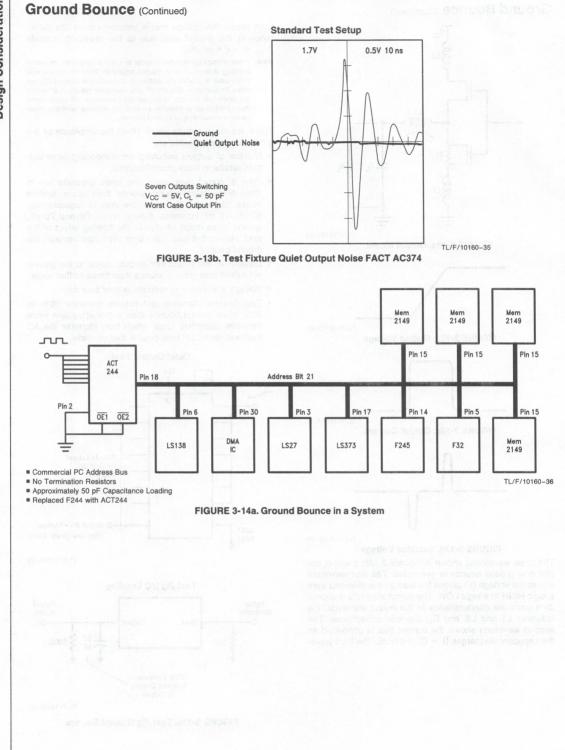


FIGURE 3-13a. Test Jig Ground Bounce



Ground Bounce (Continued)

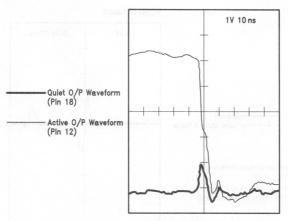


FIGURE 3-14b. System Ground Bounce

TL/F/10160-37

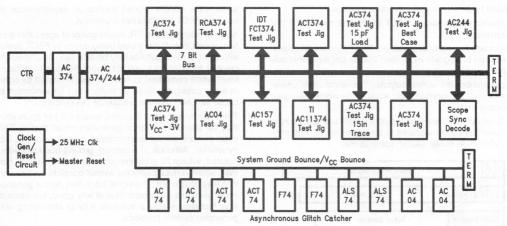


FIGURE 3-15a. Ground Bounce Demo Board Block Diagram

Ground Bounce (Continued)

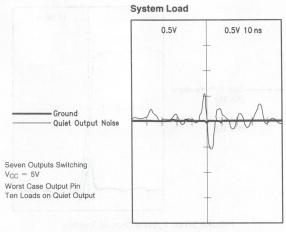
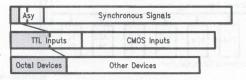


Figure 3-15b. System Quiet Output Noise FACT AC244

TL/F/10160-39

Ground bounce produces several symptoms:

- Altered device states. FACT logic does not exhibit this symptom.
- Propagation delay degradation. FACT devices are specified not to degrade more than 250 ps per additional output switching.
- Undershoot on active outputs. The worst-case undershoot will be approximately equal to the worst-case quiet output noise.
- Quiet output noise. FACT logic's worst-case quiet output noise has been measured to be approximately 500 mV– 1100 mV in actual system applications.



TL/F/10160-40

Use caution when using FACT octals to drive asynchronous signals into TTL level inputs.

FIGURE 3-16. Design Recommendation

Looking at the entire spectrum of logic applications, we can break them up into two distinct categories: Synchronous Signals and Asynchronous Signals. Only asynchronous signals could be affected because device generated noise is concurrent with active edges and is within the device's specified maximum propagation delay. These signals include Clock Pulses, Resets, Presets, Write Enable, etc. Asynchronous signals typically represent only about 10% of the overall spectrum of applications.

These asynchronous signal applications may be broken into two categories: TTL Input Thresholds and CMOS Input Thresholds. FACT inputs typically switch at 3.0V, for a 2.0 ns pulse width, and TTL inputs will switch at 1.7V (FAST and ALS), for the same pulse width. Because of this addi-

tional noise margin, ground bounce on asynchronous signals into FACT inputs is not a concern.

Again breaking up the TTL inputs group of applications into two groups, only those inputs being driven by FACT devices with eight or more outputs may be affected. Ground bounce created by 6 or less outputs switching simultaneously is small when compared to noise levels generated by octals. In many cases, the need for buffers can be eliminated because all FACT devices feature 24 mA outputs.

Therefore only a small segment (about 5%) of applications may be affected by device generated noise, that is, FACT octal devices driving asynchronous signals into TTL input thresholds. Although in a system, ground bounce levels, if isolated, will not be great enough to switch TTL inputs. However, when summed with the overall possible system noise that may couple onto the signal trace line, device generated noise becomes a concern. That is why good, low noise design techniques play a valuable role in eliminating noise generated system problems.

Observing either one of the following rules is sufficient to avoid running into any of the problems associated with ground bounce:

First, use caution when driving asynchronous TTL-level inputs from CMOS octal outputs, or Second, use caution when running control lines (set, reset, load, clock, chip select) which are glitch-sensitive through the same devices that drive data or address lines.

When it is not possible to avoid the above conditions, there are simple precautions available which can minimize ground bounce noise. These are:

- Locate these outputs as close to the ground pin as possible.
- Use the lowest V_{CC} possible or separate the power supplies.
- Use board design practices which reduce any additive noise sources, such as crosstalk, reflections, etc.

Design Rules

The set of design rules listed below is recommended to ensure reliable system operation by providing the optimum power supply connection to the devices. Most designers will recognize these guidelines as those they have employed with advanced bipolar logic families.

- Use multi-layer boards with V_{CC} and ground planes, with the device power pins soldered directly to the planes to insure the lowest power line impedances possible.
- Use decoupling capacitors for every device, usually 0.10 μ F should be adequate. These capacitors should be located as close to the ground pin as possible.
- Do not use sockets or wirewrap boards whenever possiblo
- Do not connect capacitors from the outputs directly to ground.

Decoupling Requirements

National Semiconductor Advanced CMOS, as with other high-performance, high-drive logic families, has special decoupling and printed circuit board layout requirements. Adhering to these requirements will ensure the maximum advantages are gained with FACT products.

Local high frequency decoupling is required to supply power to the chip when it is transitioning from a LOW to HIGH value. This power is necessary to charge the load capacitance or drive a line impedance. *Figure 3-18* displays various V_{CC} and ground layout schemes along with associated impedances.

For most power distribution networks, the typical impedance is between 50Ω and $100\Omega.$ This impedance appears in series with the load impedance and will cause a droop in the V_{CC} at the part. This limits the available voltage swing at the local node, unless some form of decoupling is used. This drooping of rails will cause the rise and fall times to become elongated. Consider the example described in Figure 3-19 to calculate the amount of decoupling necessary. This circuit utilizes an 'AC240 driving a 100Ω bus from a point somewhere in the middle.

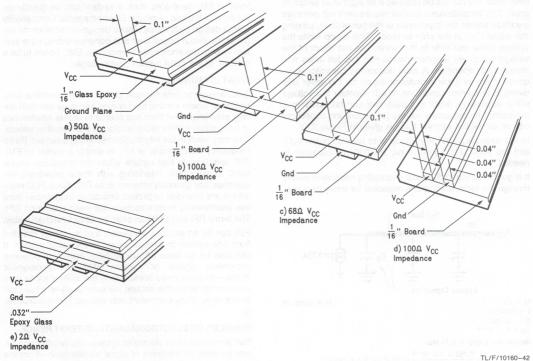


FIGURE 3-18. Power Distribution Impedances

3

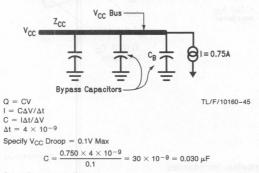
Decoupling Requirements (Continued) Buffer Output Sees Net 50Ω Load. 50Ω Load Line on IOH-VOH Data Bus Characteristic. Shows Low-to-High Step of Approx. 4.8V. 100Ω 4.9V VOUT Buffer 0.1 Ground Plane 1 of 8 94 mA OH 100Ω TL/F/10160-44 Worst-Case Octal Drain = 8 × 94 mA = 0.75 AmpTL/F/10160-43

FIGURE 3-19. Octal Buffer Driving a 100 $\!\Omega$ Bus

Being in the middle of the bus, the driver will see two 100Ω loads in parallel, or an effective impedance of 50Ω . To switch the line from rail to rail, a drive of 94 mA is needed; more than 750 mA will be required if all eight lines switch at once. This instantaneous current requirement will generate a voltage across the impedance of the power lines, causing the actual $V_{\rm CC}$ at the chip to droop. This droop limits the voltage swing available to the driver. The net effect of the voltage droop will lengthen device rise and fall times and slow system operation. A local decoupling capacitor is required to act as a low impedance supply for the driver chip during high current conditions. It will maintain the voltage within acceptable limits and keep rise and fall times to a minimum. The necessary values for decoupling capacitors can be calculated with the formula given in Figure 3-20.

In this example, if the V_{CC} droop is to be kept below 0.1V and the edge rate equals 4 ns, a 0.030 μF capacitor is needed.

It is good practice to distribute decoupling capacitors evenly through the logic, placing one capacitor for every package.



Select $C_B \ge 0.047 \ \mu F$

Place one decoupling capacitor adjacent to each package driving any transmission line and distribute others evenly throughout the logic. One capacitor per three packages.

FIGURE 3-20. Formula for Calculating Decoupling Capacitors

Capacitor Types

Decoupling capacitors need to be of the high K ceramic type with low equivalent series resistance (ESR), consisting primarily of series inductance and series resistance. Capacitors using 5ZU dielectric have suitable properties and make a good choice for decoupling capacitors; they offer minimum cost and effective performance.

Electromagnetic Interference

One of the features of advanced CMOS is its fast output edge rates. For the first time a non-ECL logic family is capable of switching outputs at ECL speeds. In fact, advanced CMOS edge rates exceed that of ECL. ECL outputs typically swing 900 mV in 700 ps, translating into an edge rate of 1.3 V/ns. Advanced CMOS outputs, on the other hand, swing 5.0V in approximately 3.0 ns, translating into an edge rate of 1.6 V/ns. Logic families driving at these speeds, however, are more prone to generate higher levels of system noise. Electronic systems using advanced CMOS logic, as with any other high performance logic system, require a higher level of design considerations.

One element of system noise that will be discussed here is referred to as Electromagnetic Interference, or EMI. The level of EMI generated from a system can be greatly reduced with the use of proper Electromagnetic Compatibility (EMC) design techniques. These design considerations begin at the circuit board level and continue through the system level to the enclosures themselves; EMC needs to be a concern at the initial system design stage.

WHAT IS EMI/RFI?

Electromagnetic Interference, or EMI, is an electrical phenomenon where electric field energy and magnetic field energy are transmitted from one source to create interference of transmitted and/or received signals from another source. This may result in the information becoming distorted. Radio Frequency Interference, or RFI, is simply a subset of EMI. EMI components that radiate within the broadcast broadband, consequently interfering with these broadcast frequencies, are generally referred to as RFI. Since FCC regulations are intended to protect broadcast frequencies from this interference, most emphasis has been placed on RFI. The terms RFI and EMI can often be used interchangeably. EMI can be an issue of emissions, that is, energy radiated from one system to another or within the same system. It can also be an issue of susceptibility, from high powered microwave signals or nuclear EMP (Electromagnetic Pulse)—an issue more applicable in the military arena than commercial. While this section will specifically address radiated energy, many comments may also apply to susceptibili-

SOURCES OF ELECTROMAGNETIC INTERFERENCE

EMI generation in an electronic system may result from several sources. All mediums of signal transmission—from the signal origin to its destination—are possible sources of radiated EMI. Understanding how each medium—including ICs, coaxial cables, and connectors—can radiate EMI is paramount in effective, high performance system design.

Electromagnetic Interference (Continued)

As Figure 3-21 illustrates, EMI in a typical electronic circuit is generated by a current flowing in a loop configured within the circuit. These paths can be either V_{CC}-to-GND loops or output-to-GND loops. The propagating current pulse creates magnetic field energy, while the voltage drop across the loop area creates electric field energy. The loop material inself acts as an antenna radiating—or receiving—both the electric and magnetic fields.

EMI generation is a function of several factors. Transmitted signal frequency, duty cycle, edge rate, and output voltage swings are the major factors of the resultant EMI levels. Figure 3-22 illustrates a generalized Fourier transformation of the transmitted signal from the time domain to the frequency domain. To think in terms of EMI, one must think in terms of the frequency domain. This illustration helps to realize the role of the time domain signal components in the frequency domain. Notice that as the signal's period decreases, duty cycle decreases, or rise/fall time decreases that the radiated bandwidth increases.

On the circuit level, in addition to the signal component factors mentioned earlier, radiating loop area, and the resultant antenna's radiating efficiency also play an important role in EMI generation. Also, current spikes, power line noise, and output ringing caused by outputs switching also contribute to the overall EMI. Good design techniques that moderate this noise will play a major role in minimizing radiated EMI.

OVERALL SYSTEM EMI

System EMI is a function of the current loop area. Some of the largest loop areas in a system consist of circuit board signal transmission lines, backplane transmission lines, and I/O cables. The current loop areas of the integrated circuit packages—V_{CC}-to-GND loops—are small in comparison to those of the transmission lines and I/O cables. Differences in IC package pinout schemes are much less noticeable in terms of overall system radiated EMI.

Figures 3-23a and 3-23b illustrate results from an EMI radiation predication model of logic ICs with standard (corner V_{CC} and GND) pinout and non-standard (central V_{CC} and GND) pinout, respectively. The V_{CC} -to-GND loop was analyzed. The formula used to model the maximum electric field is listed below. This formula takes into account the antenna dimension and efficiency as well as the basic signal components

$$|\mathsf{E}|_{\mathsf{Max}} = \frac{1.32 \times 10^{-3} \bullet ! \bullet A \bullet \mathsf{Freq}^2}{\mathsf{D}} \left[1 + \left(\frac{\lambda}{2} \, \pi \mathsf{D} \right)^2 \, \right]^{\frac{1}{2}} \frac{\mu \mathsf{V}}{\mathsf{m}}$$

where,

|E|Max is the maximum E-field in the plane of the loop

I is the current amplitude in milliamps

A is the loop area in square cm

 λ is the wavelength at the frequency of interest

D is the observation distance in meters

Freg is the frequency in MHz

and the perimeter of the loop $P \ll \lambda$.

Figure 3-23c illustrates the predicted radiation from signals propagating on eight typical PCB transmission lines. Note the difference in the levels of radiated EMI between the IC packages and the signal traces. The difference between package pinout becomes negligible.

CIRCUIT BOARD DESIGN CONSIDERATIONS

Original equipment manufacturers cannot afford to fail electromagnetic emissions tests. Since these tests are measured outside of the system, precautions to shield the enclosures, I/O cables, and connections are paramount. However, EMI within a system may also cause errors in data transmission or unreliable system operation. Therefore, good EMC design techniques at the circuit board level are just as necessary.

Designing a system free of all EMI is an overwhelming task. However, considering the following design recommendations at the circuit board level forms a good foundation on which to design a system with good EMC.

- The use of multilayer printed circuit board is a virtual necessity. Two-sided printed circuit board and wire-wrap boards provide no shielding of EMI. Two-sided boards also do not allow the use of power and ground planes. Instead they require the use of high impedance power and ground traces. Planes provide impedances several orders of magnitude lower than that of traces, reducing transient voltage drops in the power distribution and return loops. As a result of these lower voltage drops, power supply induced EMI can also be reduced.
- In addition to the reduced impedance, these power and ground planes have an inherent EMI shielding effect that the large areas of copper provide. With the use of striplines or signal transmission lines sandwiched between the power and ground planes, the designer can take full advantage of the planes' shielding capabilities. To maximize this shielding effect, keep the power and ground plane areas as homogeneous as possible.
- Since plastic provides no EMI shielding, and sockets of any profile provide plenty of lead length, ICs should be soldered directly to the board. Solder power and ground pins directly to the power and ground planes, respectively. Minimize the IC and associated component lead lengths wherever possible.
- Minimizing the number of simultaneously switching outputs will also help to moderate the current pulse amplitude and output ringing.
- Terminating signal traces longer than 6 inches (typical) will minimize reflections and ringing due to those reflections.
- Avoid capacitively coupling signals from one transmission line to another—crosstalk—by avoiding long parallel signal transmission lines. If parallel transmission lines are unavailable, maximize the distance between the two lines, or insert a ground trace. Minimizing the spacing between the signal plane and ground plane will also help reduce crosstalk. For more details, see section on Crosstalk.

Electromagnetic Interference (Continued)

POWER SUPPLY DECOUPLING CONSIDERATIONS

Much of a system's radiated EMI may originate from the power supply itself. Propagation of power supply noise throughout a system is a very undersirable situation in any respect, including EMI. Suppression of this power supply noise is highly recommended. Decoupling the power supply at every level, from the system supply distribution network, down to the individual IC, is also a necessity when designing for low noise—and low EMI.

- On the system level, the use of a tantalum or aluminum electrolytic capacitor in the power supply distribution network is recommended.
- Decoupling the power supply at the point of entry onto the printed circuit board is also highly recommended. The use of a low equivalent series inductance, or ESL, multilayer ceramic capacitor, 1.0 μF to 10.0 μF , provides good low to medium frequency filtering and EMI suppression.
- To further suppress power supply noise and associated EMI throughout the circuit board itself, the use of a low ESL chip capacitor for each IC is highly recommended. Because the location of any transient noise on a power or ground plane would be impossible to predict, and the IC density of different circuit boards vary dramatically, every IC on these circuit boards should be adequately decoupled. A 0.10 μF to 0.01 μF chip capacitor, located as close to each ground pin as possible, will provide good high frequency power supply noise filtering and added EMI suppression.

BACKPLANE CONSIDERATIONS

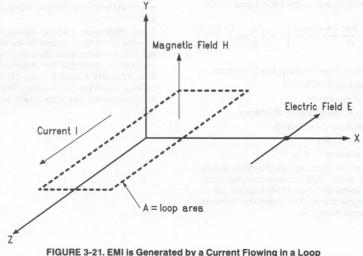
The above discussion emphasized design techniques for printed circuit boards. However, because the backplane may, and usually does, consist of several long signal transmission lines, the same low noise design techniques should be used.

 Multilayer board techniques should also be applied to the backplane. If possible, these transmission lines should be shielded individually. This would allow for a denser parallel layout of transmission lines as well as providing good EMC. Use multiple ground and power connections from the backplane to the circuit boards' power and ground planes to minimize the connection impedance. This will help to further suppress any source of power supply generated EMI.

SYSTEM CONSIDERATIONS

One of the major sources of radiated system EMI are the edge connectors, I/O cables, and their associated connectors

- Use care to ensure that, not only the cables are shielded and the shield properly grounded, but that the shield totally envelopes both the cable and its connectors. The shield should seat firmly into a grounded chassis and touch the chassis a full 360° around the connection. An open ended cable or an improperly grounded connector shield will be a prime suspect for out-of-spec EMI emissions and should be avoided. Use shielded coaxial cables whenever possible. If ribbon cable is preferred, shield all ribbon cables with commercially available ribbon cable shielding. Again, ensure that this shield is properly attached to the connector shield by a full 360°.
- In choosing or designing the enclosure for the system, minimize the number of openings in the enclosure. Since high performance logic now deals with smaller wavelengths than the older technologies, enclosure opening sizes should also be considered. Keep openings as small as possible. If openings are necessary (displays, controls, fans, etc.) there are commercially available accessories that offer good built-in EMI shielding.
- If access panels are necessary, ensure that these panels are properly sealed with some sort of shielding material (gaskets, copper brushes, etc.).
- Of course, the enclosure itself should be of a material that provides good shielding against electric fields.



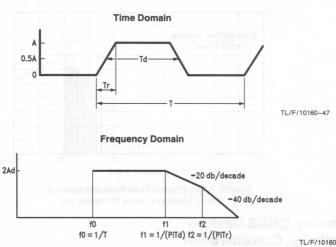


FIGURE 3-22. Output Characteristics

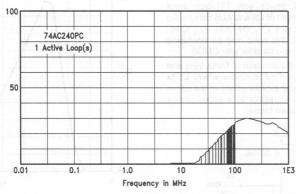


FIGURE 3-23a. Electric Field Radiation in $dB\mu V/m$ from 1 Loop(s) of Area 0.6 square cm

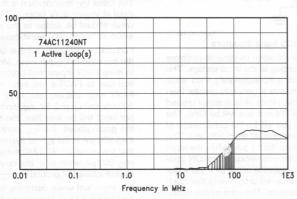


FIGURE 3-23b. Electric Field Radiation in $dB\mu V/m$ from 1 Loop(s) of Area 0.19 square cm

TL/F/10160-49

Electromagnetic Interference (Continued)

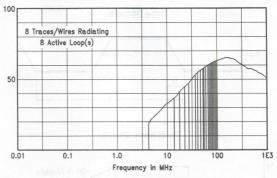


FIGURE 3-23c. Electric Field Radiation in $dB\mu V/m$ from 8 Loop(s) of Area 10 square cm

TL/F/10160-51

TTL-Compatible CMOS Designs Require Delta I_{CC} Consideration

The FACT product line is comprised of two types of advanced CMOS circuits: 'AC and 'ACT devices. 'ACT indicates an advanced CMOS device with TTL-type input thresholds for direct replacement of LS and ALS circuits. As this 'ACT series is used to replace TTL, the Delta I_{CCT} specification must be considered; this spec may be confusing and misleading to the engineer unfamiliar with CMOS.

It is important to understand the concept of Delta I_{CCT} and how to use it within a design. First, consider where Delta I_{CCT} initiates. Most CMOS input structures are of the totem pole type with an n-channel transistor in a series with a p-channel transistor as illustrated below.

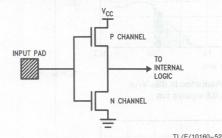


FIGURE 3-24. CMOS Input Structure

These two transistors can be modeled as variable resistors with resistances varying according to the input voltage. The resistance of an ON transistor is approximately 4 k Ω while the resistance of an OFF transistor is generally greater than 500 M Ω . When the input to this structure is at either ground or V_{CC}, one transistor will be ON and one will be OFF. The total series resistance of this pair will be the combination of the two individual resistances, greater than 500 M Ω . The leakage current will then be less than 1 µA. When the input is between ground and V_{CC}, the resistance of the ON transistor will increase while the resistance of the OFF transistor will decrease. The net resistance will drop due to the much larger value of the OFF resistance. The total series resistance can be as low as 600Ω . This reduction in series resistance of the input structure will cause a corresponding increase in I_{CC} as current flows through the input structure. The following graph depicts typical I_{CC} variance with input voltage for an 'ACT device.

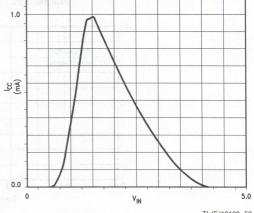


FIGURE 3-25. I_{CC} versus Input Voltage for 'ACT Devices

The Delta I_{CC} specification is the increase in I_{CC} . For each input at $V_{CC} = 2.1V$ (approx. TTL V_{OH} level), the Delta I_{CC} value should be added to the quiescent supply current to

arrive at the circuit's worst-case static I_{CC} value.

device instead of ground or VCC.

Fortunately, there are several factors which tend to reduce the increase in $I_{\rm CC}$ per input. Most TTL devices will be able to drive FACT inputs well beyond the TTL output specification due to FACT's low input loading in a typical system. FAST logic outputs can drive 'ACT-type inputs down to 200 mV and up to 3.5V. Additionally, the typical $I_{\rm CC}$ increase per input will be less than the specified limit. As shown in the graph above, the $I_{\rm CC}$ increase at $V_{\rm CC}-2.1V$ is less than 200 $\mu{\rm A}$ in the typical system. Experiments have shown that the $I_{\rm CC}$ of an 'ACT240 series device typically increases only 200 $\mu{\rm A}$ when all of the inputs are connected to a FAST

It is important when designing with FACT, as with any TTL-compatible CMOS technology, that the Delta I_{CC} specification be considered. Designers should be aware of the spec's significance and that the data book specification is a worst-case value; most systems will see values that are much less.

3

Testing Advanced CMOS Devices with I/O Pins

There are more and more CMOS families becoming available which can replace TTL circuits. Although testing these new CMOS units with programs and fixtures which were developed for bipolar devices will yield acceptable results most of the time, there are some cases where this approach will cause the test engineer problems.

Such is the case with parts that have a bidirectional pin, exemplified by the '245 Octal Transceiver. If the proper testing methods are not followed, these types of parts may not pass those tests for I_{CC} and input leakage currents, even when there is no fault with the devices.

CMOS circuits, unlike their bipolar counterparts, have static $I_{\rm CC}$ specification orders of magnitude less than standard load currents. Most CMOS $I_{\rm CC}$ specifications are usually less than 100 $\mu{\rm A}.$ When conducting an $I_{\rm CC}$ test, greater care must be taken so that other currents will not mask the actual $I_{\rm CC}$ of the device. These currents are usually sourced from the inputs and outputs.

Since the static I_{CC} requirements of CMOS devices are so low, output load currents must be prevented from masking the current load of the device during an I_{CC} test. Even a standard 500Ω load resistor will sink 10 mA at 5V, which is more than twice the I_{CC} level being tested. Thus, most manufacturers will specify that all outputs must be unloaded during I_{CC} tests.

Another area of concern is identified when considering the inputs of the device. When the input is in the transition region, $I_{\rm CC}$ can be several orders of magnitude greater than the specification. When the input voltage is in the transition region, both the n-channel and the p-channel transistors in the input totem-pole structure will be slightly ON, and a conduction is created from $V_{\rm CC}$ to ground. This conduction path leads to the increased $I_{\rm CC}$ current seen in the $I_{\rm CC}$ vs $V_{\rm IN}$ curve. When the input is at either rail, the input structure no longer conducts. Most $I_{\rm CC}$ testing is done with all of the inputs tied to either $V_{\rm CC}$ or ground. If the inputs are allowed to float, they will typically float to the middle of the transition region, and the input structure will conduct an order of magnitude more current than the actual $I_{\rm CC}$ of the device under test which is being measured by the tester.

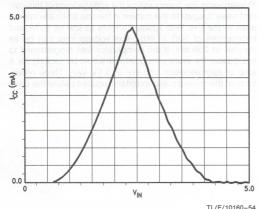
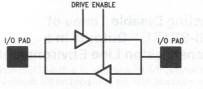


FIGURE 3-26. I_{CC} versus I_{IN}

When testing the I_{CC} of a CMOS '245, problems can arise depending upon how the test is conducted. Note the structure of the '245's I/O pins illustrated below.



TL/F/10160-55

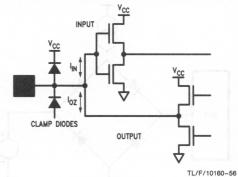
FIGURE 3-27. '245 I/O Structure

Each I/O pin is connected to both an input device and an output device. The pin can be viewed as having three states: input, output and output disabled. However, only two states actually exist.

The pin is either an input or an output. When testing the I_{CC} of the device, the pins selected as outputs by the T/R signal must either be enabled and left open or be disabled and tied to either rail. If the output device is disabled and allowed to float, the input device will also float, and an excessive amount of current will flow from V_{CC} to ground. A simple rule to follow is to treat any output which is disabled as an input. This will help insure the integrity of an I_{CC} test.

Another area which might precipitate problems is the measurement of the leakages on I/O pins. The I/O pin internal structure is depicted below.

The pin is internally connected to both an input device and an output device; the limit for a leakage test must be the combined I_{IN} specification of the input and the I_{OZ} specification of the output. This combined leakage test is defined as IOZ_T. For FACT devices, I_{IN} is specified at $\pm 1~\mu \text{A}$ while I_{OZ} is specified at $\pm 5~\mu \text{A}$. Combining these gives a limit of $\pm 6~\mu \text{A}$ for I/O pins. Usually, I/O pins will show leakages that are less than the I_{OZ} specification of the output alone.



11/7/10/00-50

FIGURE 3-28. I/O Pin Internal Structure

Testing CMOS circuits is no more difficult than testing their bipolar counterparts. However, there are some areas of concern that will be new to many test engineers beginning

Testing Advanced CMOS Devices with I/O Pins (Continued)

to work with CMOS. Becoming familiar with and understanding these areas of concern prior to creating a test philosophy will avert many problems that might otherwise arise later.

Testing Disable Times of TRI-STATE® Outputs in a Transmission Line Environment

Traditionally, the disable time of a TRI-STATE buffer has been measured from the 50% point on the disable input, to the ($V_{OL}+0.3V$) or ($V_{OH}-0.3V$) point on the output. On a bench test site, the output waveform is generated by a load capacitor and a pull-up/pull-down resistor. This circuit gives an RC charge/discharge curve as shown below.

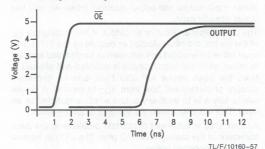


FIGURE 3-29. Typical Bench TRI-STATE Waveform

ATE test sites generally are unable to duplicate the bench test structure. ATE test loads differ because they are usually programmable and are situated away from the actual device. A commonly used test load is a Wheatstone bridge. The following figure illustrates the Wheatstone bridge test structure when used on the MCT 2000 test-system to duplicate the bench load.

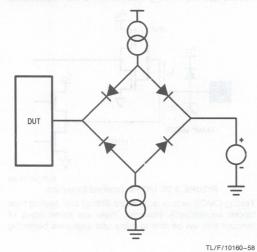
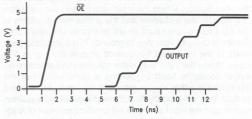


FIGURE 3-30. MCT Wheatstone Bridge Test Load

The voltage source provides a pull-up/pull-down voltage while the current sources provide I_{OH} and I_{OL} . When devices with slow output slew rates are tested with the ATE load, the resultant waveforms closely approximate the bench waveform, and a high degree of correlation can be achieved. However, when devices with high output slew rates are tested, different results are observed that make correlating tester results with bench results more difficult. This difference is due to the transmission line properties of the test equipment. Most disable tests are preceded by establishing a current flow through the output structure. Typically, these currents will be between 5 mA and 20 mA. The device is then disabled, and a comparator detects when the output has risen to the $(\mathsf{V}_{\mathsf{OH}} - 0.3\mathsf{V})$ level or fallen to the $(\mathsf{V}_{\mathsf{OH}} - 0.3\mathsf{V})$ level.

Consider the situation where the connection between the device under test (DUT) and the comparator is a transmission line. Visualize the device output as a switch; the effect is easier to see. There is current flowing through the line, and then the switch is opened. At the device end, the reflection coefficient changes from 0 to 1. This generates a current edge flowing back down the line equal to the current flowing in the line prior to the opening of the switch. This current wave will propagate down the line where it will encounter the high impedance tester load. This will cause the wave to be reflected back down the line toward the DUT. The current wave will continue to reflect in the transmission line until it reaches the voltage applied to the tester load. At this point, the current source impedance decreases and it will dissipate the current. A typical waveshape on a modern ATE is depicted in Figure 3-31.



TL/F/10160-59

FIGURE 3-31. Typical ATE TRI-STATE Waveform

Transmission line theory states the voltage level of this current wave is equal to the current in the line times the impedance of the line. With typical currents as low as 5 mA and impedances of 50Ω to 60Ω , this voltage step can be as minimal as 250 mV. If the comparator was programmed to the disable measurement points, it would be looking for a step of approximately 575 mV at 5.5 V V $_{CC}$. Three reflections of the current pulse would be required before the com-

Testing Disable Times of TRI-STATE Outputs in a Transmission Line Environment (Continued)

parator would detect the level. It is this added delay time caused by the transmission line environment of the ATE that may cause parts to fail customer's incoming tests, even though the device meets specifications. The figure below graphically shows this stepout.

Point A represents the typical 50% measurement point on tester driven waveforms. Point B represents the point at which the delay time would be measured on a bench test fixture. Point C represents where the delay time could be measured on ATE fixtures. The delay time measured on the ATE fixture can vary from the bench measured delay time to some greater value, depending upon the voltage level that the tester is set. If the voltage level of the tester is close to voltage levels of the plateaus, the results may become nonrepeatable.

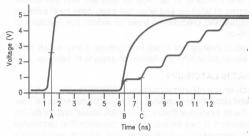


FIGURE 3-32. Measurement Stepout

Understanding Latch-Up in Advanced CMOS Logic

National Semiconductor Application Note 600



Latch-up has long been a bane to CMOS IC applications; its occurence and theory have been the subjects of numerous studies and articles. The applications engineer and systems designer, however, are not so much concerned with the theory and modeling of latch-up as they are with the consequences of latch-up and what has been done by the device designer and process engineer to render ICs resistant to latch-up.

Of equal interest are those precautions, if any, which must be observed to limit the liability of designs to latch-up.

WHAT IS LATCH-UP?

Latch-up is a failure mechanism of CMOS (and bipolar) integrated circuits characterized by excessive current drain coupled with functional failure, parametric failure and/or device destruction. It may be a temporary condition that terminates upon removal of the exciting stimulus, a catastrophic condition that requires the shutdown of the system to clear or a fatal condition that requires replacement of damaged parts. Regardless of the severity of the condition, latch-up is an undesirable but controllable phenomenon. In many cases, latch-up is avoidable.

The cause of the latch-up exists in all junction-isolated or bulk CMOS processes: parasitic PNPN paths. Figure 1, a basic CMOS cross section, shows the parasitic NPN and PNP bipolar transistors which most frequently participate in latch-up. The P+ sources and drains of the P-channel MOS devices act as the emitters (and sometimes collectors) of lateral PNP devices: the N-substrate is the base of this device and collector of a vertical NPN device. The P-well acts as the collector of the PNP and the base of the NPN. Finally, the N+ sources and drains of the N-channel MOS devices serve as the emitter of the NPN. The substrate is normally connected to V_{CC}, the most positive circuit voltage, via an N+ diffusion tap while the P-well is terminated at Gnd, the most negative circuit voltage, through a P+ diffusion. These power supply connections involve bulk or spreading resistance to all points of the substrate and P-well.

Normally, only a small leakage current flows between the substrate and P-well causing only a minute bias to be built up across the bulk due to the resistivity of the material. In

this case the depletion layer formed around the reverse-biased PN junction between P-well and the substrate supports the majority of the V_{CC}-Gnd voltage drop. As long as the MOS source and drain junctions remain reverse-biased, CMOS is well behaved. In the presence of intense ionizing radiation, thermal or over-voltage stress, however, current can be injected into the PNP emitter-base junction, forwardbiasing it and causing current to flow through the substrate and into the P-well. At this point, the NPN device turns on. increasing the base drive to the PNP. The circuit next enters a regenerative phase and begins to draw significant current from the external network thus causing most of the undesirable consequences of latch-up. Once established, a latchup site, through the fields generated by the currents being conducted, may trigger similar action in both elements of the IC.

WHAT TO DO

As might be expected, latch-up is highly dependent on the characteristics of the bipolar devices involved in the latchup loop. Device current gains, emitter efficiencies, minority carrier life times and the degree of NPN-PNP circuit coupling are all important factors relating to both the sensitivity of the particular latch-up device and to the severity of the failure once it has been excited. Layout geometry and process both contribute significantly to these parameters; CMOS, like other technologies, has been shrunk to provide more function per unit area, increasing susceptibility to latch-up. All major CMOS vendors have upgraded their processes and/or design rules to compensate for this increased susceptibility, some with more success than others. The lateral PNP is typically the weak link in the latch-up loop. As such, various devices can be exploited toward reducing the effectiveness of the PNP to participate in latchup. Guard banding, device placement, the installation of pseudo-collectors between the P-channel devices and the P-well, and the use of a low resistivity substrate under an epitaxial layer are a few of the IC design tactics now being practiced to reduce the current gain or to control the action of the lateral PNP structures in state-of-the-art CMOS devic-

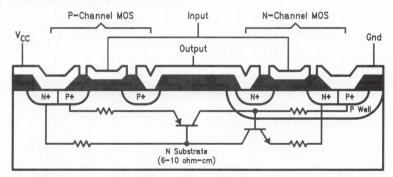


FIGURE 1. Basic CMOS Inverter Cross Section with Latch-Up Circuit Model

TL/F/10192-1

Vendors of CMOS ICs have always been aware of the latch-up phenomenon and have considerably improved their designs and processes to reduce the danger of latch-up occuring under normal usage. Abnormal applications and misuse of CMOS ICs may still pose problems that the CMOS vendor has little control over. Hence, CMOS users must be aware of what they are doing and those measures which must be taken to reduce the susceptibility to latch-up. The use of CMOS at or beyond its rated maximum voltage range and the presence of inductive transients are applications-related situations which can trigger latch-up. Environment, including thermal stress, poorly regulated or noisy supplies and radiation incidence can also contribute to or cause latch-up. The system engineer must consider these situations when using CMOS in designs.

While latch-up is generally recognized as resulting from regenerative switching along a PNPN path, many designers incorrectly assume that this regenerative action places the device in a state that can only be recovered from if the system is powered down. The fact is that there is probably an equal, if not greater, chance that the regenerative switching, when encountered, will be non-sustaining (the condition, more accurately referred to as current amplification, will disappear when the triggering stimulus is removed); over-voltage applied to properly designed input protection networks is one example of controlled current amplification. For sustained latch-up to occur, the regeneration loop must have sufficient gain and the power source must be able to supply a minimum current. From this we can see that current-limited power supplies might be used to recover from or reduce the effects of latch-up. Another method uses current-limiting series resistors in the power connections of offending ICs in conjunction with storage capacitors shunting the devices. Normal switching current will be drawn from the capacitors while DC current will be limited by the resistors. In the loop of positive current feedback formed by the parasitic PNP and NPN transistors of the latch-up structures. regenerative switching may result if sufficient loop gain is available. One must remember, though, that three conditions are necessary for latch-up to occur.

- both parasitic bipolars must be biased into the active state;
- the product of the parasitic bipolar transistor current gains (Bnpn•Bpnp) must be sufficient to allow regeneration, i.e., greater than or equal to one;
- the terminal network must be capable of supplying a current greater than the holding current required by the PNPN path. In processes utilizing an epitaxial silicon, this current is usually in excess of 1A.

If any of these conditions is not met both during the initiation and in the steady state, then the latch-up condition is either non-sustaining or cannot be initiated. If the current to the latched structure is not limited, permanent damage may result. Again, any means to prevent any of these conditions from being satisfied will protect the circuit from exhibiting sustained latch-up.

The prevention of biasing the bipolars into the active region and the limiting of the current which may be supplied by the network are the two factors which system designers have under their control. Many of the protective measures long exercised in discrete and TTL designs may also be applied to CMOS designs to reduce susceptibility and prevent damage to these systems. Diode clamping of inductive loads, signal and supply level regulation, and sharing of large DC loads by several devices with suitable series limiting resis-

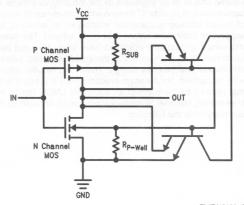
tors to distribute thermal stress over a larger area or multiple ICs are all positive-preventive measures to exploit.

While we have been considering the CMOS device in a generic manner, there are two primary structures used in all CMOS ICs which have latch-up paths associated with them; these are the inverter or gate and the transmission switch. Both structures may be susceptible under the right conditions. While the CMOS inverter can exhibit latch-up independent of circuit configuration, the transmission switch usually has lower holding current, and thus, a lower threshold for latch-up, but is dependent on its external connections for latch-up to occur. Figure 2 shows the lumped equivalent circuit of the inverter. Notice the shunting resistors across the base-emitter junctions of the bipolar transistors: these resistors divert base drive from the bipolars and as a result increase both the trigger current and holding current levels required for the structures to participate in latch-up. A further increase in these current levels can be achieved by further decreasing the shunt resistance. Diffusing all active components into an epitaxial silicon, under which would lie a substrate of substantially less resistivity, will have a dramatic effect on decreasing the shunt resistance, therefore increasing the trigger current and holding current levels required for latch-up.

THE CIRCUIT CONNECTION

As we have seen above, the external circuit connections are regular participants in the latch-up process. The current for latch-up comes from these connections and often the triggering mechanism is external to the latching device. All three classes of external connections (power, input and output) are important in latch-up. We will now look at how these connections relate to this process.

Current injection through the power terminals when the power supply voltage is beyond the maximum rated for the CMOS device can directly cause latch-up through base collector leakage or breakdown mechanisms. One aspect of high power supply voltages that is not often recognized is the effect of field-aiding lateral currents under the emitters of the PNP devices. This can effect a significant increase in the beta of these devices, making internally trigger latch-up much more prevalent. Again, the warning to the the system designer is to avoid using CMOS at maximum rated supply voltages unless precautions are taken to insure latch-up is unlikely or is at least acceptable and recoverable. Switching transients coupled onto power lines has become a problem



TL/F/10192-2

FIGURE 2. CMOS Inverter with Parasitic Bipolars

now that CMOS has become a high-speed logic technology. Attention to power supply decoupling is now a necessity when designing with high-speed CMOS. Of course, CMOS processes incorporating an epitaxial silicon over a substrate of very low resistivity is less prone to latch-up under these conditions. These recommended precautions should be taken just the same.

Latch-up involving input terminals, next to gate oxide rupture, used to be one of the most common failure mechanisms of CMOS. Transients exceeding the power supply routinely caused either or both of these effects to occur. Fortunately, CMOS vendors have learned to make better input protection networks and have learned that proper placement of these components with respect to the rest of the chip circuitry is necessary to reduce susceptibility to latch-up. The system designer should review foreign input signals to CMOS systems and take precautions necessary to limit the severity of over/undershoot from these sources. Measures which could be used to reduce the possibility of latch-up induced by input signals are: proper termination of transmission lines driving CMOS, series current limiting resistors. AC coupling with DC restoration to the CMOS supplies, and the addition of Schottky diode clamps to the CMOS power rails. As an additional measure there are several CMOS circuits which have input protection networks that can handle overvoltage in one direction or the other and which are specifically designed to act as interface circuits between other logic families and CMOS. Judicious application of these will also aid in suppressing any tendencies of CMOS systems to latch-up.

Finally, attention to CMOS outputs, their loading and the stresses applied to them will also enable the designer to generate latch-up free systems. Historically, output terminals of CMOS have been least likely to cause latch-up though they can participate in latch-up once it is initiated. The normal mode of failure in this respect is, again, the application of voltages beyond the CMOS supplies or the maximum limit for the devices though excessive current has also been linked to latch-up failure at elevated temperatures. Inductive surges and transmission line reflections are the most likely sources of output latch-up in CMOS and should be attended to in the most applicable method, i.e., by clamping, termination or through dissipative measures.

WHAT WE HAVE DONE

National Semiconductor, as an important supplier of advanced CMOS to all segments of the industry, has made a commitment to provide IC designs which make use of state-of-the-art latch-up suppression techniques in an effort to support its customers before they need support. The three most important actions which we have taken to guard our customers from latch-up are in the areas of layout, power distribution and process design. These techniques, along with recognized good design practice, yield a product line that lives up to the intent of an advanced CMOS family. In brief review, National Semiconductor's attack on latch-up is summarized in the following.

Latch-Up Protection Geometries

Every FACTTM IC employs special geometries to isolate every input protection device and every output from active areas on the chip. In this way, structures which would normally participate in latch-up loops are decoupled and are thus less troublesome. All devices are scrutinized for potential latch-up sites and are protected by similar geometries where any risk is significant.

Power Distribution

Careful attention to on-chip power distribution and enhanced termination of P-wells and substrate is used by National Semiconductor to improve latch-up resistance. Our double metal process affords the advantage in maintaining low impedance distribution of power and ground potentials over the entire chip; the potential gradient-caused fields which often induce or enhance latch-up are thus minimized while functional performance is enhanced by cleaner on-chip power supplies.

Process Design

By design, the FACT process is better both in low latch-up susceptibility and in enhanced device performance. The most significant advancement of the FACT process has been the incorporation of an epitaxial silicon layer. Figure 3 illustrates a modified version of Figure 1, utilizing an epitaxial layer of silicon to contain all of the active components of the CMOS circuit. This epitaxial layer allows the use of a separate layer of substrate silicon, of a resistivity some three orders of magnitude lower than the epitaxial layer. The effect is also modeled in Figure 3.

As illustrated, the resistivity of the epitaxial silicon, R_1 , is on the order of 6 ohm-cm to 10 ohm-cm. The underlying substrate resistivity, R_2 , is as low as 0.008 ohm-cm to 0.025 ohm-cm. The result is a parallel combination of resistivities, R_1 and R_2 , that is equivalent to R_2 . What has now happened is that the gain of the parasitic PNP-NPN circuit has been dramatically slashed. Under the same latch-up conditions described earlier, the introduction of the low resistivity substrate now means that at least 10 times more current is needed to trigger the parasitic PNP-NPN combination.

The active components within the epitaxial layer maintain the same performance characteristics as those of the active area illustrated in the non-epitaxial CMOS circuit of *Figure 1*. Therefore the introduction of the epitaxial layer to the FACT process does not reduce any AC, DC, functional or ESD performance. However, what we have is an advanced CMOS logic family that is now virtually latch-up immune.

Thus, through innovative and careful layout, attention to eliminating circuit situations which could be latch-up prone and by careful selection and maintenance of our advanced CMOS process, FACT sets the standard for latch-up resistance.

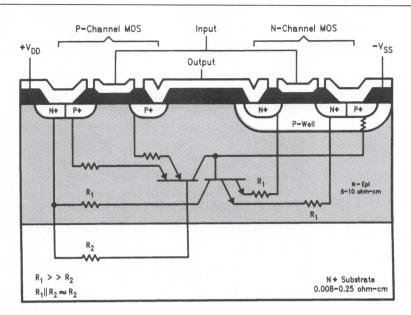


FIGURE 3

TL/F/10192-3



E-S910193-3

ENBBRE



Section 4 Advanced CMOS Datasheets



Section 4 Contents

| 54AC/74AC00 Quad 2-Input NAND Gate | 4-5 |
|--|-------|
| 54ACT/74ACT00 Quad 2-Input NAND Gate | 4-5 |
| 54AC/74AC02 Quad 2-Input NOR Gate | 4-9 |
| 54AC/74AC04 Hex Inverter | 4-12 |
| 54ACT/74ACT04 Hex Inverter | 4-12 |
| 54AC/74AC08 Quad 2-Input AND Gate | 4-15 |
| 54ACT/74ACT08 Quad 2-Input AND Gate | 4-15 |
| 54AC/74AC10 Triple 3-Input NAND Gate | 4-18 |
| 54AC/74AC11 Triple 3-Input AND Gate | 4-21 |
| 54AC/74AC14 Hex Inverter with Schmitt Trigger Input | 4-24 |
| 54ACT/74ACT14 Hex Inverter with Schmitt Trigger Input. | 4-24 |
| | |
| 54AC/74AC20 Dual 4-Input NAND Gate | 4-27 |
| 54AC/74AC32 Quad 2-Input OR Gate | 4-30 |
| 54ACT/74ACT32 Quad 2-Input OR Gate | 4-30 |
| 54AC/74AC74 Dual D Positive Edge-Triggered Flip-Flop | 4-33 |
| 54ACT/74ACT74 Dual D Positive Edge-Triggered Flip-Flop | 4-33 |
| 54AC/74AC85 4-Bit Magnitude Comparator | 4-39 |
| 54ACT/74ACT85 4-Bit Magnitude Comparator | 4-39 |
| 54AC/74AC86 Quad 2-Input Exclusive-OR Gate | 4-40 |
| 54AC/74AC109 Dual JK Positive Edge-Triggered Flip-Flop | 4-43 |
| 54ACT/74ACT109 Dual JK Positive Edge-Triggered Flip-Flop | 4-43 |
| 54AC/74AC112 Dual JK Negative Edge-Triggered Flip-Flop | 4-49 |
| 54ACT/74ACT112 Dual JK Negative Edge-Triggered Flip-Flop | 4-49 |
| 54AC/74AC138 1-of-8 Decoder/Demultiplexer | 4-50 |
| 54ACT/74ACT138 1-of-8 Decoder/Demultiplexer | 4-50 |
| 54AC/74AC139 Dual 1-of-4 Decoder/Demultiplexer | 4-57 |
| 54ACT/74ACT139 Dual 1-of-4 Decoder/Demultiplexer | 4-57 |
| 54AC/74AC151 8-Input Multiplexer | 4-62 |
| 54ACT/74ACT151 8-Input Multiplexer | 4-62 |
| 54AC/74AC153 Dual 4-Input Multiplexer | 4-68 |
| 54ACT/74ACT153 Dual 4-Input Multiplexer | 4-68 |
| 54AC/74AC157 Quad 2-Input Multiplexer | 4-73 |
| 54ACT/74ACT157 Quad 2-Input Multiplexer | 4-73 |
| 54AC/74AC158 Quad 2-Input Multiplexer | 4-78 |
| 54ACT/74ACT158 Quad 2-Input Multiplexer | 4-78 |
| 54AC/74AC161 Synchronous Presettable Binary Counter | 4-83 |
| 54ACT/74ACT161 Synchronous Presettable Binary Counter | 4-83 |
| 54AC/74AC163 Synchronous Presettable Binary Counter | 4-91 |
| 54ACT/74ACT163 Synchronous Presettable Binary Counter | 4-91 |
| 54AC/74AC164 Serial-In, Parallel-Out Shift Register | 4-99 |
| 54ACT/74ACT164 Serial-In, Parallel-Out Shift Register | 4-99 |
| 54AC/74AC169 4-Stage Synchronous Bidirectional Counter | 4-100 |
| 54AC/74AC174 Hex D Flip-Flop with Master Reset | |
| 54ACT/74ACT174 Hex D Flip-Flop with Master Reset | 4-105 |
| | 4-105 |
| 54AC/74AC175 Quad D Flip-Flop | 4-111 |
| 54ACT/74ACT175 Quad D Flip-Flop | 4-111 |
| 54ACT/74ACT181 4-Bit Arithmetic Logic Unit | 4-117 |
| 54ACT/74ACT182 Carry Look-Ahead Generator | 4-118 |

| S | Section 4 Contents (Continued) | |
|---|---|---|
| | 54AC/74AC191 Up/Down Counter with Preset and Ripple Clock | 4-119 |
| | 54AC/74AC240 Octal Buffer/Line Driver with TRI-STATE Outputs | 4-126 |
| | 54ACT/74ACT240 Octal Buffer/Line Driver with TRI-STATE Outputs | 4-126 |
| | 54AC/74AC241 Octal Buffer/Line Driver with TRI-STATE Outputs | 4-130 |
| | 54ACT/74ACT241 Octal Buffer/Line Driver with TRI-STATE Outputs | 4-130 |
| | 54AC/74AC244 Octal Buffer/Line Driver with TRI-STATE Outputs | 4-134 |
| | 54ACT/74ACT244 Octal Buffer/Line Driver with TRI-STATE Outputs | 4-134 |
| | 54AC/74AC245 Octal Bidirectional Transceiver with TRI-STATE Inputs/Outputs | 4-138 |
| | 54ACT/74ACT245 Octal Bidirectional Transceiver with TRI-STATE Inputs/Outputs | 4-138 |
| | 54AC/74AC251 8-Input Multiplexer with TRI-STATE Output. | 4-142 |
| | 54ACT/74ACT251 8-Input Multiplexer with TRI-STATE Output | 4-142 |
| | 54AC/74AC253 Dual 4-Input Multiplexer with TRI-STATE Outputs | 4-148 |
| | 54ACT/74ACT253 Dual 4-Input Multiplexer with TRI-STATE Outputs | 4-148 |
| | 54AC/74AC257 Quad 2-Input Multiplexer with TRI-STATE Outputs | 4-140 |
| | 54ACT/74ACT257 Quad 2-Input Multiplexer with TRI-STATE Outputs | 4-154 |
| | | |
| | 54AC/74AC258 Quad 2-Input Multiplexer with TRI-STATE Outputs | 4-159 |
| | 54ACT/74ACT258 Quad 2-Input Multiplexer with TRI-STATE Outputs | 4-159 |
| | 54AC/74AC269 8-Bit Bidirectional Binary Counter | 4-164 |
| | 54AC/74AC273 Octal D Flip-Flop | 4-165 |
| | 54ACT/74ACT273 Octal D Flip-Flop | 4-165 |
| | 54AC/74AC280 9-Bit Parity Generator/Checker | 4-170 |
| | 54ACT/74ACT280 9-Bit Parity Generator/Checker | 4-170 |
| | 54AC/74AC283 4-Bit Binary Full Adder with Fast Carry | 4-174 |
| | 54ACT/74ACT283 4-Bit Binary Full Adder with Fast Carry | 4-174 |
| | 54AC/74AC299 8-Input Universal Shift/Storage Register with Common Parallel I/O Pins | 4-175 |
| | 54ACT/74ACT299 8-Input Universal Shift/Storage Register with Common Parallel I/O Pins | 4-175 |
| | 54ACT/74ACT323 8-Bit Universal Shift/Storage Register with Synchronous Reset and | OAA6 |
| | Common I/O Pins | 4-182 |
| | 54AC/74AC350 4-Bit Shifter with TRI-STATE Outputs | 4-187 |
| | 54ACT/74ACT350 4-Bit Shifter with TRI-STATE Outputs | 4-187 |
| | 54AC/74AC373 Octal Transparent Latch with TRI-STATE Outputs | 4-188 |
| | 54ACT/74ACT373 Octal Transparent Latch with TRI-STATE Outputs | 4-188 |
| | 54AC/74AC374 Octal D Flip-Flop with TRI-STATE Outputs | 4-194 |
| | 54ACT/74ACT374 Octal D Flip-Flop with TRI-STATE Outputs | 4-194 |
| | 54AC/74AC377 Octal D Flip-Flop with Clock Enable | 4-200 |
| | 54ACT/74ACT377 Octal D Flip-Flop with Clock Enable | 4-200 |
| | 54ACT/74ACT381 4-Bit Arithmetic Logic Unit | 4-206 |
| | 54ACT/74ACT399 Quad 2-Port Register | 4-207 |
| | 54AC/74AC520 8-Bit Identity Comparator | 4-211 |
| | | 4-211 |
| | 54ACT/74ACT520 8-Bit Identity Comparator | 4-211 |
| | 54ACT/74ACT520 8-Bit Identity Comparator | |
| | 54AC/74AC521 8-Bit Identity Comparator 54ACT/74ACT521 8-Bit Identity Comparator | 4-211 |
| | 54AC/74AC521 8-Bit Identity Comparator | 4-211 4-217 |
| | 54AC/74AC521 8-Bit Identity Comparator 54ACT/74ACT521 8-Bit Identity Comparator | 4-211 4-217 4-217 |
| | 54AC/74AC521 8-Bit Identity Comparator | 4-211 4-217 4-217 4-223 |
| | 54AC/74AC521 8-Bit Identity Comparator 54ACT/74ACT521 8-Bit Identity Comparator 54ACT/74ACT534 Octal D Flip-Flop with TRI-STATE Outputs 54AC/74AC540 Octal Buffer/Line Driver with TRI-STATE Outputs 54ACT/74ACT540 Octal Buffer/Line Driver with TRI-STATE Outputs 54AC/74AC541 Octal Buffer/Line Driver with TRI-STATE Outputs | 4-211 4-217 4-217 4-223 4-228 |
| | 54AC/74AC521 8-Bit Identity Comparator 54ACT/74ACT521 8-Bit Identity Comparator 54ACT/74ACT534 Octal D Flip-Flop with TRI-STATE Outputs 54AC/74AC540 Octal Buffer/Line Driver with TRI-STATE Outputs 54ACT/74ACT540 Octal Buffer/Line Driver with TRI-STATE Outputs | 4-211 4-217 4-217 4-223 4-228 4-228 |
| | 54AC/74AC521 8-Bit Identity Comparator 54ACT/74ACT521 8-Bit Identity Comparator 54ACT/74ACT534 Octal D Flip-Flop with TRI-STATE Outputs 54AC/74AC540 Octal Buffer/Line Driver with TRI-STATE Outputs 54ACT/74ACT540 Octal Buffer/Line Driver with TRI-STATE Outputs 54AC/74AC541 Octal Buffer/Line Driver with TRI-STATE Outputs | 4-211 4-217 4-217 4-223 4-228 4-228 4-231 |
| | 54AC/74AC521 8-Bit Identity Comparator 54ACT/74ACT521 8-Bit Identity Comparator 54ACT/74ACT534 Octal D Flip-Flop with TRI-STATE Outputs 54AC/74AC540 Octal Buffer/Line Driver with TRI-STATE Outputs 54ACT/74ACT540 Octal Buffer/Line Driver with TRI-STATE Outputs 54AC/74AC541 Octal Buffer/Line Driver with TRI-STATE Outputs 54ACT/74ACT541 Octal Buffer/Line Driver with TRI-STATE Outputs 54ACT/74ACT543 Octal Registered Transceiver 54ACT/74ACT544 Octal Registered Transceiver | 4-211 4-217 4-217 4-223 4-228 4-228 4-231 4-231 |
| | 54AC/74AC521 8-Bit Identity Comparator 54ACT/74ACT521 8-Bit Identity Comparator 54ACT/74ACT534 Octal D Flip-Flop with TRI-STATE Outputs 54AC/74AC540 Octal Buffer/Line Driver with TRI-STATE Outputs 54ACT/74ACT540 Octal Buffer/Line Driver with TRI-STATE Outputs 54AC/74AC541 Octal Buffer/Line Driver with TRI-STATE Outputs 54ACT/74ACT541 Octal Buffer/Line Driver with TRI-STATE Outputs 54ACT/74ACT543 Octal Registered Transceiver 54ACT/74ACT544 Octal Registered Transceiver 54ACT/74ACT563 Octal Latch with TRI-STATE Outputs | 4-211 4-217 4-217 4-223 4-228 4-228 4-231 4-231 4-234 |
| | 54AC/74AC521 8-Bit Identity Comparator 54ACT/74ACT521 8-Bit Identity Comparator 54ACT/74ACT534 Octal D Flip-Flop with TRI-STATE Outputs 54AC/74AC540 Octal Buffer/Line Driver with TRI-STATE Outputs 54ACT/74ACT540 Octal Buffer/Line Driver with TRI-STATE Outputs 54AC/74AC541 Octal Buffer/Line Driver with TRI-STATE Outputs 54ACT/74ACT541 Octal Buffer/Line Driver with TRI-STATE Outputs 54ACT/74ACT543 Octal Registered Transceiver 54ACT/74ACT544 Octal Registered Transceiver | 4-211 4-217 4-217 4-223 4-228 4-231 4-231 4-234 4-235 |

| Section 4 Contents (Continued) | |
|--|-------|
| 54AC/74AC574 Octal D Flip-Flop with TRI-STATE Outputs | 4-249 |
| 54ACT/74ACT574 Octal D Flip-Flop with TRI-STATE Outputs | |
| 54AC/74AC646 Octal Transceiver/Register with TRI-STATE Outputs | |
| 54ACT/74ACT646 Octal Transceiver/Register with TRI-STATE Outputs | |
| 54AC/74AC648 Octal Transceiver/Register with TRI-STATE Outputs | 4-263 |
| 54ACT/74ACT657 Octal Bidirectional Transceiver with 8-Bit Parity Generator/Checker and | |
| TRI-STATE Outputs | 4-269 |
| 54ACT/74ACT705 Arithmetic Logic Unit for Digital Signal Processing Applications | 4-270 |
| 54ACT/74ACT715 Programmable Video Sync Generator | 4-271 |
| 54ACT/74ACT725 512 x 9 First In, First Out Memory (FIFO) | 4-272 |
| 54ACT/74ACT818 8-Bit Diagnostic Register | |
| 54AC/74AC821 10-Bit D Flip-Flop with TRI-STATE Outputs | 4-279 |
| 54ACT/74ACT821 10-Bit D Flip-Flop with TRI-STATE Outputs | |
| 54AC/74AC823 9-Bit D Flip-Flop | |
| 54ACT/74ACT823 9-Bit D Flip-Flop | 4-285 |
| 54AC/74AC825 8-Bit D Flip-Flop | 4-289 |
| 54ACT/74ACT825 8-Bit D Flip-Flop | |
| 54ACT/74ACT827 10-Bit Buffer/Line Driver with TRI-STATE Outputs | 4-293 |
| 54ACT/74ACT841 10-Bit Transparent Latch with TRI-STATE Outputs | 4-294 |
| 54AC/74AC843 9-Bit Transparent Latch | 4-299 |
| 54ACT/74ACT843 9-Bit Transparent Latch | 4-299 |
| 54AC/74AC845 8-Bit Transparent Latch with TRI-STATE Outputs | 4-307 |
| 54ACT/74ACT845 8-Bit Transparent Latch with TRI-STATE Outputs | 4-307 |
| 54ACT/74ACT1016 16 x 16 Parallel Multiplier | 4-312 |
| 54ACT/74ACT1110 Single Port 16 x 16 Bit Multiplier/Accumulator | 4-322 |
| 54AC/74AC2708 64 x 9 First-In, First-Out Memory | 4-324 |
| 54ACT/74ACT2708 64 x 9 First-In, First-Out Memory | |
| 54AC/74AC4024 7-Stage Binary Ripple Counter | 4-340 |
| | |



54AC/74AC00 • 54ACT/74ACT00 Quad 2-Input NAND Gate

General Description

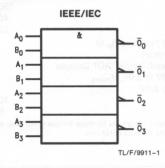
The 'AC/'ACT00 contains four 2-input NAND gates.

Features

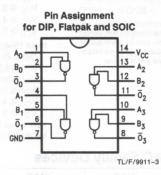
- Outputs source/sink 24 mA
- 'ACT00 has TTL-compatible inputs

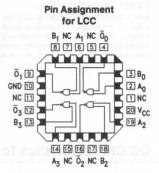
Ordering Code: See Section 5

Logic Symbol



Connection Diagrams





TL/F/9911-2

| Pin Names | Description | | | | |
|---------------------------------|-------------|--|--|--|--|
| A _n , B _n | Inputs | | | | |
| \overline{O}_n | Outputs | | | | |

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Office/ Distributors for availability | ty and specimounions. |
|---|-----------------------------------|
| Supply Voltage (V _{CC}) | -0.5V to $+7.0V$ |
| DC Input Diode Current (IIK) | |
| $V_I = -0.5V$ | -20 mA |
| $V_I = V_{CC} + 0.5V$ | + 20 mA |
| DC Input Voltage (V _I) | $-0.5V$ to $V_{CC} + 0.5V$ |
| DC Output Diode Current (IOK) | |
| $V_O = -0.5V$ Am AS | -20 mA |
| $V_O = V_{CC} + 0.5V$ | + 20 mA |
| DC Output Voltage (V _O) | -0.5 V to to V_{CC} + 0.5 V |
| DC Output Source | |
| or Sink Current (IO) | ±50 mA |
| DC V _{CC} or Ground Current | |
| per Output Pin (I _{CC} or I _{GND}) | ±50 mA |
| Storage Temperature (T _{STG}) | -65°C to +150°C |
| | |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (VCC)

| 'AC | 2.0V to 6.0V |
|--|-----------------------|
| 'ACT | 4.5V to 5.5V |
| Input Voltage (V _I) | 0V to V _{CC} |
| Output Voltage (V _O) | 0V to V _{CC} |
| 이 얼마나 이렇게 되었다. 그 그 그 그 그 그 그 그 그 그 그 그 그 그 그 그 그 그 그 | |

Operating Temperature (T_A)
74AC/ACT -40°C to +85°C
54AC/ACT -55°C to +125°C

Junction Temperature (T_J)
CDIP 175°C
PDIP 140°C

(Note 2) (Typical)
(Except Schmitt Inputs) 'AC Devices
V_{IN} from 30% to 70% of V_{CC}

Input Rise and Fall Time (tr, tf)

 VCC @ 3.0V
 150 ns/V

 VCC @ 4.5V
 40 ns/V

 VCC @ 5.5V
 25 ns/V

Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'ACT Devices V_{IN} from 0.8V to 2.0V, V_{meas} from 0.8V to 2.0V V_{CC} @ 4.5V

V_{CC} @ 5.5V 8 ns/V

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

10 ns/V

DC Characteristics for 'AC Family Devices

| | Parameter | | 74 | AC | 54AC | 74AC | | |
|-----------------|--------------------------------------|---------------------|-------------------------|----------------------|-----------------------------------|---------------------------------|-------|--|
| Symbol | | V _{CC} (V) | T _A = +25°C | | T _A = -55°C to + 125°C | T _A = -40°C to +85°C | Units | Conditions |
| | | | Тур | | Guaranteed Li | mits | - | |
| V _{IH} | Minimum High Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ |
| V _{IL} | Maximum Low Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ |
| V _{OH} | Minimum High Level Output Voltage | 3.0 4.5 5.5 | 2.99 4.49 5.49 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | ٧ | $I_{OUT} = -50 \mu\text{A}$ |
| | | 3.0 4.5 5.5 | | 2.56 3.86 4.86 | 2.4 3.7 4.7 | 2.46 3.76 4.76 | V | *V _{IN} = V _{IL} or V _{II} - 12 m/ I _{OH} - 24 m/ - 24 m/ |
| V _{OL} | Maximum Low Level Output Voltage | 3.0 4.5 5.5 | 0.002 0.001 0.001 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | ٧ | $I_{OUT} = 50 \mu A$ |
| | | 3.0 4.5 5.5 | | 0.36 0.36 0.36 | 0.5 0.5 0.5 | 0.44 0.44 0.44 | V | $V_{IN} = V_{IL} \text{ or } V_{IH}$ 12 m/s V_{IOL} 24 m/s |
| I _{IN} | Maximum Input Leakage Current | 5.5 | | ±0.1 | ± 1.0 | ±1.0 | μΑ | $V_I = V_{CC}$, GND |

^{*}All outputs loaded; thresholds on input associated with output under test.

[†]Maximum test duration 2.0 ms, one output loaded at a time.

Note: $I_{|N}$ and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC} . I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'AC Family Devices (Continued) (School and Characteristics for 'AC Family Devices (Continued))

| Symbol | Parameter | | 74AC T _A = +25°C | | 54AC | 74AC | | |
|------------------|-------------------------------------|---------------------|--------------------------------|-------|----------------------------------|---------------------------------|-------|------------------------------|
| | | V _{CC} (V) | | | T _A = -55°C to +125°C | T _A = -40°C to +85°C | Units | Conditions |
| | | | Тур | 12 | Guaranteed Li | mits | | |
| I _{OLD} | †Minimum Dynamic | 5.5 | XXXX | CHERN | 50 | 75 | mA | V _{OLD} = 1.65V Max |
| IOHD | Output Current | 5.5 | 2.8 | 0.1 | -50 o | -75 | mA | V _{OHD} = 3.85V Min |
| Icc | Maximum Quiescent Supply Current | 5.5 | 9.0 | 4.0 | 0.8 80.0 ^{3.8} | 40.0 | μА | $V_{IN} = V_{CC}$ or GND |

^{*}All outputs loaded; thresholds on input associated with output under test.

Note: $I_{|N}$ and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}. I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

| | 6mU 0 86 + of | | 74. | ACT | 54ACT | 74ACT | hater | Symbol Peran | |
|------------------|--------------------------------------|------------------------|------------------------|--------------|---|---------------------------------|------------------|---|--|
| Symbol | Parameter | V _{CC} (V) | T _A = +25°C | | T _A = -55°C to +125°C | T _A = -40°C to +85°C | Units | Conditions | |
| 2-5 | an 8.8 0.1 | | Тур | 0.1 | Guaranteed Li | mits | rsieQ no | fagagoraof | |
| V _{IH} | Minimum High Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 2.0 2.0 | 2.0 2.0 | 2.0 2.0 | rale v no | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{IL} | Maximum Low Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 0.8 0.8 | 0.8 0.8 | 0.8 0.8 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{OH} | Minimum High Level Output Voltage | 4.5 5.5 | 4.49 5.49 | 4.4 5.4 | 4.4 A \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ | 4.4 5.4 | V | $I_{OUT} = -50 \mu\text{A}$ | |
| | VO | 4.5 5.5 | υV υV | 3.86 4.86 | 3.70 4.70 | 3.76 4.76 | wo V | $^{*V_{\text{IN}}} = V_{\text{IL}} \text{ or } V_{\text{IH}} \\ -24 \text{ mA} \\ -24 \text{ mA}$ | |
| V _{OL} | Maximum Low Level Output Voltage | 4.5 5.5 | 0.001 0.001 | 0.1 0.1 | 0.1 0.1 | 0.1 0.1 | ٧ | I _{OUT} = 50 μA | |
| | | 4.5 5.5 | | 0.36 0.36 | 0.50 0.50 | 0.44 0.44 | v | $\begin{tabular}{ll} *V_{IN} = V_{IL} \mbox{ or } V_{IH} \\ I_{OL} & 24 \mbox{ mA} \\ & 24 \mbox{ mA} \\ \end{tabular}$ | |
| I _{IN} | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | ±1.0 | μΑ | $V_{I} = V_{CC}$, GND | |
| Ісст | Maximum I _{CC} /Input | 5.5 | 0.6 | | 1.6 | 1.5 | mA | $V_I = V_{CC} - 2.1V$ | |
| I _{OLD} | †Minimum Dynamic | 5.5 | | | 50 | 75 | mA | V _{OLD} = 1.65V Max | |
| I _{OHD} | Output Current 5.5 | | | | -50 | -75 | mA | V _{OHD} = 3.85V Min | |
| Icc | Maximum Quiescent Supply Current | 5.5 | | 4.0 | 80.0 | 40.0 | μА | $V_{IN} = V_{CC}$ or GND | |

 $^{{}^{*}}$ All outputs loaded; thresholds on input associated with output under test.

[†]Maximum test duration 2.0 ms, one output loaded at a time.

[†]Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

| | Parameter | V _{CC} * | 74AC T _A = +25°C C _L = 50 pF | | | 54 | 54AC | | AC | | |
|------------------|-------------------|-------------------|--|------------|------------|--|-------------|--|-------------|-------|-------------|
| Symbol | | | | | | T _A = -55°C to + 125°C C _L = 50 pF | | $T_A = -40^{\circ}C$ $to +85^{\circ}C$ $C_L = 50 pF$ | | Units | Fig. No. |
| | | | Min | Тур | Max | Min | Max | Min | Max | | |
| t _{PLH} | Propagation Delay | 3.3 5.0 | 2.0 1.5 | 7.0 6.0 | 9.5 8.0 | 1.0 1.0 | 11.0 8.5 | 2.0 1.5 | 10.0 8.5 | ns | 2-5 |
| t _{PHL} | Propagation Delay | 3.3 5.0 | 1.5 1.5 | 5.5 4.5 | 8.0 6.5 | 1.0 1.0 | 9.0 7.0 | 1.0 1.0 | 8.5 7.0 | ns | 2-5 |

^{*}Voltage Range 3.3 is 3.3V ± 0.3 V Voltage Range 5.0 is 5.0V ± 0.5 V

AC Electrical Characteristics

| Symbol | Parameter annu | | 74ACT T _A = +25°C C _L = 50 pF | | | $\begin{aligned} & 54\text{ACT} \\ & \textbf{T}_{\textbf{A}} = -55^{\circ}\text{C} \\ & \text{to} + 125^{\circ}\text{C} \\ & \textbf{C}_{\textbf{L}} = 50 \text{ pF} \end{aligned}$ | | 744 | CT | Second Second | - |
|------------------|-------------------|-------------------|---|-----|-----|---|-----|--|-----|---------------|-------------|
| | | V _{CC} * | | | | | | $T_A = -40^{\circ}C$ to $+85^{\circ}C$ $C_L = 50 \text{ pF}$ | | Units | Fig. No. |
| anold | | nou anno page of | Min | Тур | Max | Min | Max | Min | Max | 1 | en nya |
| t _{PLH} | Propagation Delay | 5.0 | 1.5 | 5.5 | 9.0 | 1.0 | 9.5 | 1.0 | 9.5 | ns | 2-5 |
| t _{PHL} | Propagation Delay | 5.0 | 1.5 | 4.0 | 7.0 | 1.0 | 8.0 | 1.0 | 8.0 | ns | 2-5 |

Voltage Range 5.0 is 5.0V ±0.5V

| Symbol | Parameter | AC/ACT | Units | Conditions | | |
|-----------------|----------------------------------|--------|-------|------------------------|--|--|
| | T di dinetei | Тур | Onito | SAIC CONTRIBUTION | | |
| C _{IN} | Input Capacitance | 4.5 | pF | V _{CC} = 5.0V | | |
| C _{PD} | Power Dissipation Capacitance | 30.0 | pF | V _{CC} = 5.0V | | |



54AC/74AC02 **Quad 2-Input NOR Gate**

General Description

The 'AC02 contains four, 2-input NOR gates.

Features

Outputs source/sink 24 mA

TL/F/9912-3

Connection Diagrams

Ordering Code: See Section 5

IEEE/IEC

 \bar{o}_0

TL/F/9912-1

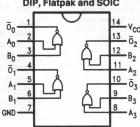
Logic Symbol

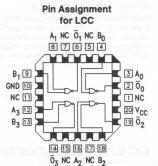
A2

A₃

B3

Pin Assignment for DIP, Flatpak and SOIC ·Vcc 13 02





TL/F/9912-2

| Pin Names | Description |
|---------------------------------|-------------|
| A _n , B _n | Inputs |
| Ōn | Outputs |

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

-0.5V to +7.0VSupply Voltage (VCC) DC Input Diode Current (IIK) $V_1 = -0.5V$ -20 mA $V_I = V_{CC} + 0.5V$ +20 mA DC Input Voltage (V_I) -0.5V to $V_{CC} + 0.5V$ DC Output Diode Current (IOK) -20 mA $V_0 = -0.5V$ $V_O = V_{CC} + 0.5V$ +20 mA DC Output Voltage (VO) -0.5V to to $V_{CC} + 0.5V$ DC Output Source

or Sink Current (I_O)
DC V_{CC} or Ground Current
per Output Pin (I_{CC} or I_{GND})

Storage Temperature (T_{STG}) -65°C to +150°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

Recommended Operating Conditions

 Supply Voltage (V_{CC})
 2.0V to 6.0V

 'AC
 2.0V to 5.5V

 4.5V to 5.5V

 $\begin{array}{ll} \text{Input Voltage (V_I)} & \text{OV to V}_{\text{CC}} \\ \text{Output Voltage (V}_{\text{O}}) & \text{OV to V}_{\text{CC}} \end{array}$

Operating Temperature (T_A)
74AC/ACT -40°C to +85°C
54AC/ACT -55°C to +125°C

Junction Temperature (T_J)

CDIP 175°C
PDIP 140°C

Input Rise and Fall Time (tr, tf)

(Note 2) (Typical)
(Except Schmitt Inputs) 'AC Devices

V_{IN} from 30% to 70% of V_{CC}

V_{CC} @ 3.0V 150 ns/V V_{CC} @ 4.5V 40 ns/V V_{CC} @ 5.5V 25 ns/V

Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical)

(Except Schmitt Inputs) 'ACT Devices

V_{IN} from 0.8V to 2.0V, V_{meas}

from 0.8V to 2.0V

V_{CC} @ 4.5V 10 ns/V V_{CC} @ 5.5V 8 ns/V

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

| | | | 74 | AC | 54AC | 74AC | | |
|-----------------|--------------------------------------|---------------------|-------------------------|----------------------|----------------------------------|---------------------------------|-------|---|
| Symbol | Parameter | V _{CC} (V) | T _A = +25°C | | T _A = -55°C to +125°C | T _A = -40°C to +85°C | Units | Conditions |
| | | | Тур | | Guaranteed Li | mits | | AB ₁₀ A |
| V _{IH} | Minimum High Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ |
| V _{IL} | Maximum Low Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ |
| V _{OH} | Minimum High Level Output Voltage | 3.0 4.5 5.5 | 2.99 4.49 5.49 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | V | $I_{OUT} = -50 \mu$ A |
| | | 3.0 4.5 5.5 | | 2.56 3.86 4.86 | 2.4 3.7 4.7 | 2.46 3.76 4.76 | V | *V _{IN} = V _{IL} or V - 12 m I _{OH} - 24 m - 24 m |
| V _{OL} | Maximum Low Level Output Voltage | 3.0 4.5 5.5 | 0.002 0.001 0.001 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | V | $I_{OUT} = 50 \mu A$ |
| | | 3.0 4.5 5.5 | | 0.36 0.36 0.36 | 0.5 0.5 0.5 | 0.44 0.44 0.44 | V | $*V_{IN} = V_{IL} \text{ or } V_{I}$ 12 m I_{OL} 24 m 24 m |
| I _{IN} | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | ±1.0 | μА | $V_{I} = V_{CC}$, GND |

 $\pm 50 \text{ mA}$

 $\pm 50 \text{ mA}$

DC Characteristics for 'AC Family Devices (Continued)

| Symbol | Parameter | | 74AC T _A = +25°C | | 54AC | 74AC | Units | Conditions | |
|------------------|-------------------------------------|-----------------|--------------------------------|-----|----------------------------------|---------------------------------|-------|------------------------------|--|
| | | V _{CC} | | | T _A = -55°C to +125°C | T _A = -40°C to +85°C | | | |
| | | | Тур | | Guaranteed Li | mits | | RPANJARE | |
| I _{OLD} | †Minimum Dynamic | 5.5 | | | 50 | 75 | mA | V _{OLD} = 1.65V Max | |
| I _{OHD} | Output Current | 5.5 | | | -50 | -75 | mA | V _{OHD} = 3.85V Min | |
| Icc | Maximum Quiescent Supply Current | 5.5 | eink 24 | 4.0 | 80.0 | 40.0 | μА | $V_{IN} = V_{CC}$ or GND | |

^{*}All outputs loaded; thresholds on input associated with output under test.

Note: $I_{\|N\|}$ and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC} . I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

AC Electrical Characteristics

| Symbol | | | $I_A = +25^{\circ}C$ to +129 | | | AC | 74AC T _A = -40°C to +85°C C _L = 50 pF | | Units | Fig. | |
|------------------|-------------------|-----------------------|------------------------------|------------|------------|---|--|------------|------------|----------------------------|-----|
| | Parameter | V _{CC} * (V) | | | | $T_A = -55^{\circ}C$ to + 125°C $C_L = 50 \text{ pF}$ | | | | | |
| | | 8) | Min | Тур | Max | Min | Max | Min | Max | of the same of the same of | 114 |
| t _{PLH} | Propagation Delay | 3.3 5.0 | 1.5 1.5 | 5.0 4.0 | 7.5 6.0 | 1.0 1.0 | 9.0 7.0 | 1.0 1.0 | 8.0 6.5 | ns | 2-5 |
| t _{PHL} | Propagation Delay | 3.3 5.0 | 1.5 1.5 | 5.0 4.5 | 7.5 6.5 | 1.0 1.0 | 9.0 7.5 | 1.0 | 8.0 7.0 | ns | 2-5 |

^{*}Voltage Range 3.3 is 3.3V \pm 0.3V Voltage Range 5.0 is 5.0V \pm 0.5V

| Symbol | Parameter | AC/ACT | Units | Conditions | |
|-----------------|-------------------------------|--------|-------|-----------------|--|
| Oymbol . | rananeter | Тур | Onits | | |
| C _{IN} | Input Capacitance | 4.5 | pF | $V_{CC} = 5.0V$ | |
| C _{PD} | Power Dissipation Capacitance | 30.0 | pF | $V_{CC} = 5.0V$ | |

[†]Maximum test duration 2.0 ms, one output loaded at a time.



54AC/74AC04 • 54ACT/74ACT04 **Hex Inverter**

General Description

The 'AC/'ACT04 contains six inverters.

The information for the 'ACT04 is Advanced Information only.

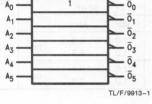
Features

- Outputs source/sink 24 mA
- 'ACT04 has TTL-compatible inputs

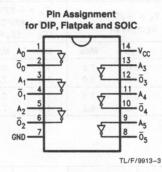
Ordering Code: See Section 5

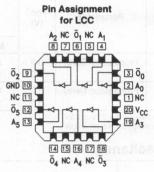
Logic Symbol

IEEE/IEC 0, ō,



Connection Diagrams





TL/F/9913-2

| Pin Names | Description |
|-----------|-------------|
| An | Inputs |
| Ōn | Outputs |

Absolute Maximum Rating (Note 1) Recommended Operating

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Supply Voltage (V _{CC}) | -0.5V to +7.0V |
|--|-----------------------------------|
| DC Input Diode Current (I_{IK}) $V_I = -0.5V$ | -20 mA |
| $V_{I} = V_{CC} + 0.5V$ | + 20 mA |
| DC Input Voltage (V _I) | $-0.5V$ to $V_{CC} + 0.5V$ |
| DC Output Diode Current (I_{OK}) $V_O = -0.5V$ $V_O = V_{CC} + 0.5V$ | −20 mA +20 mA |
| DC Output Voltage (VO) | -0.5 V to to V_{CC} + 0.5 V |
| DC Output Source or Sink Current (I _O) | ± 50 mA |
| DC V _{CC} or Ground Current per Output Pin (I _{CC} or I _{GND}) | ±50 mA |
| Storage Temperature (T _{STG}) | -65°C to +150°C |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

Recommended Operating Conditions

typical input rise and fall times noted here.

| Conditions | | |
|---|-------------------------|------------------------------|
| Supply Voltage (V _{CC}) 'AC 'ACT | | 2.0V to 6.0V 4.5V to 5.5V |
| Input Voltage (V _I) | | 0V to V _{CC} |
| Output Voltage (V _O) | | 0V to V _{CC} |
| Operating Temperatur 74AC/ACT 54AC/ACT | e (T _A) | |
| Junction Temperature | | 10 Marie 14 1 1 1 2 2 3 3 1 |
| CDIP | sipases sugn no abienes | 175°C |
| Input Rise and Fall Tir (Note 2) (Typical) (Except Schmitt Input) V _{IN} from 30% to 70 | uts) 'AC Devices | |
| V _{CC} @ 3.0V | | 150 ns/V |
| V _{CC} @ 4.5V | | 40 ns/V |
| V _{CC} @ 5.5V | | 25 ns/V |
| Input Rise and Fall Tir (Note 2) (Typical) (Except Schmitt Input V _{IN} from 0.8V to 2.0V from 0.8V to 2.0V | uts) 'ACT Devices | |
| V _{CC} @ 4.5V V _{CC} @ 5.5V | | 10 ns/V 8 ns/V |
| Note 2: See individual data | sheets for those device | s which differ from the |

DC Characteristics for 'AC Family Devices

| | | | 74AC | | 54AC | 74AC | | Conditions | |
|-----------------|----------------------------------|-------------------------------|-------|--------|----------------------------------|---------------------------------|-------|---------------------------------------|--|
| Symbol | | Parameter V _{CC} (V) | | + 25°C | T _A = -55°C to +125°C | T _A = -40°C to +85°C | Units | | |
| | | | Тур | | Guaranteed Li | mits | | | |
| VIH | Minimum High Level | 3.0 | 1.5 | 2.1 | 2.1 | 2.106050 h | qnl | V _{OUT} = 0.1V | |
| | Input Voltage | 4.5 | 2.25 | 3.15 | 3.15 | 3.15 | V | or V _{CC} - 0.1V | |
| | - Y0 | 5.5 | 2.75 | 3.85 | 3.85 | 3.85 | .0 | | |
| VIL | Maximum Low Level | 3.0 | 1.5 | 0.9 | 0.9 | 0.9 | | V _{OUT} = 0.1V | |
| | Input Voltage | 4.5 | 2.25 | 1.35 | 1.35 | 1.35 | V | or V _{CC} - 0.1V | |
| | | 5.5 | 2.75 | 1.65 | 1.65 | 1.65 | | | |
| V _{OH} | Minimum High Level | 3.0 | 2.99 | 2.9 | 2.9 | 2.9 | | $I_{OUT} = -50 \mu A$ | |
| | Output Voltage | 4.5 | 4.49 | 4.4 | 4.4 | 4.4 | V | | |
| | | 5.5 | 5.49 | 5.4 | 5.4 | 5.4 | | | |
| | | | | | | | | *VIN = VIL or VIH | |
| | | 3.0 | | 2.56 | 2.4 | 2.46 | | -12 mA | |
| | | 4.5 | | 3.86 | 3.7 | 3.76 | V | I _{OH} -24 mA | |
| | | 5.5 | | 4.86 | 4.7 | 4.76 | | −24 mA | |
| V _{OL} | Maximum Low Level | 3.0 | 0.002 | 0.1 | 0.1 | 0.1 | | $I_{OUT} = 50 \mu A$ | |
| | Output Voltage | 4.5 | 0.001 | 0.1 | 0.1 | 0.1 | V | | |
| | | 5.5 | 0.001 | 0.1 | 0.1 | 0.1 | | | |
| | | | | | | | | $*V_{IN} = V_{IL} \text{ or } V_{IH}$ | |
| | | 3.0 | | 0.36 | 0.5 | 0.44 | | 12 mA | |
| | | 4.5 | | 0.36 | 0.5 | 0.44 | V | I _{OL} 24 mA | |
| | | 5.5 | | 0.36 | 0.5 | 0.44 | | 24 mA | |
| I _{IN} | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | ±1.0 | μΑ | $V_{I} = V_{CC}$, GND | |

DC Characteristics for 'AC Family Devices (Continued) and the state of the state of

| | Parameter | V _{CC} (V) | 74AC T _A = +25°C | | 54AC | 74AC | Units | Conditions | |
|--------|-------------------------------------|---------------------|-----------------------------|--------------------|-----------------------------------|---------------------------------|-----------|------------------------------|--|
| Symbol | | | | | T _A = -55°C to + 125°C | T _A = -40°C to +85°C | | | |
| | | | Тур | pgs/feV/fi | Guaranteed Li | mits | on() impa | NO aboli hard 00 | |
| IOLD | †Minimum Dynamic | 5.5 | (6V) 9 | BNoV Rou | 50 | 75 | mA | V _{OLD} = 1.65V Max | |
| IOHD | Output Current | 5.5 | PASK-Car | et gnuz Foekost | -50 | V 01 V3 /2-75 | mA | V _{OHD} = 3.85V Min | |
| Icc | Maximum Quiescent Supply Current | 5.5 | | 4.0 | 80.0 | 40.0 | μА | $V_{IN} = V_{CC}$ or GND | |

^{*}All outputs loaded; thresholds on input associated with output under test.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

AC Electrical Characteristics

| V\an at | Parameter | | 74AC | | 54AC T _A = -55°C to + 125°C C _L = 50 pF | | 74AC T _A = -40°C to +85°C C _L = 50 pF | | Units | Fig. | |
|------------------|-------------------|-----------------------|--|------------|--|------------|--|------------|-------------|------|-----|
| Symbol | | V _{CC} * (V) | T _A = +25°C C _L = 50 pF | | | | | | | | |
| | | V. Venera | on V. Vo. | Min | Тур | Max | Min | Max | Min | Max | |
| t _{PLH} | Propagation Delay | 3.3 5.0 | 1.5 1.5 | 4.5 4.0 | 9.0 7.0 | 1.0 1.0 | 11.0 8.5 | 1.0 1.0 | 10.0 7.5 | ns | 2-5 |
| t _{PHL} | Propagation Delay | 3.3 5.0 | 1.5 1.5 | 4.5 3.5 | 8.5 6.5 | 1.0 1.0 | 10.0 7.5 | 1.0 1.0 | 9.5 7.0 | ns | 2-5 |

Paramet

| Symbol | Parameter | AC/ACT | Units | Conditions | |
|------------------------|----------------------------------|--------|--------|------------------------|--|
| Symbol | affi | Тур | Office | | |
| CIN | Input Capacitance | 4.5 | pF | $V_{CC} = 5.0V$ | |
| C _{PD} 00V 10 | Power Dissipation Capacitance | 30.0 | pF | V _{CC} = 5.0V | |

[†]Maximum test duration 2.0 ms, one output loaded at a time.

^{*}Voltage Range 3.3 is 3.3V ± 0.3 V Voltage Range 5.0 is 5.0V ± 0.5 V



54AC/74AC08 • 54ACT/74ACT08 Quad 2-Input AND Gate

General Description

The 'AC/'ACT08 contains four, 2-input AND gates.

Features

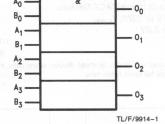
- Outputs source/sink 24 mA
- 'ACT08 has TTL-compatible inputs

The information for the 'ACT08 is Advanced Information only.

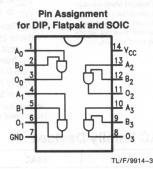
Ordering Code: See Section 5

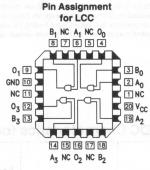
Logic Symbols

IEEE/IEC



Connection Diagrams





TL/F/9914-2

| Pin Names | Description |
|---------------------------------|-------------|
| A _n , B _n | Inputs |
| On | Outputs |

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Office, Distributoro for availabili | cy and opcomodition |
|---|-----------------------------------|
| Supply Voltage (V _{CC}) | -0.5V to $+7.0V$ |
| DC Input Diode Current (IIK) | |
| $V_1 = -0.5V$ | -20 mA |
| $V_I = V_{CC} + 0.5V$ | + 20 mA |
| DC Input Voltage (V _I) | $-0.5V$ to $V_{CC} + 0.5V$ |
| DC Output Diode Current (IOK) | |
| $V_{O} = -0.5V$ | -20 mA |
| $V_O = V_{CC} + 0.5V$ | + 20 mA |
| DC Output Voltage (V _O) | -0.5 V to to V_{CC} + 0.5 V |
| DC Output Source | |
| or Sink Current (I _O) | \pm 50 mA |
| DC V _{CC} or Ground Current | |
| per Output Pin (I _{CC} or I _{GND}) | ± 50 mA |
| Storage Temperature (T _{STG}) | -65°C to +150°C |
| | |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

Recommended Operating Conditions

| Conditions | |
|---|-----------------------|
| Supply Voltage (V _{CC}) | |
| 'AC | 2.0V to 6.0V |
| 'ACT | 4.5V to 5.5V |
| Input Voltage (V _I) | 0V to V _{CC} |
| Output Voltage (V _O) | 0V to V _{CC} |
| Operating Temperature (T _A) | |
| 74AC/ACT | -40°C to +85°C |
| 54AC/ACT | -55°C to +125°C |
| Junction Temperature (T _J) | |
| CDIP | 175°C |
| PDIP somethal at 507 JA1 at 1 sol n | 140°C |
| Input Rise and Fall Time (t _r , t _f) | |
| (Note 2) (Typical) | |
| (Except Schmitt Inputs) 'AC Devices | S |
| V_{IN} from 30% to 70% of V_{CC} | |
| V _{CC} @ 3.0V | 150 ns/V |
| V _{CC} @ 4.5V | 40 ns/V |
| V _{CC} @ 5.5V | 25 ns/V |
| Input Rise and Fall Time (t _r , t _f) | |
| (Note 2) (Typical) | |
| (Except Schmitt Inputs) 'ACT Device | es |
| V _{IN} from 0.8V to 2.0V, V _{meas} | |

V_{CC} @ 5.5V Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

10 ns/V

8 ns/V

from 0.8V to 2.0V

V_{CC} @ 4.5V

DC Characteristics for 'AC Family Devices

| | Fall of the GP Act of the GP A | | 74 | AC | 54AC | 74AC | | |
|-----------------|--|------------------------|-------------------------|----------------------|----------------------------------|---|-------|---|
| Symbol | Parameter | V _{CC} (V) | T _A = | + 25°C | T _A = -55°C to +125°C | $T_A = -40^{\circ}C \text{ to } +85^{\circ}C$ | Units | Conditions |
| | | | Тур | | Guaranteed Lin | mits delicated | 6.0 | Pin Nam |
| V _{IH} | Minimum High Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ |
| V _{IL} | Maximum Low Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ |
| V _{OH} | Minimum High Level Output Voltage | 3.0 4.5 5.5 | 2.99 4.49 5.49 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | ٧ | I _{OUT} = -50 μ/ |
| | | 3.0 4.5 5.5 | , | 2.56 3.86 4.86 | 2.4 3.7 4.7 | 2.46 3.76 4.76 | ٧ | *V _{IN} = V _{IL} or V - 12 m I _{OH} - 24 m - 24 m |
| V _{OL} | Maximum Low Level Output Voltage | 3.0 4.5 5.5 | 0.002 0.001 0.001 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | ٧ | I _{OUT} = 50 μA |
| | | 3.0 4.5 5.5 | | 0.36 0.36 0.36 | 0.5 0.5 0.5 | 0.44 0.44 0.44 | ٧ | *V _{IN} = V _{IL} or V 12 n I _{OL} 24 n 24 n |
| I _{IN} | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | ±1.0 | μΑ | $V_{I} = V_{CC}$, GND |

DC Characteristics for 'AC Family Devices (Continued)

| | | | 74 | AC | 54AC | 74AC | 1000 | |
|------------------|-------------------------------------|---------------------|------------------------|-----|----------------------------------|---------------------------------|-------|------------------------------|
| Symbol | Parameter | V _{CC} (V) | T _A = +25°C | | T _A = -55°C to +125°C | T _A = -40°C to +85°C | Units | Conditions |
| | | | Тур | | Guaranteed Li | mits | | RETURNS |
| I _{OLD} | †Minimum Dynamic | 5.5 | | | 50 | 75 | mA | V _{OLD} = 1.65V Max |
| I _{OHD} | Output Current | 5.5 | | | -50 | -75 | mA | V _{OHD} = 3.85V Min |
| Icc | Maximum Quiescent Supply Current | 5.5 | sink 24 | 4.0 | 80.0 | 40.0 | μА | $V_{IN} = V_{CC}$ or GND |

^{*}All outputs loaded; thresholds on input associated with output under test.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC} . I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

AC Electrical Characteristics

| | for LCG | | | 74AC | ine double | 54 | AC | 74 | AC | - | |
|------------------|-------------------|--------------------------|------------|-----------------------|------------|------------|-------------------------|------------|------------------------|-------|-------------|
| Symbol | Parameter | V _{CC} * (V) | | C _L = +25° | | to + | −55°C 125°C 50 pF | to + | -40°C 85°C 50 pF | Units | Fig. No. |
| | pu(E) 39- | | Min | Тур | Max | Min | Max | Min | Max | | |
| t _{PLH} | Propagation Delay | 3.3 5.0 | 1.5 1.5 | 7.5 5.5 | 9.5 7.5 | 1.0 1.0 | 12.5 9.0 | 1.0 1.0 | 10.0 8.5 | ns | 2-5 |
| t _{PHL} | Propagation Delay | 3.3 5.0 | 1.5 1.5 | 7.0 5.5 | 8.5 7.0 | 1.0 1.0 | 11.5 8.5 | 1.0 1.0 | 9.0 7.5 | ns | 2-5 |

^{*}Voltage Range 3.3 is 3.3V \pm 0.3V Voltage Range 5.0 is 5.0V \pm 0.5V

| Symbol | Parameter | AC/ACT | Units | Conditions |
|-----------------|----------------------------------|--------|-------|-----------------|
| Зуппоот | Farameter | Тур | Onits | Conditions |
| C _{IN} | Input Capacitance | 4.5 | pF | $V_{CC} = 5.0V$ |
| C _{PD} | Power Dissipation Capacitance | 20.0 | pF | $V_{CC} = 5.0V$ |

[†]Maximum test duration 2.0 ms, one output loaded at a time.



54AC/74AC10 Triple 3-Input NAND Gate

General Description

The 'AC10 contains three, 3-input NAND gates.

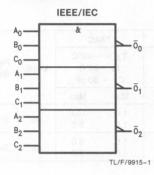
Features

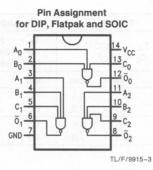
■ Outputs source/sink 24 mA

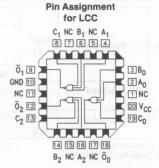
Ordering Code: See Section 5

Logic Symbol

Connection Diagrams







TL/F/9915-2

| Pin Names | Description |
|--|-------------|
| A _n , B _n , C _n | Inputs |
| \overline{O}_n | Outputs |

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required. please contact the National Semiconductor Sales Office/Distributors for availability and specifications. -0.5V to +7.0V Supply Voltage (Vcc)

| | 0.04 10 17.04 |
|------------|--------------------------|
| | -20 mA |
| | + 20 mA |
| -0.5V t | o V _{CC} + 0.5V |
| | −20 mA +20 mA |
| -0.5V to t | o V _{CC} + 0.5V |
| | ± 50 mA |
| | ± 50 mA |
| | e√-0.5V t |

Storage Temperature (TSTG) Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

-65°C to +150°C

Recommended Operating **Conditions**

| | 1010ms74 2.0 4.5 | V to 6.0V V to 5.5V |
|---------------------|--|---|
| | C | V to V _{CC} |
| | Ownimm Ovnemic | V to V _{CC} |
| e (T _A) | | to +85°C |
| | | |
| Signer : | | 175°C |
| uts) 'A(| Devices | |
| | | 150 ns/V |
| | | 40 ns/V 25 ns/V |
| uts) 'A0 | CT Devices | |
| | | 10 ns/V 8 ns/V |
| | The (T_A) (T_J) The (t_r, t_r) | (T_A) The (T_A) -40°C f -55°C to (T_J) The (t _r , t _f) The (t _r , t _f) |

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

| | | | 74 | AC | 54AC | 74AC | 2/8/4 | Capaditan |
|-----------------|----------------------------------|------------------------|-------------------------|--------------|----------------------------------|---------------------------------|-------|--|
| Symbol | Parameter | V _{CC} (V) | T _A = | + 25°C | T _A = -55°C to +125°C | T _A = -40°C to +85°C | Units | Conditions |
| | | | Тур | | Guaranteed Li | mits | | |
| V _{IH} | Minimum High Level | 3.0 | 1.5 | 2.1 | 2.1 | 2.1 | qui . | $V_{OUT} = 0.1V$ |
| | Input Voltage | 4.5 5.5 | 2.25 2.75 | 3.15 3.85 | 3.15 3.85 | 3.15 3.85 | | or V _{CC} = 0.1V |
| V _{IL} | Maximum Low Level | 3.0 | 1.5 | 0.9 | 0.9 | 0.9 | | $V_{OUT} = 0.1V$ |
| | Input Voltage | 4.5 5.5 | 2.25 2.75 | 1.35 1.65 | 1.35 1.65 | 1.35 1.65 | V | or V _{CC} - 0.1V |
| V _{OH} | Minimum High Level | 3.0 | 2.99 | 2.9 | 2.9 | 2.9 | | $I_{OUT} = -50 \mu A$ |
| | Output Voltage | 4.5 5.5 | 4.49 5.49 | 4.4 5.4 | 4.4 5.4 | 4.4 5.4 | V | |
| | | | | | | | | *V _{IN} = V _{IL} or V _{II} |
| | | 3.0 | | 2.56 | 2.4 | 2.46 | | −12 m |
| | | 4.5 5.5 | | 3.86 4.86 | 3.7 4.7 | 3.76 4.76 | V | l _{OH} −24 m _s −24 m _s |
| V _{OL} | Maximum Low Level | 3.0 | 0.002 | 0.1 | 0.1 | 0.1 | | I _{OUT} = 50 μA |
| | Output Voltage | 4.5 5.5 | 0.001 0.001 | 0.1 0.1 | 0.1 0.1 | 0.1 0.1 | V | |
| | | | | | | | | *V _{IN} = V _{IL} or V _{II} |
| | | 3.0 | | 0.36 | 0.5 | 0.44 | | 12 m |
| | | 4.5 5.5 | | 0.36 0.36 | 0.5 0.5 | 0.44 0.44 | V | I _{OL} 24 m. |
| IIN | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | ±1.0 | μΑ | $V_I = V_{CC}$, GND |

DC Characteristics for 'AC Family Devices (Continued) partial management of the continued o

| | | | 74 | AC | 54AC | 74AC | esta esta land med | Decreasy satisfied it |
|--------|-------------------------------------|---------------------|------------------|-----------|----------------------------------|---------------------------------|-----------------------|------------------------------|
| Symbol | Parameter | V _{CC} (V) | T _A = | + 25°C | T _A = -55°C to +125°C | T _A = -40°C to +85°C | Units | Conditions |
| | (0 | | Тур | agalloV : | Guaranteed Li | mits | rent (luc | DC Input Diede Sur |
| IOLD | †Minimum Dynamic | 5.5 | (0/5.0) | effoV too | 50 | 75 | mA | V _{OLD} = 1.65V Max |
| IOHD | Output Current | 5.5 | Little regin | | -50 | / of √8.0−75 | mA | V _{OHD} = 3.85V Min |
| Icc | Maximum Quiescent Supply Current | 5.5 | | 4.0 | 80.0 | 40.0 | μА | $V_{IN} = V_{CC}$ or GND |

^{*}All outputs loaded; thresholds on input associated with output under test.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

AC Electrical Characteristics

| | | | | 74AC | 908 | 54 | AC | 74 | AC | endoadr .l | 67gH |
|------------------|-------------------|------------|------------|---------------------------|------------|------------|---|------------|--|------------|------|
| Symbol | Parameter | | | T _A = +25°C to | | to + | $T_A = -55^{\circ}C$ to + 125°C $C_L = 50 pF$ | | $T_A = -40^{\circ}C$ $to +85^{\circ}C$ $C_L = 50 pF$ | | Fig. |
| | as | pmV NO | Min | Тур | Max | Min | Max | Min | Max | | |
| t _{PLH} | Propagation Delay | 3.3 5.0 | 1.5 1.5 | 6.0 4.5 | 9.5 7.0 | 1.0 1.0 | 11.0 8.5 | 1.0 1.0 | 10.5 8.0 | ns | 2-5 |
| t _{PHL} | Propagation Delay | 3.3 5.0 | 1.5 1.5 | 5.5 4.0 | 8.5 6.0 | 1.0 1.0 | 10.0 7.0 | 1.0 1.0 | 10.0 6.5 | ns | 2-5 |

^{*}Voltage Range 3.3 is 3.3V ± 0.3 V Voltage Range 5.0 is 5.0V ± 0.5 V

| Symbol | Parameter | AC/ACT | Units | Conditions |
|-----------------|-------------------------------|--------|--------|-----------------|
| Зушьог | rarameter | Тур | Office | Conditions |
| C _{IN} | Input Capacitance | 4.5 | pF | $V_{CC} = 5.0V$ |
| C _{PD} | Power Dissipation Capacitance | 25.0 | pF | $V_{CC} = 5.0V$ |

[†]Maximum test duration 2.0 ms, one output loaded at a time.



54AC/74AC11 Triple 3-Input AND Gate

General Description

The 'AC11 contains three 3-input AND gates.

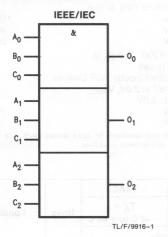
Features

Outputs source/sink 24 mA

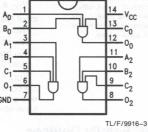
Connection Diagrams

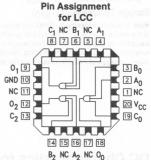
Ordering Code: See Section 5

Logic Symbol



Pin Assignment for DIP, Flatpak and SOIC





TL/F/9916-2

| Pin Names | Description |
|--|-------------|
| A _n , B _n , C _n | Inputs |
| On | Outputs |

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Supply Voltage (V _{CC}) | -0.5V to $+7.0V$ |
|---|-----------------------------------|
| DC Input Diode Current (I _{IK}) | |
| $V_{I} = -0.5V$ | -20 mA |
| $V_I = V_{CC} + 0.5V$ | + 20 mA |
| DC Input Voltage (V _I) | -0.5 V to V_{CC} + 0.5 V |
| DC Output Diode Current (IOK) | |
| $V_O = -0.5V$ | -20 mA |
| $V_O = V_{CC} + 0.5V$ | + 20 mA |
| DC Output Voltage (VO) | -0.5 V to to V_{CC} + 0.5 V |
| DC Output Source | |
| or Sink Current (IO) | ±50 mA |
| DC V _{CC} or Ground Current | |
| per Output Pin (I _{CC} or I _{GND}) | ±50 mA |
| Storage Temperature (T _{STG}) | -65°C to +150°C |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

Recommended Operating Conditions

| O O I I GITTO I I I I I I I I I I I I I I I I I I | |
|--|-----------------------|
| Supply Voltage (V _{CC}) | |
| 'AC | 2.0V to 6.0V |
| 'ACT | 4.5V to 5.5V |
| input voltage (VI) | OA TO ACC |
| Output Voltage (V _O) | 0V to V _{CC} |
| Operating Temperature (T _A) | |
| 74AC/ACT | -40°C to +85°C |
| 54AC/ACT | -55°C to +125°C |
| Junction Temperature (T _J) | |
| CDIP | 175°C |
| PDIP | 140°C |
| Input Rise and Fall Time (t _r , t _f) (Note 2) (Typical) (Except Schmitt Inputs) 'AC Devices | |
| V _{IN} from 30% to 70% of V _{CC} | |
| V _{CC} @ 3.0V | 150 ns/V |
| V _{CC} @ 4.5V | 40 ns/V |
| V _{CC} @ 5.5V | 25 ns/V |
| | 201137 4 |
| Input Rise and Fall Time (t _r , t _f) | |
| (Note 2) (Typical) | |
| (Except Schmitt Inputs) 'ACT Devices | |
| V _{IN} from 0.8V to 2.0V, V _{meas} from 0.8V to 2.0V | |
| 110111 0.00 to 2.00 | |

V_{CC} @ 5.5V Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

10 ns/V

8 ns/V

V_{CC} @ 4.5V

DC Characteristics for 'AC Family Devices

| | l Parameter | | 74 | AC | 54AC | 74AC | | James 24 |
|-----------------|--------------------------------------|---------------------|-------------------------|----------------------|---------------------------------|----------------------|------------|---|
| Symbol | | V _{CC} (V) | | | T _A = -40°C to +85°C | Units | Conditions | |
| | | | Тур | | Guaranteed Li | mits | | |
| V _{IH} | Minimum High Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ |
| V _{IL} | Maximum Low Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ |
| V _{OH} | Minimum High Level Output Voltage | 3.0 4.5 5.5 | 2.99 4.49 5.49 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | ٧ | $I_{OUT} = -50 \mu A$ |
| | | 3.0 4.5 5.5 | | 2.56 3.86 4.86 | 2.4 3.7 4.7 | 2.46 3.76 4.76 | ٧ | $V_{\rm IN} = V_{\rm IL} \text{ or } V_{\rm IH}$ -12 mA -24 mA -24 mA |
| V _{OL} | Maximum Low Level Output Voltage | 3.0 4.5 5.5 | 0.002 0.001 0.001 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | ٧ | $I_{OUT} = 50 \mu A$ |
| | | 3.0 4.5 5.5 | | 0.36 0.36 0.36 | 0.5 0.5 0.5 | 0.44 0.44 0.44 | ٧ | $*V_{IN} = V_{IL} \text{ or } V_{IH}$ 12 mA I_{OL} 24 mA 24 mA |
| I _{IN} | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | ±1.0 | μΑ | $V_I = V_{CC}$, GND |

DC Characteristics for 'AC Family Devices (Continued)

| | | | 74AC | | 54AC | 74AC | | |
|------------------|-------------------------------------|---------------------|------------------|--------|----------------------------------|---|-------|--|
| Symbol | Parameter | V _{CC} (V) | T _A = | + 25°C | T _A = -55°C to +125°C | $T_A = -40^{\circ}C \text{ to } +85^{\circ}C$ | Units | Conditions |
| | | | Тур | | Guaranteed Li | mits | MI W. | |
| I _{OLD} | †Minimum Dynamic | 5.5 | - Annual Control | uqni | 50 | 75 | mA | V _{OLD} = 1.65V Max |
| IOHD | Output Current | 5.5 | | | -50 | -75 | mA | V _{OHD} = 3.85V Min |
| Icc | Maximum Quiescent Supply Current | 5.5 | aleyri ser | 4.0 | 0.08 mg AO | 40.0 | μΑ | V _{IN} = V _{CC} or GND |

^{*}All outputs loaded; thresholds on input associated with output under test.

AC Characteristics

| | | | 74AC T _A = +25°C C _L = 50 pF | | | 54AC T _A = -55°C to + 125°C C _L = 50 pF | | 74AC T _A = -40°C to +85°C C _L = 50 pF | | Units | Fig. |
|------------------|-------------------|-------------------|---|------------|------------|--|-------------|--|-------------|-------|------|
| Symbol | Parameter | V _{CC} * | | | | | | | | | |
| | 2 | mater | Min | Тур | Max | Min | Max | Min | Max | | |
| t _{PLH} | Propagation Delay | 3.3 5.0 | 1.5 1.5 | 5.5 4.0 | 9.5 8.0 | 1.0 1.0 | 11.0 8.5 | 1.0 1.0 | 10.0 8.5 | ns | 2-5 |
| t _{PHL} | Propagation Delay | 3.3 5.0 | 1.5 1.5 | 5.5 4.0 | 8.5 7.0 | 1.0 | 10.5 8.0 | 1.0 1.0 | 9.5 7.5 | ns | 2-5 |

^{*}Voltage Range 3.3 is 3.3V ± 0.3 V

| Symbol | Parameter | 54/74AC | Units | Conditions | |
|-----------------|-------------------------------|---------|----------|-----------------|--|
| Symbol | Farameter | Тур | Office | | |
| CIN | Input Capacitance | 4.5 | pF - 3/0 | $V_{CC} = 5.0V$ | |
| C _{PD} | Power Dissipation Capacitance | 20.0 | pF | $V_{CC} = 5.0V$ | |

[†]Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

^{*}Voltage Range 5.0 is 5.0V ±0.5V



54AC/74AC14 • 54ACT/74ACT14 Hex Inverter with Schmitt Trigger Input

General Description

The 'AC/'ACT14 contains six inverter gates each with a Schmitt trigger input. The 'AC/'ACT14 contains six logic inverters which accept standard CMOS input signals (TTL levels for 'ACT14) and provide standard CMOS output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have a greater noise margin than conventional inverters

The 'AC/'ACT14 has hysteresis between the positive-going and negative-going input thresholds (typically 1.0V) which is determined internally by transistor ratios and is essentially insensitive to temperature and supply voltage variations.

Features

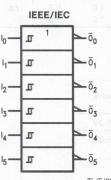
- Outputs source/sink 24 mA
- 'ACT14 has TTL-compatible inputs

The information for the 'ACT14 is Advanced Information only.

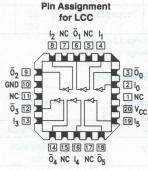
Ordering Code: See Section 5

Logic Symbol

Connection Diagrams



TL/F/9917-1



TL/F/9917-3

Function Table

| Input | Output |
|-------|--------|
| Α | ō |
| L | Н |
| Н | L |

| Pin Names | Description |
|------------------|-------------|
| In | Inputs |
| \overline{O}_n | Outputs |

Absolute Maximum Rating (Note 1) Recommended Operating

If Military/Aerospace specified devices are required. please contact the National Semiconductor Sales Office/Distributors for availability and specifications

| Office, Biotificatoro for avail | | |
|---|-------------------|---------------------------|
| Supply Voltage (V _{CC}) | 40°C to +85° | 0.5V to +7.0V |
| DC Input Diode Current (I _{IK}) | | |
| $V_1 = -0.5V$ | | -20 mA |
| $V_I = V_{CC} + 0.5V$ | | + 20 mA |
| DC Input Voltage (V _I) | -0.5V | to V _{CC} + 0.5V |
| DC Output Diode Current (IOK |) | |
| $V_0 = -0.5V$ | | -20 mA |
| $V_O = V_{CC} + 0.5V$ | | + 20 mA |
| DC Output Voltage (V _O) | -0.5V to | to V _{CC} + 0.5V |
| DC Output Source | | |
| or Sink Current (IO) | | ±50 mA |
| DC V _{CC} or Ground Current | | |
| per Output Pin (I _{CC} or I _{GND}) | | ± 50 mA |
| Storage Temperature (T _{STG}) | -6 | 5°C to +150°C |
| Note 1: Absolute maximum ratings are | those values beyo | ond which damage |

to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

Conditions

| Supply Voltage (V _{CC}) 'AC | 2.0V to 6.0V |
|--|-----------------------|
| 'ACT | 4.5V to 5.5V |
| Input Voltage (V _I) | 0V to V _{CC} |
| Output Voltage (V _O) | 0V to V _{CC} |
| Operating Temperature (T _A) 74AC/ACT | -40°C to +85°C |
| 54AC/ACT | -55°C to +125°C |
| Junction Temperature (T _J) CDIP PDIP | 175°C 140°C |
| Input Rise and Fall Time (t _r , (Note 2) (Typical) (Except Schmitt Inputs) 'A V _{IN} from 30% to 70% of V | C Devices |
| V _{CC} @ 3.0V | memic vice 150 ns/V |
| V _{CC} @ 4.5V | 40 ns/V |
| V _{CC} @ 5.5V | 25 ns/V |
| Input Rise and Fall Time (t _r , (Note 2) (Typical) (Except Schmitt Inputs) 'A V _{IN} from 0.8V to 2.0V, V _m from 0.8V to 2.0V | CT Devices |
| V _{CC} @ 4.5V | 10 ns/V |
| V _{CC} @ 5.5V | 8 ns/V |
| Aleke A One led then detect ante to | |

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

| | Parameter | | 74 | AC | 54AC | 74AC | all and | |
|-----------------|----------------------------------|---------------------|------------------------|----------------------|-----------------------------------|---------------------------------|---------|--|
| Symbol | | V _{CC} (V) | T _A = +25°C | | T _A = -55°C to + 125°C | T _A = -40°C to +85°C | Units | Conditions |
| 8-8 | 3.8 3.7 | (| Тур | 0.1 | Guaranteed Li | mits 0.8 | | |
| V _{OH} | Minimum High Level | 3.0 | 2.99 | 2.9 | 2.9 | 2.9 | SUE VSS | $I_{OUT} = -50 \mu A$ |
| | Output Voltage | 4.5 | 4.49 | 4.4 | 4.4 | 4.4 | V | |
| | | 5.5 | 5.49 | 5.4 | 5.4 | 5.4 | 40.5 | Capacitani |
| | 87) | 3.0 4.5 5.5 | 0 | 2.56 3.86 4.86 | 2.4 3.7 4.7 | 2.46 3.76 4.76 | V | $^*V_{\text{IN}} = V_{\text{IL}} \text{ or } V_{\text{IH}}$ -12 mA $I_{\text{OH}} -24 \text{ mA}$ -24 mA |
| ., | 76. | | 0.000 | | | Jennesses 14 | D(II) | |
| VOL | Maximum Low Level | 3.0 | 0.002 | 0.1 | 0.1 | 0.1 | 09 | $I_{OUT} = 50 \mu\text{A}$ |
| | Output Voltage | 4.5 5.5 | 0.001 | 0.1 | 0.1 | | 90 V | |
| | | 5.5 | 0.001 | 0.1 | 0.1 | 0.1 | | |
| | | 3.0 | | 0.36 | 0.5 | 0.44 | | $^*V_{IN} = V_{IL} \text{ or } V_{IH}$ 12 mA |
| | | 4.5 | | 0.36 | 0.5 | 0.44 | V | I _{OL} 24 mA |
| | | 5.5 | | 0.36 | 0.5 | 0.44 | | 24 mA |
| I _{IN} | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | ±1.0 | μΑ | $V_I = V_{CC}$, GND |
| V _{t+} | Maximum Positive | 3.0 | 2.2 | | 2.2 | | | T _A = Worst Case |
| | Threshold | 4.5 | 3.2 | 2.0 | 3.2 | 2.0 | V | |
| | | 5.5 | 3.9 | | 3.9 | | | |
| V_{t-} | Minimum Negative | 3.0 | 0.5 | | 0.5 | | | T _A = Worst Case |
| | Threshold | 4.5 | 0.9 | 0.8 | 0.9 | 0.8 | V | |
| | | 5.5 | 1.1 | | 1.1 | | | |

DC Characteristics for 'AC Family Devices (Continued)

| | | | | | 54AC | 74AC | Units | paosea vyteria ff |
|---------------------|-------------------------------------|---------------------|------------------------|------------|-----------------------------------|---------------------------------|-----------|------------------------------|
| Symbol | | V _{CC} (V) | | | T _A = -55°C to + 125°C | T _A = -40°C to +85°C | | Conditions |
| | | | Тур | patioV luc | Guaranteed Li | mits | rent (lik | DC arout Dioge Cu |
| V _{h(max)} | Maximum Hysteresis | 3.0 | 1.2 | stic Volta | 1.2 | | | T _A = Worst Case |
| | | 4.5 | 1.4 | 1.2 | 1.4 | V of V6.0 1.2 | V | Alegalia Visieni CO |
| 0.58 | -40°C to | 5.5 | 1.6 | PARCHAGE | 1.6 | | | |
| V _{h(min)} | Minimum Hysteresis | 3.0 | 0.3 | DAMOLAG | 0.3 | 3.7% | | T _A = Worst Case |
| 0.921 | | 4.5 | 0.4 | 0.4 | 0.4 | 0.4 | V | $E_0 + n_0 V = 0 V$ |
| 0.000 | | 5.5 | 0.5 | 9104 | 0.5 | ot of Va.0 | (04) | egatioV fu quiO .OO |
| I _{OLD} | †Minimum Dynamic | 5.5 | Tills9 bi | n pairl in | 50 | 75 | mA | V _{OLD} = 1.65V Max |
| I _{OHD} | Output Current | 5.5 | E (Epolov ent euros | (Note 2) (| -50 | -75 | mA | V _{OHD} = 3.85V Min |
| ICC | Maximum Quiescent Supply Current | 5.5 | 7 61 -80 | 4.0 | 80.0 | 40.0 | μА | $V_{IN} = V_{CC}$ or GND |

^{*}All outputs loaded; thresholds on input associated with output under test.

AC Electrical Characteristics

| | | | | 74AC | | 54 | AC | 74 | AC | | |
|------------------|-------------------|------------|-----------------------|--|--------------|---|--------------|--|--------------|-------|-------------|
| Symbol | Parameter **** | | V _{CC} * (V) | $T_A = +25^{\circ}C$ $C_L = 50 \text{ pF}$ | | $T_A = -55^{\circ}C$ to $+125^{\circ}C$ $C_L = 50 pF$ | | $T_{A} = -40^{\circ}C$ to $+85^{\circ}C$ $C_{L} = 50 \text{ pF}$ | | Units | Fig. No. |
| | | | Min | Тур | Max | Min | Max | Min | Max | | 100.00 |
| t _{PLH} | Propagation Delay | 3.3 5.0 | 1.5 1.5 | 9.5 7.0 | 13.5 10.0 | 1.0 1.0 | 16.0 12.0 | 1.5 1.5 | 15.0 11.0 | ns | 2-5 |
| t _{PHL} | Propagation Delay | 3.3 5.0 | 1.5 1.5 | 7.5 6.0 | 11.5 8.5 | 1.0 1.0 | 14.0 10.0 | 1.5 1.5 | 13.0 9.5 | ns | 2-5 |

^{*}Voltage Range 3.3 is 3.3V ± 0.3 V Voltage Range 5.0 is 5.0V ± 0.5 V

| Symbol | Parameter | AC/ACT | Units | Conditions | |
|-----------------|-------------------------------|--------|-------|-----------------|--|
| No24 | V 83.8 | Тур | 96.8 | | |
| CIN | Input Capacitance | 4.5 | pF | $V_{CC} = 5.0V$ | |
| C _{PD} | Power Dissipation Capacitance | 25.0 | pF | $V_{CC} = 5.0V$ | |

[†]Maximum test duration 2.0 ms, one output loaded at a time.

Note: $I_{|N}$ and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC} . I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.



54AC/74AC20 Dual 4-Input NAND Gate

General Description

The 'AC20 contains four 4-input NAND gates.

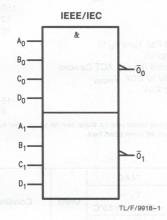
Features

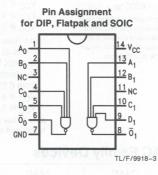
■ Outputs source/sink 24 mA

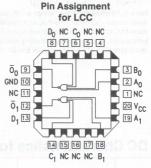
Ordering Code: See Section 5

Logic Symbol

Connection Diagrams







TL/F/9918-2

| Pin Names | Description |
|---|-------------|
| A _m , B _n , C _n , D _n | Inputs 38.0 |
| \overline{O}_n | Outputs |

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| -0.5V to +7.0V |
|-----------------------------------|
| 0.57 to 17.57 |
| |
| -20 mA |
| + 20 mA |
| -0.5 V to $V_{CC}+0.5$ V |
| |
| -20 mA |
| + 20 mA |
| -0.5 V to to V_{CC} + 0.5 V |
| |
| ±50 mA |
| |
| |

Storage Temperature (T_{STG}) -65°C to $+150^{\circ}\text{C}$ Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

per Output Pin (I_{CC} or I_{GND})

Recommended Operating Conditions

Supply Voltage (Vcc)

Input Rise and Fall Time (tr, tf)

(Except Schmitt Inputs) 'ACT Devices V_{IN} from 0.8V to 2.0V, V_{meas} from 0.8V to 2.0V V_{CC} @ 4.5V

(Note 2) (Typical)

| Supply voltage (vCC) | |
|---|-----------------------|
| 'AC | 2.0V to 6.0V |
| 'ACT | 4.5V to 5.5V |
| Input Voltage (V _I) | 0V to V _{CC} |
| Output Voltage (V _O) | 0V to V _{CC} |
| Operating Temperature (T _A) | |
| 74AC/ACT | -40°C to +85°C |
| 54AC/ACT | -55°C to +125°C |
| Junction Temperature (T _J) | |
| CDIP | 175°C |
| PDIP a solos control | 140°C |
| Input Rise and Fall Time (t _r , t _f) | |
| (Note 2) (Typical) | |
| (Except Schmitt Inputs) 'AC Devices | |
| V _{IN} from 30% to 70% of V _{CC} | |
| V _{CC} @ 3.0V | 150 ns/V |
| V _{CC} @ 4.5V | 40 ns/V |
| V _{CC} @ 5.5V | 25 ns/V |

V_{CC} @ 5.5V 8 ns/V **Note 2:** See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

10 ns/V

DC Characteristics for 'AC Family Devices

| | | | 74 | AC | 54AC | 74AC | | | |
|-----------------|--------------------------------------|------------------------|-------------------------|----------------------|----------------------------------|---------------------------------|-----------------|--|--|
| Symbol | Parameter | V _{CC} (V) | T _A = +25°C | | T _A = -55°C to +125°C | T _A = -40°C to +85°C | Units | Conditions | |
| | | | Тур | | Guaranteed Li | mits | | | |
| V _{IH} | Minimum High Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | 98 V M 8 | V _{OUT} = 0.1V or V _{CC} - 0.1V | |
| V _{IL} | Maximum Low Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | V | V _{OUT} = 0.1V or V _{CC} - 0.1V | |
| V _{OH} | Minimum High Level Output Voltage | 3.0 4.5 5.5 | 2.99 4.49 5.49 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | V | $I_{OUT} = -50 \mu A$ | |
| | | 3.0 4.5 5.5 | | 2.56 3.86 4.86 | 2.4 3.7 4.7 | 2.46 3.76 4.76 | V | $\begin{tabular}{ll} *V_{\text{IN}} &= V_{\text{IL}} \text{ or } V_{\text{IH}} \\ &- 12 \text{ mA} \\ &- 24 \text{ mA} \\ &- 24 \text{ mA} \\ \end{tabular}$ | |
| V _{OL} | Maximum Low Level Output Voltage | 3.0 4.5 5.5 | 0.002 0.001 0.001 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | V | I _{OUT} = 50 μA | |
| | | 3.0 4.5 5.5 | | 0.36 0.36 0.36 | 0.5 0.5 0.5 | 0.44 0.44 0.44 | V | $*V_{IN} = V_{IL} \text{ or } V_{IH}$ 12 mA I_{OL} 24 mA 24 mA | |
| I _{IN} | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | ±1.0 | μА | $V_{I} = V_{CC}$, GND | |

±50 mA

DC Characteristics for 'AC Family Devices (Continued)

| Symbol | Parameter | | 74. | AC | 54AC | 74AC | looi | | |
|------------------|-------------------------------------|---------------------|------------------------|-----|----------------------------------|---------------------------------|------------|--|--|
| | | V _{CC} (V) | T _A = +25°C | | T _A = -55°C to +125°C | T _A = -40°C to +85°C | Units | Conditions | |
| | | | Тур | | Guaranteed Li | mits | St. Parket | and the state of t | |
| I _{OLD} | †Minimum Dynamic Output Current | 5.5 | | | 50 | 75 | mA | V _{OLD} = 1.65V Max | |
| I _{OHD} | | 5.5 | | | -50 | -75 | mA | V _{OHD} = 3.85V Min | |
| Icc | Maximum Quiescent Supply Current | 5.5 | (sink 24 | 4.0 | 80.0 | 40.0 | μА | $V_{IN} = V_{CC}$ or GND | |

^{*}All outputs loaded; thresholds on input associated with output under test.

AC Electrical Characteristics

| Symbol | | | | 74AC | | 54 | AC | 74 | AC | | |
|------------------|-------------------|-------------------|--|------------|------------|------------|--|-----|--|----|----------------|
| | Parameter | V _{CC} * | T _A = +25°C C _L = 50 pF | C = 50 pF | | to + | T _A = -55°C to + 125°C C _L = 50 pF | | $T_A = -40^{\circ}C$ to $+85^{\circ}C$ $C_L = 50 pF$ | | Fig. No. |
| | CMM MM | | Min | Тур | Max | Min | Max | Min | Max | | 0 ⁶ |
| t _{PLH} | Propagation Delay | 3.3 5.0 | 2.0 1.5 | 6.0 5.0 | 8.5 7.0 | 1.0 1.0 | 11.0 8.5 | 1.5 | 10.0 8.0 | ns | 2-5 |
| t _{PHL} | Propagation Delay | 3.3 5.0 | 1.5 1.5 | 5.0 4.0 | 7.0 6.0 | 1.0 1.0 | 10.5 7.0 | 1.0 | 9.0 7.0 | ns | 2-5 |

^{*}Voltage Range 3.3 is 3.3V ± 0.3 V Voltage Range 5.0 is 5.0V ± 0.5 V

| Symbol | Parameter | AC/ACT | Units | Conditions | |
|-----------------|----------------------------------|--------|-------|-----------------|--|
| Symbol | raiametei | Тур | Onits | | |
| C _{IN} | Input Capacitance | 4.5 | pF | $V_{CC} = 5.0V$ | |
| C _{PD} | Power Dissipation Capacitance | 40.0 | pF | $V_{CC} = 5.0V$ | |

[†]Maximum test duration 2.0 ms, one output loaded at a time.

Note : I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC} . I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.



54AC/74AC32 • 54ACT/74ACT32 Quad 2-Input OR Gate

General Description

The 'AC/'ACT32 contains four, 2-input OR gates.

Features

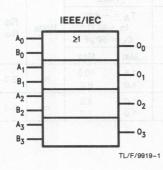
- Outputs source/sink 24 mA
- 'ACT32 has TTL-compatible inputs

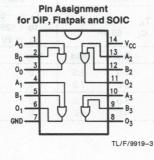
The information for the 'ACT32 is Advanced Information only.

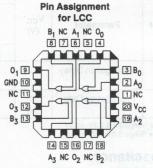
Ordering Code: See Section 5

Logic Symbol

Connection Diagrams







TL/F/9919-2

| Pin Names | Description |
|---------------------------------|-------------|
| A _n , B _n | Inputs |
| On | Outputs |

Absolute Maximum Rating (Note 1) Recommended Operating

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Supply Voltage (V _{CC}) | -0.5V to $+7.0$ V |
|---|-------------------------------|
| DC Input Diode Current (I _{IK}) | |
| $V_1 = -0.5V$ | -20 mA |
| $V_I = V_{CC} + 0.5V$ | + 20 mA |
| DC Input Voltage (V _I) | -0.5 V to $V_{CC} + 0.5$ V |
| DC Output Diode Current (I_{OK}) $V_O = -0.5V$ | -20 mA |
| $V_O = V_{CC} + 0.5V$ | + 20 mA |
| DC Output Voltage (V _O) | $-0.5V$ to to $V_{CC} + 0.5V$ |
| DC Output Source | |
| or Sink Current (IO) | \pm 50 mA |
| DC V _{CC} or Ground Current | |
| | |

Storage Temperature (T_{STG}) -65°C to +150°C Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

per Output Pin (I_{CC} or I_{GND})

Conditions

typical input rise and fall times noted here.

| Supply Voltage (V _{CC}) 'AC 'ACT | | 2.0V | to 6.0V |
|--|-----------|-------------------------------|--------------------|
| Input Voltage (V _I) | | | to V _{CC} |
| Output Voltage (V _O) | | VO Minimum Dynamio | |
| Operating Temperatur | | Output Current | 10 100 |
| 74AC/ACT | e (1A) | -40°C to | +85°C |
| 54AC/ACT | | -55°C to | |
| Junction Temperature | (Ta) | Supply Gunent | |
| | | | 175°C |
| PDIP and a te bet | | | 140°C |
| (Note 2) (Typical) (Except Schmitt Inn | uts) 'A | /cc 113 143 113 30 11 | |
| Input Rise and Fall Ti (Note 2) (Typical) (Except Schmitt Inp V _{IN} from 0.8V to 2.0 from 0.8V to 2.0V | uts) 'A | CT Devices eas | Symbol HU9 |
| V _{CC} @ 4.5V | | | 10 ns/V |
| V _{CC} @ 5.5V | 3.8 | Propagation Dalay | 8 ns/V |
| Note 2: See individual data | isneets f | or those devices which differ | from the |

DC Characteristics for 'AC Family Devices

| | Parameter and | | 74 | AC | 54AC | 74AC | 90 | Capacitani | |
|-----------------|--------------------------------------|------------------------|-------------------------|----------------------|-----------------------------------|---------------------------------|-------------------|---|--|
| Symbol | | V _{CC} (V) | T _A = +25°C | | T _A = -55°C to + 125°C | T _A = -40°C to +85°C | Units | Conditions | |
| | VO | 2 = 0- | Тур | ac | Guaranteed Li | mits | uril . | ио | |
| V _{IH} | Minimum High Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | 09 80 V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{IL} | Maximum Low Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{OH} | Minimum High Level Output Voltage | 3.0 4.5 5.5 | 2.99 4.49 5.49 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | ٧ | $I_{OUT} = -50 \mu\text{A}$ | |
| | | 3.0 4.5 5.5 | | 2.56 3.86 4.86 | 2.4 3.7 4.7 | 2.46 3.76 4.76 | ٧ | *V _{IN} = V _{IL} or V _{II} -12 m/ I _{OH} -24 m/ -24 m/ | |
| V _{OL} | Maximum Low Level Output Voltage | 3.0 4.5 5.5 | 0.002 0.001 0.001 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | ٧ | $I_{OUT} = 50 \mu A$ | |
| | | 3.0 4.5 5.5 | | 0.36 0.36 0.36 | 0.5 0.5 0.5 | 0.44 0.44 0.44 | V | $*V_{IN} = V_{IL} \text{ or } V_{II}$ 12 m/ I_{OL} 24 m/ 24 m/ | |
| I _{IN} | Maximum Input Leakage Current | 5.5 | | ±0.1 | ± 1.0 | ±1.0 | μА | $V_{I} = V_{CC}$, GND | |

±50 mA

DC Characteristics for 'AC Family Devices (Continued)

| Symbol | Parameter | | 74AC T _A = +25°C | | 54AC | 74AC | ingu sub isid sid | Conditions | |
|------------------|-------------------------------------|---------------------|--------------------------------|------------|-----------------------------------|---------------------------------|----------------------|--|--|
| | | V _{CC} (V) | | | T _A = -55°C to + 125°C | T _A = -40°C to +85°C | Units | | |
| | | | Тур | postlov ju | Guaranteed Li | mits | Sid) Iner | DC Input Diode Cu | |
| I _{OLD} | †Minimum Dynamic | 5.5 | (gV) e | alloV Jugi | 50 | 75 | mA | V _{OLD} = 1.65V Max | |
| I _{OHD} | Output Current | 5.5 | defloger | J philate | -50 | -75 | mA | V _{OHD} = 3.85V Min | |
| Icc | Maximum Quiescent Supply Current | 5.5 | | 4.0 | 80.0 | 40.0 | μΑ | V _{IN} = V _{CC} or GND | |

^{*}All outputs loaded; thresholds on input associated with output under test.

AC Electrical Characteristics

| Symbol | Parameter | | 74AC T _A = +25°C C _L = 50 pF | | | 54 | 54AC | | AC | isimpi en | 7036 |
|------------------|-------------------|-----------------------|---|------------|------------|---|-------------|--|-------------|-----------|-------------|
| | | V _{CC} * | | | | $T_A = -55^{\circ}C$ to + 125°C $C_L = 50 pF$ | | $T_A = -40^{\circ}C$ to $+85^{\circ}C$ $C_L = 50 pF$ | | Units | Fig. No. |
| | | La pote) "ACT Devices | Min | Тур | Max | Min | Max | Min | Max | | |
| t _{PLH} | Propagation Delay | 3.3 5.0 | 1.5 1.5 | 7.0 5.5 | 9.0 7.5 | 1.0 1.0 | 12.0 9.0 | 1.5 1.0 | 10.0 8.5 | ns | 2-5 |
| t _{PHL} | Propagation Delay | 3.3 5.0 | 1.5 1.5 | 7.0 5.0 | 8.5 7.0 | 1.0 1.0 | 11.5 8.5 | 1.0 1.0 | 9.0 7.5 | ns | 2-5 |

^{*}Voltage Range 3.3 is 3.3V ± 0.3 V Voltage Range 5.0 is 5.0V ± 0.5 V

| Symbol | Parameter | AC/ACT | Units | Conditions | | |
|-----------------|----------------------------------|--------|-------|------------------------|--|--|
| Symbol | raidiffetei | Тур | Omto | Conditions | | |
| CIN | Input Capacitance | 4.5 | pF | $V_{CC} = 5.0V$ | | |
| C _{PD} | Power Dissipation Capacitance | 20.0 | pF | V _{CC} = 5.0V | | |

[†]Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{1N} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC} . I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.



54AC/74AC74 • 54ACT/74ACT74 **Dual D-Type Positive Edge-Triggered Flip-Flop**

General Description

The 'AC/'ACT74 is a dual D-type flip-flop with Asynchronous Clear and Set inputs and complementary (Q, Q) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. After the Clock Pulse input threshold voltage has been passed. the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.

Asynchronous Inputs:

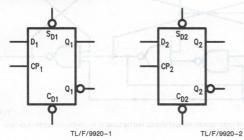
LOW input to SD (Set) sets Q to HIGH level LOW input to CD (Clear) sets Q to LOW level Clear and Set are independent of clock Simultaneous LOW on \overline{C}_D and \overline{S}_D makes both Q and \overline{Q}

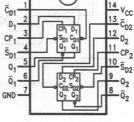
Features

- Output source/sink 24 mA
- 'ACT74 has TTL-compatible inputs

Ordering Code: See Section 5

Logic Symbols

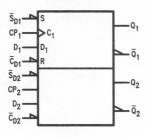




Connection Diagrams Pin Assignment for DIP, Flatpak and SOIC

TL/F/9920-4

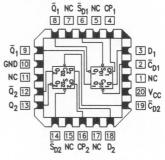
IEEE/IEC



TL/F/9920-3

| Pin Names | Description |
|--|---------------------|
| D ₁ , D ₂ | Data Inputs |
| CP ₁ , CP ₂ | Clock Pulse Inputs |
| $\overline{C}_{D1}, \overline{C}_{D2}$ | Direct Clear Inputs |
| $\overline{S}_{D1}, \overline{S}_{D2}$ | Direct Set Inputs |
| $Q_1, \overline{Q}_1, Q_2, \overline{Q}_2$ | Outputs |

Pin Assignment for LCC



TL/F/9920-5

Truth Table (Each Half)

| | Inp | uts | | Outputs | | | |
|--------------------|----------------|-------|---|---------|------------------|--|--|
| \overline{s}_{D} | Ū _D | СР | D | Q | Q | | |
| L | Н | X | X | Н | L | | |
| Н | L | X | X | L | Н | | |
| L | L | X | X | Н | Н | | |
| Н | Н | 5 | Н | Н | L | | |
| Н | Н | 5 | L | L | Н | | |
| Н | H | HELHO | X | Qo | \overline{Q}_0 | | |

H = HIGH Voltage Level

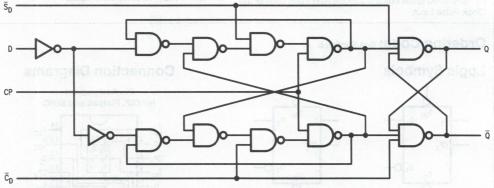
L = LOW Voltage Level

X = Immaterial

= LOW-to-HIGH Clock Transition

 $Q_0(\overline{Q}_0) = \text{Previous } Q(\overline{Q}) \text{ before LOW-to-HIGH Transition of Clock}$

Logic Diagram



TL/F/9920-6

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1) Recommended Operating

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | , p | | |
|--|---------------|------------------------|--|
| Supply Voltage (V _{CC}) | 88 - 010 0-0. | .5V to +7.0V | |
| DC Input Diode Current (I_{IK}) $V_I = -0.5V$ $V_I = V_{CC} + 0.5V$ | | −20 mA +20 mA | |
| DC Input Voltage (V _I) | -0.5V to | V _{CC} + 0.5V | |
| DC Output Diode Current (I_{OK}) $V_O = -0.5V$ $V_O = V_{CC} + 0.5V$ | | −20 mA +20 mA | |
| DC Output Voltage (V _O) | -0.5V to to | $V_{CC} + 0.5V$ | |
| DC Output Source or Sink Current (I _O) | | ±50 mA | |
| DC V _{CC} or Ground Current per Output Pin (I _{CC} or I _{GND}) | | ± 50 mA | |
| | | | |

Storage Temperature (T_{STG}) -65°C to +150°C Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

Conditions

| Supply Voltage (V _{CC}) 'AC 'ACT | 2.0V to 6.0V 4.5V to 5.5V |
|--|---|
| Input Voltage (V _I) | 0V to V _{CC} |
| Output Voltage (V _O) | 0V to V _{CC} |
| Operating Temperature (T _A) 74AC/ACT 54AC/ACT | |
| Junction Temperature (T _{.1}) | menuO ylacuS |
| CDIP | 175°C 140°C |
| (Note 2) (Typical) (Except Schmitt Inputs) '/ | , t _f) AC Devices Vcc |
| V _{CC} @ 3.0V | 150 ns/V |
| V _{CC} @ 4.5V | 40 ns/V |
| V _{CC} @ 5.5V | 25 ns/V |
| Input Rise and Fall Time (t _r (Note 2) (Typical) (Except Schmitt Inputs) '/ | ACT Devices |
| V_{IN} from 0.8V to 2.0V, V_r from 0.8V to 2.0V | |
| V _{CC} @ 4.5V | 10 ns/V |
| V _{CC} @ 5.5V | level woll reprised 8 ns/V |
| Note 2: See individual datasheets | for those devices which differ from the |

typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

| | Parameter | | 74 | AC | 54AC | 74AC | | Conditions | |
|--|--|------------------------|-------------------------|----------------------|----------------------------------|---------------------------------|---|---|--|
| Symbol | | V _{CC} (V) | T _A = | + 25°C | T _A = -55°C to +125°C | T _A = -40°C to +85°C | Units | | |
| AU | | | Тур | | Guaranteed Li | mits | opsfic | | |
| V _{IH} v to y Am AS Am AS | Minimum High Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| VIL QVID | Maximum Low Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | nuosim V.Os | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{OH} | Minimum High Level Output Voltage | 3.0 4.5 5.5 | 2.99 4.49 5.49 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | V Many Chang | $I_{OUT} = -50 \mu\text{A}$ | |
| ABSV Min | DV = VID = V | 3.0 4.5 5.5 | 32A | 2.56 3.86 4.86 | 2.4 3.7 4.7 | 2.46 3.76 4.76 | n Opiesa Sun V nt resholds o | $V_{\rm IN} = V_{\rm IL} {\rm or} V_{\rm IH}$ $-12 {\rm mA}$ $-24 {\rm mA}$ $-24 {\rm mA}$ | |
| V _{OL} | Maximum Low Level Output Voltage | 3.0 4.5 5.5 | 0.002 0.001 0.001 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | V | $I_{OUT} = 50 \mu A$ | |
| | | 3.0 4.5 5.5 | | 0.36 0.36 0.36 | 0.5 0.5 0.5 | 0.44 0.44 0.44 | ٧ | $*V_{IN} = V_{IL} \text{ or } V_{IH}$ 12 mA I_{OL} 24 mA | |
| I _{IN} | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | ±1.0 | μА | $V_{I} = V_{CC}$, GND | |

DC Characteristics for 'AC Family Devices (Continued)

| Symbol | Parameter | | 74AC T _A = +25°C | | 54AC | 74AC | alt an | Conditions | |
|------------------|-------------------------------------|---------------------|-----------------------------|------------|-----------------------------------|---------------------------------|------------|------------------------------|--|
| | | V _{CC} (V) | | | T _A = -55°C to + 125°C | T _A = -40°C to +85°C | Units | | |
| | | | Тур | egstloV te | Guaranteed Li | mits | pail) sees | DC Music Diode Gu | |
| IOLD | †Minimum Dynamic | 5.5 | fovi ar | aneV area | 50 | 75 | mA | V _{OLD} = 1.65V Max | |
| I _{OHD} | Output Current | 5.5 | U.B.R.Ch.F. | OA COAST | -50 | of V0.0-75 | mA | V _{OHD} = 3.85V Min | |
| Icc | Maximum Quiescent Supply Current | 5.5 | | 4.0 | 80.0 | 40.0 | μА | $V_{IN} = V_{CC}$ or GND | |

^{*}All outputs loaded; thresholds on input associated with output under test.

Note: $I_{|N}$ and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC} . I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

| | | | 744 | CT | 54ACT | 74ACT | epoiteration | Marte 1/ Appointer maximum | |
|-----------------------|--------------------------------------|---------------------|------------------------|--------------|----------------------------------|---------------------------------|-----------------|---|--|
| Symbol | Parameter | V _{CC} (V) | T _A = +25°C | | T _A = -55°C to +125°C | T _A = -40°C to +85°C | Units | Conditions | |
| | CT Devices | (etus | Тур | 6.Jq90X. | Guaranteed L | imits | ethunin Mr | TOAH to notisted obtain | |
| V _{IH} | Minimum High Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 2.0 2.0 | 2.0 2.0 | 2.0 2.0 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{IL} \aa 8 | Maximum Low Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 0.8 | 0.8 0.8 | 0.8 0.8 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{OH} | Minimum High Level Output Voltage | 4.5 5.5 | 4.49 5.49 | 4.4 5.4 | 4.4 5.4 | 4.4 5.4 | ٧ | $I_{OUT} = -50 \mu\text{A}$ | |
| | Mrits Cont | 4.5 5.5 | | 3.86 4.86 | 3.70 4.70 | 3.76 4.76 | ٧ | $V_{IN} = V_{IL} \text{ or } V_{IH}$ -24 mA -24 mA | |
| V _{OL} | Maximum Low Level Output Voltage | 4.5 5.5 | 0.001 0.001 | 0.1 0.1 | 0.1 0.1 | 0.1 0.1 | ٧ | $I_{OUT} = 50 \mu\text{A}$ | |
| | Tour V | 4.5 5.5 | | 0.36 0.36 | 0.50 0.50 | 0.44 0.44 | ve J dgill v | $\begin{tabular}{ll} *V_{IN} = V_{IL} \mbox{ or } V_{IH} \\ I_{OL} & 24 \mbox{ mA} \\ 24 \mbox{ mA} \\ \end{tabular}$ | |
| I _{IN} Vito | Maximum Input Leakage Current | 5.5 | | ±0.1 | 8.0 18.1 ±1.0 88.1 | 0,8 88.5 ± 1.0 B | μΑ | $V_I = V_{CC}$, GND | |
| ICCT Au 03 | Maximum I _{CC} /Input | 5.5 | 0.6 | | 1.6 gg | ges 1.5 _{0.8} | mA | $V_{\rm I} = V_{\rm CC} - 2.1V$ | |
| lold | †Minimum Dynamic | 5.5 | | | 50 | 75 | mA | V _{OLD} = 1.65V Max | |
| IOHD | Output Current | 5.5 | | | -50 | -75 | mA | V _{OHD} = 3.85V Min | |
| Icc St Am AS | Maximum Quiescent Supply Current | 5.5 | | 4.0 | 80.0 | 40.0 | μА | V _{IN} = V _{CC} or GND | |

^{*}All outputs loaded; thresholds on input associated with output under test.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

[†]Maximum test duration 2.0 ms, one output loaded at a time.

[†]Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics

| | PARCT | 75 | 848 | 74AC | TOART | 54 | AC | 74 | AC | | |
|------------------|---|-------------------|------------|--|--------------|---|--------------|--|--------------------|-------|-------------|
| Symbol | Parameter | V _{CC} * | | T _A = +25°C C _L = 50 pF | | $T_A = -55^{\circ}C$ to $+125^{\circ}C$ $C_L = 50 pF$ | | $T_A = -40^{\circ}C$ to $+85^{\circ}C$ $C_L = 50 pF$ | | Units | Fig. No. |
| | | xall nile | KSAT | Min | Тур | Max | Min | Max | Min | Max | |
| f _{max} | Maximum Clock Frequency | 3.3 5.0 | 100 140 | 125 160 | 210 | 70 95 | 5.0 | 95 125 | mum Glad Leincy | MHz | 2-3 |
| t _{PLH} | Propagation Delay \overline{C}_{Dn} or \overline{S}_{Dn} to Q_n or \overline{Q}_n | 3.3 5.0 | 5.0 3.5 | 8.0 6.0 | 12.0 9.0 | 1.0 1.0 | 13.0 9.5 | 4.0 | 13.0 10.0 | ns | 2-6 |
| t _{PHL} | Propagation Delay \overline{C}_{Dn} or \overline{S}_{Dn} to Q_n or \overline{Q}_n | 3.3 5.0 | 4.0 3.0 | 10.5 8.0 | 12.0 9.5 | 1.0 1.0 | 14.0 10.5 | 3.5 2.5 | 13.5 10.5 | ns | 2-6 |
| t _{PLH} | Propagation Delay CP_n to Q_n or \overline{Q}_n | 3.3 5.0 | 4.5 3.5 | 8.0 6.0 | 13.5 10.0 | 1.0 1.0 | 17.5 12.0 | 4.0 3.0 | 16.0 10.5 | ns | 2-6 |
| tpHL | Propagation Delay CP_n to Q_n or \overline{Q}_n | 3.3 5.0 | 3.5 2.5 | 8.0 6.0 | 14.0 10.0 | 1.0 1.0 | 13.5 10.0 | 3.5 2.5 | 14.5 10.5 | ns | 2-6 |

*Voltage Range 3.3 is 3.3V \pm 0.3V

Voltage Range 5.0 is 5.0V ± 0.5V

AC Operating Requirements

| | 5% 47 5% | 7 | 74 | AC | 54AC | 74AC | | |
|------------------|---|--------------------------|-----------------------------------|------------|---|--|-------|-------------|
| Symbol | Parameter | V _{CC} * (V) | T _A = C _L = | | T _A = -55°C to +125°C C _L = 50 pF | T _A = -40°C to +85°C C _L = 50 pF | Units | Fig. No. |
| | | | Тур | | Guaranteed Min | imum | Jan. | |
| ts | Set-up Time, HIGH or LOW D _n to CP _n | 3.3 5.0 | 1.5 1.0 | 4.0 3.0 | 5.0 4.0 | 4.5 3.0 | ns | 2-9 |
| th | Hold Time, HIGH or LOW D _n to CP _n | 3.3 5.0 | -2.0 -1.5 | 0.5 0.5 | 0.5 0.5 | 0.5 0.5 | ns | 2-9 |
| t _w | CP_n or $\overline{\operatorname{C}}_{\operatorname{Dn}}$ or $\overline{\operatorname{S}}_{\operatorname{Dn}}$ Pulse Width | 3.3 5.0 | 3.0 2.5 | 5.5 4.5 | 8.0 5.5 | 7.0 5.0 | ns | 2-6 |
| t _{rec} | Recovery Time \$\overline{\overline{C}_{Dn}}\$ or \$\overline{S}_{Dn}\$ to \$\overline{CP}\$ | 3.3 5.0 | -2.5 -2.0 | 0 | 0.5 0.5 | 90 nd 8 | ns | 2-9 |

*Voltage Range 3.3 is 3.3V ±0.3V

Voltage Range 5.0 is 5.0V ± 0.5 V

AC Electrical Characteristics

| | 7440 | 0 | | 74ACT | | 54/ | ACT | 74 | ACT | | |
|------------------|--|--------------------------|-----|-----------------------|------|------|-------------------------|------|------------------------|-------|------|
| Symbol | Parameter | V _{CC} * (V) | | C _L = +25° | | to + | -55°C 125°C 50 pF | to + | -40°C 85°C 50 pF | Units | Fig. |
| | koM nilä | xeM | Min | Тур | Max | Min | Max | Min | Max | | |
| f _{max} | Maximum Clock Frequency | 5.0 | 145 | 210 | 185 | 85 | 3.8 | 125 | imum Otok Nency | MHz | 2-3 |
| t _{PLH} | Propagation Delay \overline{C}_{Dn} or \overline{S}_{Dn} to \overline{Q}_n or \overline{Q}_n | 5.0 | 3.0 | 5.5 | 9.5 | 1.0 | 11.5 | 2.5 | 10.5 | ns | 2-6 |
| tPHL | Propagation Delay \overline{C}_{Dn} or \overline{S}_{Dn} to \overline{Q}_n or \overline{Q}_n | 5.0 | 3.0 | 6.0 | 10.0 | 1.0 | 12.5 | 3.0 | 11.5 | ns | 2-6 |
| t _{PLH} | Propagation Delay CP_n to Q_n or \overline{Q}_n | 5.0 | 4.0 | 7.5 | 11.0 | 1.0 | 14.0 | 4.0 | 13.0. | ns | 2-6 |
| t _{PHL} | Propagation Delay CP_n to Q_n or \overline{Q}_n | 5.0 | 3.5 | 6.0 | 10.0 | 1.0 | 12.0 | 3.0 | 11.5 | ns | 2-6 |

^{*}Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

| | | | 74A | СТ | 54ACT | 74ACT | No. of the second second | 100000 |
|------------------|--|--------------------------|-----------------------------------|-----|--|--|--------------------------|-------------|
| Symbol | Parameter Order | V _{CC} * (V) | T _A = C _L = | | T _A = -55°C to + 125°C C _L = 50 pF | $T_A = -40^{\circ}C$ $to +85^{\circ}C$ $C_L = 50 pF$ | Units | Fig. No. |
| | 70 8 3 = 40, 1 70 (| 9 = 70 | Тур | | Guaranteed Min | imum | | |
| ts | Set-up Time, HIGH or LOW D _n to CP _n | 5.0 | 1.0 | 3.0 | 4.0 WO | 10 HO 3.5 | ns | 2-9 |
| th | Hold Time, HIGH or LOW D _n to CP _n | 5.0 | -0.5 | 1.0 | 1.0 | 1.0 hall an T | ns | 2-9 |
| t _w | CP _n or \overline{C}_{Dn} or \overline{S}_{Dn} Pulse Width | 5.0 | 3.0 | 5.0 | 7.0 | 6.0 | ns | 2-6 |
| t _{rec} | Recovery Time C D n or or or or or or or or or | 5.0 | -2.5 | 0 | 0.5 | e Widdle | ns | 2-9 |

^{*}Voltage Range 5.0 is 5.0V ±0.5V

| Symbol | Parameter | AC/ACT | Units | Conditions |
|-----------------|----------------------------------|--------|--------|-----------------|
| Зушьог | Farameter | Тур | Office | Conditions |
| C _{IN} | Input Capacitance | 4.5 | pF | $V_{CC} = 5.0V$ |
| C _{PD} | Power Dissipation Capacitance | 35.0 | pF | $V_{CC} = 5.0V$ |





54AC/74AC85 • 54ACT/74ACT85 4-Bit Magnitude Comparator

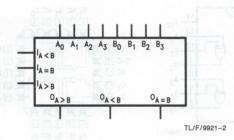
General Description

The 'AC/'ACT85 is a high speed, expandable 4-bit magnitude comparator which compares two 4-bit words in any monotonic code (binary, BCD or other) and generates three outputs: A less than B, A greater than B, and A equal to B. Three expansion inputs allow serial (ripple) expansion over any word length without external gates.

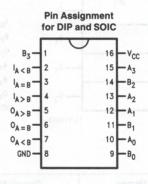
Features

- Easily expandable
- Binary or BCD comparison
- A > B, A < B, A = B output available
- 'ACT85 has TTL-compatible inputs

Logic Symbol



Connection Diagram



TL/F/9921-1

| Pin Names | Description |
|--------------------------------|-------------------------------|
| A ₀ -A ₃ | Word A Inputs |
| B ₀ -B ₃ | Word B Inputs |
| $I_A = B$ | A = B Expansion Input |
| $I_A < B, I_A > B$ | A < B, A > B Expansion Inputs |
| $O_A > B$ | A Greater Than B Output |
| O _A < B | A Less Than B Output |
| $O_A = B$ | A Equal B Output |



54AC/74AC86 Quad 2-Input Exclusive-OR Gate

General Description

Features

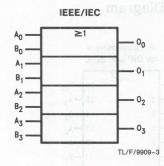
The AC/ACT 86 contains four, 2-input exclusive-OR gates.

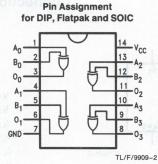
Outputs source/sink 24 mA

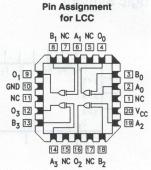
Ordering Code: See Section 5

Logic Symbol

Connection Diagrams







TL/F/9909-1

| Pin Names | Description | | |
|--------------------------------|-------------|--|--|
| A ₀ -A ₃ | Inputs | | |
| B ₀ -B ₃ | Inputs | | |
| O ₀ -O ₃ | Outputs | | |

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Office/ Distributors for av | anability and specifications. |
|--|---------------------------------|
| Supply Voltage (V _{CC}) | -0.5V to +7.0V |
| DC Input Diode Current (I _{IK}) | StimU bestmann |
| $V_{I} = 0.5V$ | -20 mA |
| $V_1 = V_{CC} + 0.5V$ | + 20 mA |
| DC Input Voltage (V _I) | -0.5V to V _{CC} +0.5V |
| DC Output Diode Current (I | ок) |
| $V_0 = -0.5V$ | -20 mA |
| $V_O = V_{CC} + 0.5V$ | + 20 mA |
| DC Output Voltage (V _O) | -0.5 V to $V_{CC} + 0.5$ V |
| DC Output Source or Sink C | urrent (I _O) ±50 mA |
| DC V _{CC} or Ground Current | |
| Per Output Pin (I _{CC} or I _{GN} | D) ± 50 mA |
| | |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

-65°C to +150°C

Storage Temperature (T_{STG})

Recommended Operating Conditions

| Supply Voltage (V _{CC}) | 2011-2011 |
|---|--|
| 'AC 'ACT | 2.0V to 6.0V 4.5V to 5.5V |
| Input Voltage (V _I) | 0V to V _{CC} |
| Output Voltage (V _O) | 0V to V _{CC} |
| Operating Temperature | (T _A) memu0 epskaal |
| 74AC/ACT 54AC/ACT | -40°C to +85°C -55°C to +125°C |
| Junction Temperature (| (T _J) |
| CDIP | obmanyO rauraidM/ 175°C |
| CDIP | 140°C |
| Input Rise and Fall Tim (Note 2) (Typical) (Except Schmitt Inpu | ts) 'AC Devices |
| | % of VCC no ablanteams charles are also less |
| | and the first sense are used to 150 ns/V |
| 00 | 40 ns/V |
| .00 | ANT OF RECEIVED AND RESERVED AN |
| Input Rise and Fall Tim (Note 2) (Typical) | Mississi Caleottical CA |
| (Except Schmitt Input V _{IN} from 0.8V to 2.0V | |
| from 0.8V to 2.0V V _{CC} @ 4.5V V _{CC} @ 5.5V | 10 ns/V 8 ns/V |
| | |

Note 2: See individual datasheets for those devices which differ from the

typical input and fall times noted here.

DC Characteristics for 'AC Family Devices

| Symbol | Parameter | | 74 | AC | 54AC | 74AC | eC note | laru Propac |
|-----------------|--------------------------------------|-------------------|-------------------------|----------------------|-----------------------------------|---------------------------------|------------|--|
| | | V _{CC} | T _A = 25°C | | T _A = -55°C to + 125°C | T _A = -40°C to +85°C | Units | Conditions |
| | | | Тур | | Guaranteed L | imits | L0: V0.6:4 | Voltage Range 6.0V |
| V _{IH} | Minimum High Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ |
| V _{IL} | Maximum Low Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | io V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ |
| V _{OH} | Minimum High Level Output Voltage | 3.0 4.5 5.5 | 2.99 4.49 5.49 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | ٧ | $I_{OUT} = -50 \mu\text{A}$ |
| | | 3.0 4.5 5.5 | | 2.56 3.86 4.86 | 2.4 3.7 4.7 | 2.46 3.76 4.76 | ٧ | $*V_{IN} = V_{IL} \text{ or } V_{IH} - 12 \text{ m/} - 12 \text{ m/} - 24 $ |
| V _{OL} | Maximum Low Level Output Voltage | 3.0 4.5 5.5 | 0.002 0.001 0.001 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | ٧ | I _{OUT} = 50 μA |
| | | 3.0 4.5 5.5 | | 0.36 0.36 0.36 | 0.50 0.50 0.50 | 0.44 0.44 0.44 | ٧ | $*V_{IN} = V_{IL} \text{ or } V_{IH}$ 12 mA $I_{OL} \qquad 24 \text{ mA}$ 24 mA |

*All outputs loaded; thresholds on input associated with output under test.

[†]Maximum test duration 20 ms, one output loaded at a time.

DC Characteristics for 'AC Family Devices (Continued)

| | | | 74 | 1AC | 54AC | 74AC | | please competi- | |
|------------------|-------------------------------------|---------------------|----------------------------|--------------------------|-----------------------------------|---------------------------------|-------------|--|--|
| Symbol P | Parameter | V _{CC} (V) | T _A = | = 25°C | T _A = -55°C to + 125°C | T _A = -40°C to +85°C | Units | Conditions | |
| 33V of V0 | | | Тур | Гур Guaranteed Limits | | | | DO Input Diode Obj | |
| INOVO | Maximum Input Leakage Current | 5.5 | gV) api heoma | ±0.1 | ±1.0 | ±1.0 | μА | $V_{I} = V_{CC}$, GND | |
| loz | Maximum TRI-STATE® | | | DANCA DANCA AACAAC | 8 Am 05 - | (se | ji) fiserii | V_{I} (OE) = V_{IL} , V_{IH} $V_{O} = V_{CC}$, GND | |
| I _{OLD} | †Minimum Dynamic | 5.5 | 80 4910 | 910 | 50 | 75 | mA | V _{OLD} = 1.65V Max | |
| IOHD | Output Current | 5.5 | | ale | -50 | −75 | mA | V _{OHD} = 3.85V Min | |
| ICC | Maximum Quiescent Supply Current | 5.5 | lari on solqyT swedo | 4.0 | 80 | 40 | μА | $V_{IN} = V_{CC}$ or GND | |

^{*}All outputs loaded; thresholds on input associated with output under test.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}. I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

AC Electrical Characteristics: See Section 2

| Symbol | Parameter | R (BRIGH | 1919 1919 1919 1911 1919 1919 | 74AC | | 54AC | | 74 | AC | | |
|------------------|--|-------------------|--|------------|-------------|---|--------------|--|-------------|-------|------|
| | | V _{CC} * | $egin{aligned} \mathbf{T_A} &= +25^{\circ}\mathbf{C} \\ \mathbf{C_L} &= 50\ \mathbf{pF} \end{aligned}$ | | | $T_{A}=-55^{\circ}C$ $to +125^{\circ}C$ $C_{L}=50$ pF | | $T_A = -40^{\circ}C$ to $+85^{\circ}C$ $C_L = 50 \text{ pF}$ | | Units | Fig. |
| | | se install here: | Min | Тур | Max | Min | Max | Min | Max | | |
| t _{PHL} | Propagation Delay Inputs to Outputs | 3.3 5.0 | 2.0 1.5 | 6.0 4.5 | 11.5 8.5 | 1.0 | 14.0 10.0 | 1.5 1.0 | 12.5 9.5 | ns | 2-5 |
| t _{PLH} | Propagation Delay Inputs to Outputs | 3.3 5.0 | 2.0 1.5 | 6.5 4.5 | 11.5 8.5 | 1.0 | 14.0 10.0 | 1.5 1.0 | 12.5 9.0 | ns | 2-5 |

^{*}Voltage Range 3.3V is 3.3V ± 0.3 V Voltage Range 5.0V is 5.0V ± 0.5 V

Capacitance

| Symbol | Parameter | AC/ACT | Units | Conditions | |
|-----------------|-------------------------------|--------|-------|-----------------|--|
| V(.0 == | 0.9 Vou | Тур | 0 | 8.0 8.1 | |
| CIN | Input Capacitance | 4.5 | pF | $V_{CC} = 5.0V$ | |
| C _{PD} | Power Dissipation Capacitance | 35 | pF | $V_{CC} = 5.0V$ | |

[†]Maximum test duration 20 ms, one output loaded at a time.



54AC/74AC109 • 54ACT/74ACT109 Dual JK Positive Edge-Triggered Flip-Flop

General Description

The 'AC/'ACT109 consists of two high-speed completely independent transition clocked $J\overline{K}$ flip-flops. The clocking operation is independent of rise and fall times of the clock waveform. The $J\overline{K}$ design allows operation as a D flip-flop (refer to 'AC/'ACT74 data sheet) by connecting the J and \overline{K} inputs together.

Asynchronous Inputs:

LOW input to \overline{S}_D (Set) sets Q to HIGH level LOW input to \overline{C}_D (Clear) sets Q to LOW level

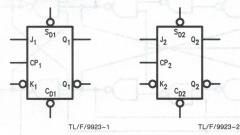
Clear and Set are independent of clock Simultaneous LOW on \overline{C}_D and \overline{S}_D makes both Q and \overline{Q}

Features

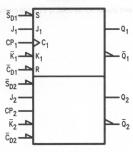
- Outputs source/sink 24 mA
- 'ACT109 has TTL-compatible inputs

Ordering Code: See Section 5

Logic Symbols



IEEE/IEC

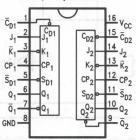


TL/F/9923-7

| Pin Names | Description |
|--|---------------------|
| $J_1, J_2, \overline{K}_1, \overline{K}_2$ | Data Inputs |
| CP ₁ , CP ₂ | Clock Pulse Inputs |
| $\overline{C}_{D1}, \overline{C}_{D2}$ | Direct Clear Inputs |
| $\overline{S}_{D1}, \overline{S}_{D2}$ | Direct Set Inputs |
| $Q_1, Q_2, \overline{Q}_1, \overline{Q}_2$ | Outputs |

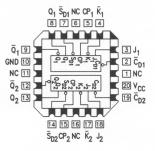
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/9923-3

Pin Assignment for LCC



TL/F/9923-4

Truth Table (each half)

| | | Inputs | | | Out | puts |
|----|-----------------|--------|---|---|----------------|------------------|
| SD | ¯c _D | СР | J | K | Q | Q |
| L | Н | X | X | X | н | L |
| Н | L | X | X | X | L | Н |
| L | L | X | X | X | Н | Н |
| Н | Н | 1 | L | L | L | Н |
| Н | Н | 5 | Н | L | Tog | ggle |
| Н | Н | 5 | L | Н | Q ₀ | \overline{Q}_0 |
| Н | Н | 5 | Н | Н | Н | L |
| H | Н | L b | X | X | Q ₀ | \overline{Q}_0 |

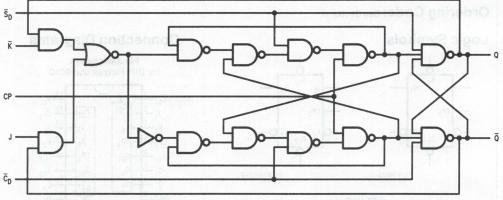
H = HIGH Voltage Level L = LOW Voltage Level

= LOW-to-HIGH Transition

X = Immaterial

 $Q_0(\overline{Q}_0)$ = Previous $Q_0(\overline{Q}_0)$ before LOW-to-HIGH Transition of Clock

Logic Diagram (one half shown)



TL/F/9923-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1) Recommended Operating

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Supply Voltage (V _{CC}) | -0.5V to + | 7.0V |
|--|--------------------------------|------|
| DC Input Diode Current (I_{IK}) $V_I = -0.5V$ $V_I = V_{CC} + 0.5V$ | |) mA |
| DC Input Voltage (V _I) | -0.5V to V _{CC} + | 0.5V |
| DC Output Diode Current (I_{OK}) $V_O = -0.5V$ $V_O = V_{CC} + 0.5V$ | |) mA |
| DC Output Voltage (V _O) | $-$ 0.5V to to V $_{\rm CC}$ + | 0.5V |
| DC Output Source or Sink Current (I _O) | ±50 |) mA |
| DC V _{CC} or Ground Current per Output Pin (I _{CC} or I _{GND}) | ±50 |) mA |
| Storage Temperature (T _{STG}) | -65°C to +15 | 50°C |
| | | |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

Conditions

| Supply Voltage (V _{CC}) 'AC 'ACT | 2.0V to 6.0V 4.5V to 5.5V |
|---|-------------------------------|
| Input Voltage (V _I) | |
| | 0V to V _{CC} |
| Output Voltage (V _O) | 0V to V _{CC} |
| Operating Temperature (T _A) 74AC/ACT | -40°C to +85°C |
| 54AC/ACT | -55°C to +125°C |
| Junction Temperature (T,) | Supply Obrent |
| CDIP | 175°C 140°C |
| Input Rise and Fall Time (t _r , 1 (Note 2) (Typical) (Except Schmitt Inputs) 'AG V _{IN} from 30% to 70% of V | t _f) C Devices |
| V _{CC} @ 3.0V | CC 150 ns/V |
| V _{CC} @ 4.5V V _{CC} @ 5.5V | 40 ns/V 25 ns/V |
| Input Rise and Fall Time (t _r , (Note 2) (Typical) (Except Schmitt Inputs) 'A | CT Devices |
| V _{IN} from 0.8V to 2.0V, V _{me} | |
| from 0.8V to 2.0V | Minimum Fight Level |
| V _{CC} @ 4.5V | egation lugal 10 ns/V |
| V _{CC} @ 5.5V | 8 ns/V |

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

| Symbol | $V = \mu_{\rm H} V^*$ | | 74 | AC | 54AC | 74AC | | |
|--|--------------------------------------|---------------------|-------------------------|----------------------|-----------------------------------|---------------------------------|-------------|---|
| | Parameter | V _{CC} (V) | T _A = | + 25°C | T _A = -55°C to + 125°C | T _A = -40°C to +85°C | Units | Conditions |
| | a - not y | | Тур | | Guaranteed Li | mits | Disposition | VOL. Maximu |
| V _{IH} H _I V 10 3 | Minimum High Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ |
| VIL | Maximum Low Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | ta Value | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ |
| V _{OH} | Minimum High Level Output Voltage | 3.0 4.5 5.5 | 2.99 4.49 5.49 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | v iii | $I_{OUT} = -50 \mu\text{A}$ |
| nim vae: | P gHOV Am ΔV = MV OMD 10 Au | 3.0 4.5 5.5 | þ | 2.56 3.86 4.86 | 2.4 3.7 4.7 | 2.46 3.76 4.76 | V | $V_{IN} = V_{IL} \text{ or } V_{IH}$ -12 mA $V_{IOH} = -24 \text{ mA}$ -24 mA |
| V _{OL} | Maximum Low Level Output Voltage | 3.0 4.5 5.5 | 0.002 0.001 0.001 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | V | I _{OUT} = 50 μA |
| | | 3.0 4.5 5.5 | | 0.36 0.36 0.36 | 0.5 0.5 0.5 | 0.44 0.44 0.44 | ٧ | $*V_{IN} = V_{IL} \text{ or } V_{IH}$ 12 mA I_{OL} 24 mA 24 mA |
| I _{IN} | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | ±1.0 | μА | $V_I = V_{CC}$, GND |

DC Characteristics for 'AC Family Devices (Continued)

| Symbol Pa | Parameter | V _{CC} (V) | 74 | AC | 54AC | 74AC | Units | oleans comman |
|-----------|-------------------------------------|---------------------|------------------|----------------------|-----------------------------------|---------------------------------|-------|------------------------------|
| | | | T _A = | + 25°C | T _A = -55°C to + 125°C | T _A = -40°C to +85°C | | Conditions |
| | /0 | | Тур | gatio V tu | Guaranteed Li | mits | | uO ebc/G turnit DG |
| IOLD | †Minimum Dynamic | 5.5 | (OV) eq | cut Voite | 50 | 75 | mA | V _{OLD} = 1.65V Max |
| IOHD | Output Current | 5.5 | 15/G(t) | SUBGILLE TORY DAY | -50 | 00 V∂.0−75 | mA (| V _{OHD} = 3.85V Min |
| Icc | Maximum Quiescent Supply Current | 5.5 | | 4.0 | 80.0 | 40.0 | μА | $V_{IN} = V_{CC}$ or GND |

^{*}All outputs loaded; thresholds on input associated with output under test.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

| | Parameter | | 74 | ACT | 54ACT | 74ACT | agniles mi | more in Absolute move |
|----------------------|--------------------------------------|------------------------|------------------------|--------------|-----------------------------------|--------------------|------------|--|
| Symbol | | V _{CC} (V) | T _A = +25°C | | T _A = -55°C to + 125°C | | Units | Conditions |
| | CT Devices | A' (etu | Тур | | Guaranteed Lin | nits | 0.000 | CONTRACTOR DESIGNATION DESIGNA |
| V _{IH} | Minimum High Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 2.0 | 2.0 2.0 | 2.0 2.0 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ |
| V _{IL} | Maximum Low Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 0.8 | 0.8 0.8 | 0.8 0.8 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ |
| V _{OH} | Minimum High Level Output Voltage | 4.5 5.5 | 4.49 5.49 | 4.4 5.4 | 4.4 5.4 | 4.4 5.4 5.4 | V | $I_{OUT} = -50 \mu\text{A}$ |
| | Sec Units Com | 4.5 5.5 | T 226 | 3.86 4.86 | 3.70 4.70 | 3.76 4.76 | Vien | $V_{IN} = V_{IL} \text{ or } V_{IH}$ -24 mA -24 mA |
| V _{OL} | Maximum Low Level Output Voltage | 4.5 5.5 | 0.001 0.001 | 0.1 0.1 | 0.1 0.1 | 0.1 0.1 | ٧ | $I_{OUT} = 50 \mu\text{A}$ |
| | 1.00V | 4.5 5.5 | | 0.36 0.36 | 0.50 0.50 | 0.44 0.44 | V | $*V_{IN} = V_{IL} \text{ or } V_{IH}$ I_{OL} 24 mA 24 mA |
| I _{IN} VI.0 | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | 89.9 ±1.0 | μА | V _I = V _{CC} , GND |
| ГССТ | Maximum I _{CC} /Input | 5.5 | 0.6 | | 1.6 | 00 S 1.5 0 H | mA | $V_{\rm I} = V_{\rm CC} - 2.1V$ |
| lold | †Minimum Dynamic | 5.5 | | | 50 | 04.8 75 8.8 | mA | V _{OLD} = 1.65V Max |
| IOHD | Output Current | 5.5 | | | -50 | -75 | mA | V _{OHD} = 3.85V Min |
| lcc | Maximum Quiescent Supply Current | 5.5 | | 4.0 | 80.0 | 40.0 | μΑ | V _{IN} = V _{CC} or GND |

^{*}All outputs loaded; thresholds on input associated with output under test.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

[†]Maximum test duration 2.0 ms, one output loaded at a time.

[†]Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics

| | PARCT | TO | Ass | 74AC | TOART | 54 | AC | 74 | AC | | |
|------------------|---|--------------------------|--|-------------|--------------|---|--------------|--|--------------------|-------|------|
| Symbol | Parameter | V _{CC} * (V) | T _A = +25°C C _L = 50 pF | | | $T_A = -55^{\circ}C$ to $+125^{\circ}C$ $C_L = 50 pF$ | | $T_A = -40^{\circ}C$ to $+85^{\circ}C$ $C_L = 50 pF$ | | Units | Fig. |
| | soft dilâ | XAM | Min | Тур | Max | Min | Max | Min | Max | | |
| f _{max} | Maximum Clock Frequency | 3.3 5.0 | 125 150 | 150 175 | 210 | 65 95 | 0.6 | 100 10 125 | amum Cle quency | MHz | 2-3 |
| t _{PLH} | Propagation Delay CP_n to Q_n or \overline{Q}_n | 3.3 5.0 | 4.0 2.5 | 8.0 6.0 | 13.5 10.0 | 1.0 1.0 | 17.5 12.0 | 3.5 2.0 | 16.0 10.5 | ns | 2-6 |
| t _{PHL} | Propagation Delay CP_n to Q_n or \overline{Q}_n | 3.3 5.0 | 3.0 2.0 | 8.0 6.0 | 14.0 10.0 | 1.0 | 13.5 10.0 | 3.0 1.5 | 14.5 10.5 | ns | 2-6 |
| t _{PLH} | Propagation Delay $\overline{\mathbb{C}}_{Dn}$ or $\overline{\mathbb{S}}_{Dn}$ to \mathbb{Q}_n or $\overline{\mathbb{Q}}_n$ | 3.3 5.0 | 3.0 2.5 | 8.0 6.0 | 12.0 9.0 | 1.0 1.0 | 13.0 9.5 | 2.5 | 13.0 10.0 | ns | 2-6 |
| t _{PHL} | Propagation Delay \overline{C}_{Dn} or \overline{S}_{Dn} to Q_n or \overline{Q}_n | 3.3 5.0 | 3.0 2.0 | 10.0 7.5 | 12.0 9.5 | 1.0 1.0 | 14.0 10.5 | 3.0 2.0 | 13.5 10.5 | ns | 2-6 |

^{*}Voltage Range 3.3 is 3.3V ± 0.3 V Voltage Range 5.0 is 5.0V ± 0.5 V

AC Operating Requirements

| | 73.5918 | 1 Y | 74AC T _A = +25°C C _L = 50 pF | | 54AC | 74AC | | Fig. No. |
|------------------|---|--------------------------|--|------------|---|--|-------|-------------|
| Symbol | Parameter | V _{CC} * (V) | | | $T_A = -55^{\circ}C$ to $+125^{\circ}C$ $C_L = 50 pF$ | $T_A = -40^{\circ}C$ to $+85^{\circ}C$ $C_L = 50 pF$ | Units | |
| | A CONTRACTOR SACRA | 11.12 12.37.08 | Тур | | Guaranteed Mi | inimum | 100.0 | |
| ts | Setup Time, HIGH or LOW J_n or \overline{K}_n to CP_n | 3.3 5.0 | 3.5 2.0 | 6.5 4.5 | 8.0 5.5 | 7.5 5.0 | ns | 2-9 |
| th s | Hold Time, HIGH or LOW J_n or \overline{K}_n to CP_n | 3.3 5.0 | -1.5 -0.5 | 0 0.5 | 0 0.5 | 0 0.5 | ns | 2-9 |
| t _w | Pulse Width CDn or SDn | 3.3 5.0 | 2.0 2.0 | 4.0 3.5 | 8.0 5.5 | 4.5 3.5 | ns | 2-6 |
| t _{rec} | Recovery Time CDn or SDn to CPn | 3.3 5.0 | -2.5 -1.5 | 0 | 0.5 0.5 | 0 | ns | 2-9 |

^{*}Voltage Range 3.3 is 3.3V \pm 0.3V Voltage Range 5.0 is 5.0V \pm 0.5V

AC Electrical Characteristics

| | TANC | 9 | 544 | 74ACT | TAAC | 54/ | ACT | 74/ | ACT | | |
|------------------|--|-----------------------|--|-------|------|---|------------|--|---------------------|-------|-------------|
| Symbol | Parameter | V _{CC} * (V) | T _A = +25°C C _L = 50 pF | | | $T_A = -55^{\circ}C$ to $+125^{\circ}C$ $C_L = 50 pF$ | | $T_A = -40^{\circ}C$ to $+85^{\circ}C$ $C_L = 50 pF$ | | Units | Fig. No. |
| | west nist | | Min | Тур | Max | Min | Max | Min | Max | | |
| f _{max} | Maximum Clock Frequency | 5.0 | 145 | 210 | 150 | 85 | 3.3 5.0 | 125 | iprom Dio foscoy | MHz | 2-3 |
| t _{PLH} | Propagation Delay CP_n to Q_n or \overline{Q}_n | 5.0 | 4.0 | 7.0 | 11.0 | 1.0 | 14.0 | 3.5 | 13.0 | ns | 2-6 |
| t _{PHL} | Propagation Delay CP_n to Q_n or \overline{Q}_n | 5.0 | 3.0 | 6.0 | 10.0 | 1.0 | 12.0 | 2.5 | 11.5 | ns | 2-6 |
| t _{PLH} | Propagation Delay \overline{C}_{Dn} or \overline{S}_{Dn} to \overline{Q}_n or \overline{Q}_n | 5.0 | 2.5 | 5.5 | 9.5 | 1.0 | 11.5 | 2.0 | 10.5 | ns | 2-6 |
| t _{PHL} | Propagation Delay \overline{C}_{Dn} or \overline{S}_{Dn} to \overline{Q}_n or \overline{Q}_n | 5.0 | 2.5 | 6.0 | 10.0 | 1.0 | 12.5 | 2.0 | 11.5 | ns | 2-6 |

^{*}Voltage Range 5.0 is 5.0V ± 0.5 V

AC Operating Requirements

| | | V _{CC} * (V) | 74A | СТ | 54ACT | 74ACT | | - |
|------------------|---|--------------------------|--|-----|---|--|-------|-------------|
| Symbol | Parameter 0% | | T _A = +25°C C _L = 50 pF | | $T_A = -55^{\circ}C$ to $+125^{\circ}C$ $C_L = 50 pF$ | $T_A = -40^{\circ}C$ $to +85^{\circ}C$ $C_L = 50 pF$ | Units | Fig. No. |
| | 7q 9c _ (3) - 7c | | Тур | | Guaranteed M | | | |
| ts | Setup Time, HIGH or LOW J_n or \overline{K}_n to CP_n | 5.0 | 0.5 | 2.0 | 2.5 | 1 10 H 2.5 am 1 0 | ns | 2-9 |
| th | Hold Time, HIGH or LOW J_n or \overline{K}_n to CP_n | 5.0 | 0 | 2.0 | 2.0 | 2.0 | ns | 2-9 |
| t _w | Pulse Width CP _n or \overline{C}_{Dn} or \overline{S}_{Dn} | 5.0 | 3.0 | 5.0 | 7.0 | 6.0 | ns ns | 2-6 |
| t _{rec} | Recovery Time CDn or SDn to CPn | 5.0 | -2.5 | 0 | 0.5 | O STAIT VIEW | ns | 2-9 |

^{*}Voltage Range 5.0 is 5.0V ± 0.5 V

Capacitance

| Symbol | Parameter | AC/ACT | Units | Conditions |
|-----------------|----------------------------------|--------|--------|-----------------|
| | Farameter | Тур | Office | Conditions |
| CIN | Input Capacitance | 4.5 | pF | $V_{CC} = 5.0V$ |
| C _{PD} | Power Dissipation Capacitance | 35.0 | pF | $V_{CC} = 5.0V$ |



54AC/74AC112 • 54ACT/74ACT112 Dual JK Negative Edge-Triggered Flip-Flop

General Description

The 'AC/'ACT112 contain two independent, high-speed JK flip-flops with Direct Set and Clear inputs. Synchronous state changes are initiated by the falling edge of the clock. Triggering occurs at a voltage level of the clock and is not directly related to the transition time. The J and K inputs can change when the clock is in either state without affecting the flip-flop, provided that they are in the desired state during the recommended setup and hold times relative to the falling edge of the clock. A LOW signal on \overline{S}_D or \overline{C}_D prevents clocking and forces Q or \overline{Q} HIGH, respectively. Simultaneous LOW signals on \overline{S}_D and \overline{C}_D force both Q and \overline{Q} HIGH.

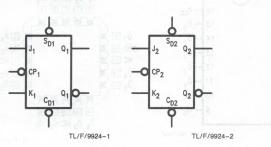
Asynchronous Inputs:

LOW input to \overline{S}_D sets Q to HIGH level LOW input to \overline{C}_D sets Q to LOW level Clear and Set are independent of clock Simultaneous LOW on \overline{C}_D and \overline{S}_D makes both Q and \overline{Q} HIGH

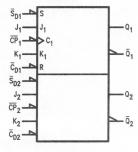
Features

■ 'ACT112 has TTL-compatible inputs

Logic Symbols



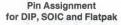
IEEE/IEC

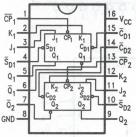


TL/F/9924-4

| Pin Names | Description |
|---|--|
| J ₁ , J ₂ , K ₁ , K ₂ | Data Inputs |
| $\overline{CP}_1, \overline{CP}_2$ | Clock Pulse Inputs (Active Falling Edge) |
| $\overline{C}_{D1}, \overline{C}_{D2}$ | Direct Clear Inputs (Active LOW) |
| $\overline{S}_{D1}, \overline{S}_{D2}$ | Direct Set Inputs (Active LOW) |
| $Q_1, Q_2, \overline{Q}_1, \overline{Q}_2$ | Outputs |

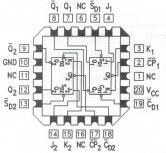
Connection Diagrams





TI /F/9924-3

Pin Assigment for LCC



TL/F/9924-5



54AC/74AC138 • 54ACT/74ACT138 1-of-8 Decoder/Demultiplexer

General Description

The 'AC/'ACT138 is a high-speed 1-of-8 decoder/demultiplexer. This device is ideally suited for high-speed bipolar memory chip select address decoding. The multiple input enables allow parallel expansion to a 1-of-24 decoder using just three 'AC/'ACT138 devices or a 1-of-32 decoder using four 'AC/'ACT138 devices and one inverter.

Features

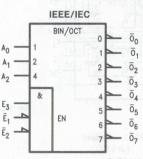
- Demultiplexing capability
- Multiple input enable for easy expansion
- Active LOW mutually exclusive outputs
- Outputs source/sink 24 mA
- 'ACT138 has TTL-compatible inputs

Ordering Code: See Section 5

Logic Symbol

E₁ A₀ A₁ A₂ E₂ E₃ O₀ O₁ O₂ O₃ O₄ O₅ O₆ O₇

TL/F/9925-1



TL/F/9925-7

| Pin Names | Description |
|-----------------------------------|----------------|
| A ₀ -A ₂ | Address Inputs |
| $\overline{E}_1 - \overline{E}_2$ | Enable Inputs |
| E ₃ | Enable Input |
| $\overline{O}_0 - \overline{O}_7$ | Outputs |

Connection Diagrams

3 A₁

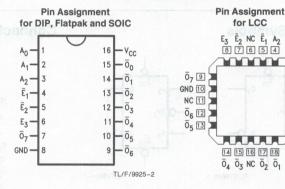
2 A₀

1 NC

20 V_{CC}

19 00

TL/F/9925-3



lock Pulse Inputs (Active Felling E feet Clest Inputs (Active LOW) incot@st.Inputs (Active LOW)

Functional Description

The 'AC/'ACT138 high-speed 1-of-8 decoder/demultiplexer accepts three binary weighted inputs (A₀, A₁, A₂) and, when enabled, provides eight mutually exclusive active-LOW outputs $(\overline{O}_0-\overline{O}_7)$. The 'AC/'ACT138 features three Enable inputs, two active-LOW (E₁, \overline{E}_2) and one active-HIGH (E₃). All outputs will be HIGH unless \overline{E}_1 and \overline{E}_2 are LOW and \overline{E}_3 is HIGH. This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines)

decoder with just four 'AC/'ACT138 devices and one inverter (see *Figure 1*). The 'AC/'ACT138 can be used as an 8-output demultiplexer by using one of the active LOW Enable inputs as the data input and the other Enable inputs as strobes. The Enable inputs which are not used must be permanently tied to their appropriate active-HIGH or active-LOW state.

Truth Table

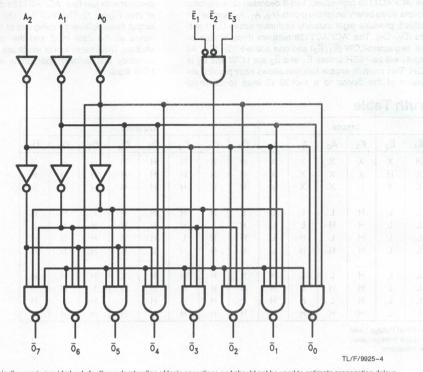
| | | Inp | uts | | | | | | Out | puts | | | |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----|
| Ē ₁ | Ē ₂ | E ₃ | A ₀ | A ₁ | A ₂ | Ō ₀ | Ō ₁ | Ō ₂ | O ₃ | Ō ₄ | Ō ₅ | Ō ₆ | 07 |
| Н | Х | Х | Х | X | X | Н | Н | Н | Н | Н | Н | Н | Н |
| X | Н | X | X | X | X | Н | Н | Н | Н | Н | Н | Н | Н |
| X | X | L | X | X | X | Н | Н | Н | Н | Н | Н | Н | Н |
| L | L | Н | L | L | L | L | н | н | Н | н | Н | Н | Н |
| L | L | Н | Н | L | L | Н | L | Н | Н | Н | Н | Н | Н |
| L | L | Н | L | Н | L | Н | Н | L | Н | Н | Н | Н | Н |
| L | L | Н | Н | Н | L | Н | Н | Н | L | Н | Н | Н | Н |
| L | L | н | L | L | Н | Н | Н | Н | Н | L | Н | Н | Н |
| L | L | Н | н | L | н | н | Н | Н | Н | Н | L | Н | Н |
| L | L | Н | L | Н | Н | Н | Н | Н | Н | Н | н | L | Н |
| L | L | Н | Н | Н | н | Н | Н | Н | Н | Н | Н | Н | E |

H = HIGH Voltage Level

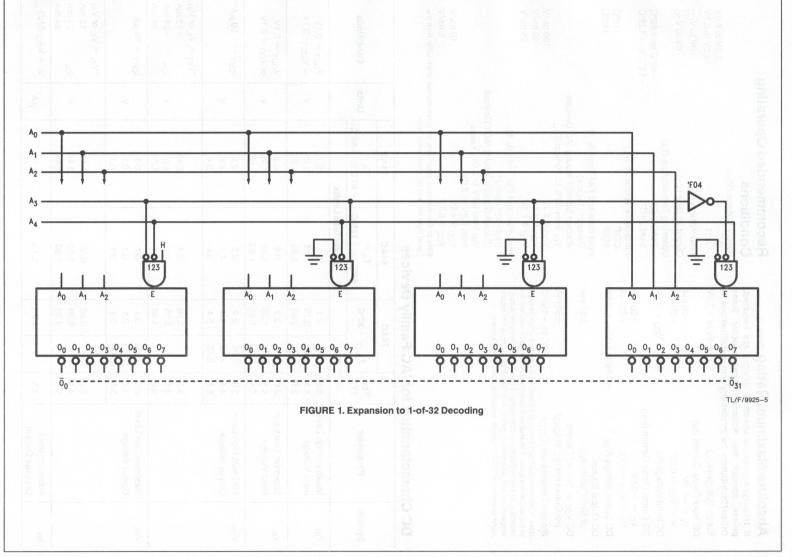
L = LOW Voltage Level

X = Immaterial

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.



Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Supply Voltage (V _{CC}) | -0.5V to $+7.0$ V |
|---|---------------------------------|
| DC Input Diode Current (I _{IK}) | |
| $V_I = -0.5V$ | -20 mA |
| $V_I = V_{CC} + 0.5V$ | + 20 mA |
| DC Input Voltage (VI) | -0.5 V to V_{CC} + 0.5 V |
| DC Output Diode Current (IOK) | |
| $V_0 = -0.5V$ | -20 mA |
| $V_0 = V_{CC} + 0.5V$ | + 20 mA |
| 0 00 | -0.5 V to to $V_{CC} + 0.5$ V |
| DC Output Voltage (V _O) | -0.5V to to VCC + 0.5V |
| DC Output Source | |
| or Sink Current (I _O) | ± 50 mA |
| DC V _{CC} or Ground Current | |
| per Output Pin (I _{CC} or I _{GND}) | ± 50 mA |
| Storage Temperature (T _{STG}) | -65°C to +150°C |
| otorago romporataro (151G) | 00001011000 |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

Recommended Operating Conditions

| Supply Voltage (V _{CC}) 'AC 'ACT | 2.0V to 6.0V 4.5V to 5.5V |
|---|-----------------------------------|
| Input Voltage (V _I) | 0V to V _{CC} |
| Output Voltage (V _O) | 0V to V _{CC} |
| Operating Temperature (T _A) 74AC/ACT 54AC/ACT | -40°C to +85°C -55°C to +125°C |
| Junction Temperature (T _J) CDIP PDIP | 175°C 140°C |
| Input Rise and Fall Time (t _r , t _f) | |

(Note 2) (Typical) (Except Schmitt Inputs) 'AC Devices

VIN from 30% to 70% of VCC V_{CC} @ 3.0V 150 ns/V

V_{CC} @ 4.5V 40 ns/V V_{CC} @ 5.5V 25 ns/V

Input Rise and Fall Time (tr, tf) (Note 2) (Typical)

(Except Schmitt Inputs) 'ACT Devices VIN from 0.8V to 2.0V, Vmeas

from 0.8V to 2.0V

V_{CC} @ 4.5V 10 ns/V V_{CC} @ 5.5V 8 ns/V

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

| | | 1 | 74 | AC | 54AC | 74AC | | | |
|-----------------|--------------------------------------|------------------------|-------------------------|----------------------|----------------------------------|---------------------------------|-------|---|--|
| Symbol | Parameter | V _{CC} (V) | T _A = +25°C | | T _A = -55°C to +125°C | T _A = -40°C to +85°C | Units | Conditions | |
| | | | Тур | | Guaranteed L | imits | | | |
| V _{IH} | Minimum High Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{IL} | Maximum Low Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{OH} | Minimum High Level Output Voltage | 3.0 4.5 5.5 | 2.99 4.49 5.49 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | V | $I_{OUT} = -50 \mu A$ | |
| | | 3.0 4.5 5.5 | -013 | 2.56 3.86 4.86 | 2.4 3.7 4.7 | 2.46 3.76 4.76 | ٧ | *V _{IN} = V _{IL} or V _{II} -12 m/ I _{OH} -24 m/ -24 m/ | |
| V _{OL} | Maximum Low Level Output Voltage | 3.0 4.5 5.5 | 0.002 0.001 0.001 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | V | I _{OUT} = 50 μA | |
| | | 3.0 4.5 5.5 | -010 | 0.36 0.36 0.36 | 0.50 0.50 0.50 | 0.44 0.44 0.44 | V | $*V_{IN} = V_{IL} \text{ or } V_{IH}$ 12 mA I_{OL} 24 mA 24 mA | |
| I _{IN} | Maximum Input Leakage Current | 5.5 | la contenta | ±0.1 | ±1.0 | ±1.0 | μА | $V_{I} = V_{CC}$, GND | |

DC Characteristics for 'AC Family Devices (Continued)

| Symbol | TANG | | 7 | 4AC | 54AC | 74AC | | | |
|------------------|-------------------------------------|---------------------|------------------|--------|----------------------------------|---------------------------------|-------|------------------------------|--|
| | Parameter | V _{CC} (V) | T _A = | + 25°C | T _A = -55°C to +125°C | T _A = -40°C to +85°C | Units | Conditions | |
| | | | Тур | 12 | Guaranteed Lin | | | | |
| I _{OLD} | †Minimum Dynamic | 5.5 | N. 53 TH 8 | 334991 | 50 | 75 | mA | V _{OLD} = 1.65V Max | |
| IOHD | Output Current | 5.5 | 0.81 | 0.1 | -50 | −75 | mA | V _{OHD} = 3.85V Min | |
| lcc | Maximum Quiescent Supply Current | 5.5 | 15.0 | 8.0 | 160.0 | 80.0 | μА | $V_{IN} = V_{CC}$ or GND | |

^{*}All outputs loaded; thresholds on input associated with output under test.

DC Characteristics for 'ACT Family Devices

| | 15 140 | | 744 | CT | 54ACT | 74ACT | Late 1 and | to a series of | |
|------------------|--------------------------------------|---------------------|------------------|-----------------------------------|--------------------------|---------------------------------|------------|---|--|
| Symbol | Parameter | V _{CC} (V) | T _A = | T _A = -55°C to + 125°C | | T _A = -40°C to +85°C | Units | Conditions | |
| | | | Тур | | Guaranteed L | imits | Value ye | Voltage Flange 5.0 in 6 | |
| V _{IH} | Minimum High Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 2.0 2.0 | 2.0 2.0 | 2.0 2.0 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{IL} | Maximum Low Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 0.8 | 0.8 0.8 | 0.8 0.8 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{OH} | Minimum High Level Output Voltage | 4.5 5.5 | 4.49 5.49 | 4.4 5.4 | 4.4 5.4 | 4.4 5.4 | ٧ | $I_{OUT} = -50 \mu\text{A}$ | |
| | 1.6 11.5 m | 4.5 5.5 | \$1 | 3.86 4.86 | 3.70 4.70 | 3.76 4.76 | on Delay | $V_{IN} = V_{IL} \text{ or } V_{IH}$ -24 mA -24 mA | |
| V _{OL} | Maximum Low Level Output Voltage | 4.5 5.5 | 0.001 0.001 | 0.1 0.1 | 0.1 0.1 | 0.1 0.6 0.1 | ٧ | I _{OUT} = 50 μA | |
| | 2.0 (2.5 ns | 4.5 5.5 | 13: | 0.36 0.36 | 0.50 0.50 d.V | 0.44 0.30 0.44 | V | $\begin{tabular}{ll} *V_{IN} = V_{IL} \mbox{ or } V_{IH} \\ I_{OL} & 24 \mbox{ mA} \\ 24 \mbox{ mA} \\ \end{tabular}$ | |
| I _{IN} | Maximum Input Leakage Current | 5.5 | 14 | ±0.1 | 0.Sr ±1.0 _{0.8} | ±1.0 | μΑ | $V_{I} = V_{CC}$, GND | |
| Ісст | Maximum I _{CC} /Input | 5.5 | 0.6 | 0.7 | a.or 1.6 a.a | 0.5 - 1.5 0.8 | mA | $V_I = V_{CC} - 2.1V$ | |
| I _{OLD} | †Minimum Dynamic | 5.5 | | | 50 | 75 | mA | V _{OLD} = 1.65V Max | |
| IOHD | Output Current | 5.5 | | | -50 | -75 | mA | V _{OHD} = 3.85V Min | |
| Icc | Maximum Quiescent Supply Current | 5.5 | | 8.0 | 160.0 | 80.0 | μА | V _{IN} = V _{CC} or GND | |

^{*}All outputs loaded; thresholds on input associated with output under test.

[†]Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC} . I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

[†]Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

| Symbol | Parameter | 0.54 | | 74AC | | 54 | AC | 74 | AC | | |
|------------------|--|-------------------|------------|---|--------------|------------|-------------------------|------------|-------------------------|-------|-------------|
| | | V _{CC} * | 3°04 | T _A = +25° C _L = 50 pF | | to + | −55°C 125°C 50 pF | to + | −40°C -85°C 50 pF | Units | Fig. No. |
| | | | Min | Тур | Max | Min | Max | Min | Max | | |
| t _{PLH} | Propagation Delay A_n to \overline{O}_n | 3.3 5.0 | 1.5 1.5 | 8.5 6.5 | 13.0 9.5 | 1.0 1.0 | 16.0 12.0 | 1.5 1.5 | 15.0 10.5 | ns | 2-6 |
| t _{PHL} | Propagation Delay A_n to \overline{O}_n | 3.3 5.0 | 1.5 1.5 | 8.0 6.0 | 12.5 9.0 | 1.0 1.0 | 15.0 11.5 | 1.5 1.5 | 14.0 10.5 | ns | 2-6 |
| t _{PLH} | Propagation Delay \overline{E}_1 or \overline{E}_2 to \overline{O}_n | 3.3 5.0 | 1.5 1.5 | 11.0 8.0 | 15.0 11.0 | 1.0 1.0 | 16.5 13.0 | 1.5 1.5 | 16.0 12.0 | ns | 2-6 |
| t _{PHL} | Propagation Delay \overline{E}_1 or \overline{E}_2 to \overline{O}_n | 3.3 5.0 | 1.5 1.5 | 9.5 7.0 | 13.5 9.5 | 1.0 1.0 | 15.5 12.0 | 1.5 1.5 | 15.0 10.5 | ns | 2-6 |
| t _{PLH} | Propagation Delay E ₃ to O _n | 3.3 5.0 | 1.5 1.5 | 11.0 8.0 | 15.5 11.0 | 1.0 1.0 | 17.0 13.5 | 1.5 1.5 | 16.5 12.5 | ns | 2-6 |
| t _{PHL} | Propagation Delay E_3 to \overline{O}_n | 3.3 5.0 | 1.5 1.5 | 8.5 6.0 | 13.0 8.0 | 1.0 1.0 | 15.0 11.0 | 1.5 1.0 | 14.0 9.5 | ns | 2-6 |

^{*}Voltage Range 3.3 is 3.3V ± 0.3 V Voltage Range 5.0 is 5.0V ± 0.5 V

AC Electrical Characteristics

| | | | | 74ACT | | 54 | ACT | 74 | ACT | | |
|------------------|--|-------------------|--|-------|------|--|------|--|------|-------|-------------|
| Symbol | Parameter | V _{CC} * | $T_A = +25^{\circ}C$ $C_L = 50 \text{ pF}$ | | | T _A = -55°C to + 125°C C _L = 50 pF | | T _A = -40°C to +85°C C _L = 50 pF | | Units | Fig. No. |
| | | 1.4 | Min | Тур | Max | Min | Max | Min | Max | uu0 | |
| tpLH | Propagation Delay A_n to \overline{O}_n | 5.0 | 1.5 | 7.0 | 10.5 | 1.0 | 12.5 | 1.5 | 11.5 | ns | 2-6 |
| t _{PHL} | Propagation Delay A_n to \overline{O}_n | 5.0 | 1.5 | 6.5 | 10.5 | 1.0 | 12.5 | 1.5 | 11.5 | ns | 2-6 |
| t _{PLH} | Propagation Delay \overline{E}_1 or \overline{E}_2 to \overline{O}_n | 5.0 | 2.5 | 8.0 | 11.5 | 1.0 | 13.5 | 2.0 | 12.5 | ns | 2-6 |
| t _{PHL} | Propagation Delay \overline{E}_1 or \overline{E}_2 to \overline{O}_n | 5.0 | 2.0 | 7.5 | 11.5 | 1.0 | 12.5 | 2.0 | 12.5 | ns | 2-6 |
| t _{PLH} | Propagation Delay E ₃ to On | 5.0 | 2.5 | 8.0 | 12.0 | 1.0 | 14.0 | 2.0 | 13.0 | ns | 2-6 |
| t _{PHL} | Propagation Delay E ₃ to On | 5.0 | 2.0 | 6.5 | 10.5 | 1.0 | 12.0 | 1.5 | 11.5 | ns | 2-6 |

^{*}Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

| Symbol | Parameter | AC/ACT | Units | Conditions |
|-----------------|----------------------------------|--------|--------|-----------------|
| Суппрог | T di dilictor | Тур | Onito | Contactions |
| C _{IN} | Input Capacitance | 4.5 | pF and | $V_{CC} = 5.0V$ |
| C _{PD} | Power Dissipation Capacitance | 60.0 | pF | $V_{CC} = 5.0V$ |



54AC/74AC139 • 54ACT/74ACT139 **Dual 1-of-4 Decoder/Demultiplexer**

General Description

The 'AC/'ACT139 is a high-speed, dual 1-of-4 decoder/demultiplexer. The device has two independent decoders, each accepting two inputs and providing four mutually-exclusive active-LOW outputs. Each decoder has an active-LOW Enable input which can be used as a data input for a 4-output demultiplexer. Each half of the 'AC/'ACT139 can be used as a function generator providing all four minterms of two variables.

Features

- Multifunction capability
- Two completely independent 1-of-4 decoders
- Active LOW mutually exclusive outputs
- Outputs source/sink 24 mA
- 'ACT139 has TTL-compatible inputs

Ordering Code: See Section 5

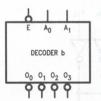
Logic Symbols

An

DECODER a

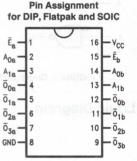
01 02 03

TL/F/9926-8



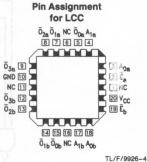
IEEE/IEC Ōla $\bar{\mathrm{o}}_{\mathrm{2a}}$ 2 EN Ō3a Onb A_{0b} \bar{o}_{1b} A_{1b} \bar{o}_{2b} $\bar{0}_{3b}$ TL/F/9926-2

Connection Diagrams



TL/F/9926-3

TL/F/9926-1 **Pin Names** Description A₀, A₁ Address Inputs **Enable Inputs** $\overline{O}_0 - \overline{O}_3$ Outputs



Functional Description

The 'AC/'ACT139 is a high-speed dual 1-of-4 decoder/demultiplexer. The device has two independent decoders, each of which accepts two binary weighted inputs (A_0-A_1) and provides four mutually exclusive active-LOW outputs $(\overline{O_0}-\overline{O_3}).$ Each decoder has an active-LOW enable $(\overline{E}).$ When \overline{E} is HIGH all outputs are forced HIGH. The enable can be used as the data input for a 4-output demultiplexer application. Each half of the 'AC/'ACT139 generates all four minterms of two variables. These four minterms are useful in some applications, replacing multiple gate functions as shown in Figure a, and thereby reducing the number of packages required in a logic network.

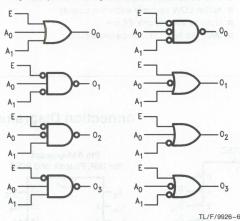


FIGURE a. Gate Functions (Each Half)

Truth Table

| | Inputs | n since | Outputs | | | | | | | |
|---|----------------|----------------|------------------|----------------|----------------|----------------|--|--|--|--|
| Ē | A ₀ | A ₁ | \overline{O}_0 | Ō ₁ | Ō ₂ | O ₃ | | | | |
| Н | X | X | Н | Н | Н | н | | | | |
| L | L | L | L | Н | Н | Н | | | | |
| L | H | L | Н | L | Н | Н | | | | |
| L | L | Н | Н | Н | L | Н | | | | |
| L | Н | Н | . н | H | Н | L | | | | |

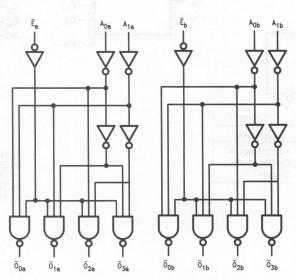
TL/F/9926-5

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1) Recommended Operating

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Supply Voltage (V _{CC}) | -0.5V to $+7.0$ V |
|--|---------------------------------|
| DC Input Diode Current (I_{IK}) $V_I = -0.5V$ | -20 mA |
| $V_I = V_{CC} + 0.5V$ | + 20 mA |
| DC Input Voltage (V _I) | -0.5 V to $V_{CC} + 0.5$ V |
| DC Output Diode Current (Id | S0 75 (xc |
| $V_{O} = -0.5V$ $V_{O} = V_{CC} + 0.5V$ | -20 mA +20 mA |
| DC Output Voltage (V _O) | -0.5 V to to $V_{CC} + 0.5$ V |
| DC Output Source | |
| or Sink Current (IO) | ± 50 mA |
| DC V _{CC} or Ground Current | |
| per Output Pin (I _{CC} or I _{GN} | b) ± 50 mA |
| Storage Temperature (TSTG | -65°C to +150°C |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

Recommended Operating Conditions

| Supply Volt 'AC 'ACT | age (V _{CC}) | 2.0V to 6.0V 4.5V to 5.5V |
|---|---|---|
| Input Voltag | ge (V _I) | 0V to V _{CC} |
| Output Volt | age (V _O) Femperature (T _A | 0V to V _{CC} |
| 74AC/AC 54AC/AC | CT . | -40°C to +85°C -55°C to +125°C |
| Junction Te CDIP PDIP | emperature (T _J) | 175°C 140°C |
| (Note 2) (Except 3 | and Fall Time (t _r (Typical) Schmitt Inputs) '/ 30% to 70% of | AC Devices |
| V _{CC} @ 3. | 0V 5V | 150 ns/V 40 ns/V |
| V _{CC} @ 5. | | 25 ns/V |
| (Note 2) (Except S V _{IN} from | Schmitt Inputs) '/ 0.8V to 2.0V, V _r | ACT Devices |
| from 0.8\ | | 10 ns/V |
| V _{CC} @ 4. V _{CC} @ 5. | | 8 ns/V |
| | | for those devices which differ from the |

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

| | s = anot A | A. | | | 54AC | 74AC | m 439, 4 | Conditions | |
|-----------------|--------------------------------------|---------------------|-------------------------|----------------------|----------------------------------|--|------------|--|--|
| Symbol | Parameter | V _{CC} (V) | | | T _A = -55°C to +125°C | T _A = -40°C to +85°C | Units | | |
| Am AS - | Table Val | 0 | | | Guaranteed Limits | | | | |
| V _{IH} | Minimum High Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| Z4 mA | Maximum Low Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | 0,9 1.35 1.65 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{OH} | Minimum High Level Output Voltage | 3.0 4.5 5.5 | 2.99 4.49 5.49 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | V | $I_{OUT} = -50 \mu\text{A}$ | |
| | E= quoV Am E=(gHoV An | 3.0 4.5 5.5 | | 2.56 3.86 4.86 | 2.4 3.7 4.7 | 2.46 3.76 4.76 |) V | $V_{\rm IN} = V_{\rm IL} {\rm or} V_{\rm IH}$ $-12 {\rm mA}$ $-24 {\rm mA}$ $-24 {\rm mA}$ | |
| V _{OL} | Maximum Low Level Output Voltage | 3.0 4.5 5.5 | 0.002 0.001 0.001 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | 0.1 0.1 0.1 0.1 0.1 0.1 0.1 0.1 0.1 0.1 0.1 | fnews v | Ι _{ΟUT} = 50 μΑ | |
| | | 3.0 4.5 5.5 | | 0.36 0.36 0.36 | 0.50 0.50 0.50 | 0.44 0.44 0.44 | V | $V_{IN} = V_{IL} \text{ or } V_{IH}$ 12 mA $I_{OL} \qquad 24 \text{ mA}$ 24 mA | |

DC Characteristics for 'AC Family Devices (Continued)

| Symbol | | | 74AC | | 54AC | 74AC | BIR OR | Josinos saesto | | |
|-----------------|-------------------------------------|------------------------|---------------------------|-----------|-----------------------------------|---------------------------------|----------|------------------------------|--|--|
| | Parameter | V _{CC} (V) | T _A = + | 25°C | T _A = -55°C to + 125°C | T _A = -40°C to +85°C | Units | Conditions | | |
| | 10 | | Тур | sileV tuo | Guaranteed L | imits | will Men | 40 epoi0 trani 00. | | |
| 1 _{IN} | Maximum Input Leakage Current | 5.5 | tage (Vg) Femperatu | ±0.1 | ±1.0 | ±1.0 | μА | $V_I = V_{CC}$, GND | | |
| lold | †Minimum Dynamic | 5.5 | TO | A CAAA | 50 | 75 | mA | V _{OLD} = 1.65V Max | | |
| IOHD | Output Current | 5.5 | emperature | Laodan | -50 | -75 | mA | V _{OHD} = 3.85V Min | | |
| Icc | Maximum Quiescent Supply Current | 5.5 | Tribe Disease | 8.0 | 160.0 | 80.0 | μА | $V_{IN} = V_{CC}$ or GND | | |

^{*}All outputs loaded; thresholds on input associated with output under test.

DC Characteristics for 'ACT Family Devices

| | Ų. | 1 1000 | 744 | CT | 54ACT | 74ACT | lagol Tour | temperature, and output in | |
|------------------|--------------------------------------|---------------------|------------------------|--------------|----------------------------------|---------------------------------|------------|--|--|
| Symbol | Parameter | V _{CC} (V) | T _A = +25°C | | T _A = -55°C to +125°C | T _A = -40°C to +85°C | Units | Conditions | |
| | | | Тур | VERW IN | Guaranteed L | | | | |
| V _{IH} | Minimum High Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 2.0 2.0 | 2.0 2.0 | 2.0 2.0 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{IL} | Maximum Low Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 0.8 0.8 | 0.8 0.8 | 0.8 0.8 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{OH} | Minimum High Level Output Voltage | 4.5 5.5 | 4.49 5.49 | 4.4 5.4 | 4.4 5.4 | 4.4 5.4 | ٧ | $I_{OUT} = -50 \mu\text{A}$ | |
| | mod letinu pra | 4.5 5.5 | o O. etingi. | 3.86 4.86 | 3.70 4.70 | 3.76 4.76 | V | $\begin{tabular}{ll} *V_{IN} &= V_{IL} \mbox{ or } V_{IH} \\ &-24 \mbox{ mA} \\ &-24 \mbox{ mA} \end{tabular}$ | |
| V _{OL} | Maximum Low Level Output Voltage | 4.5 5.5 | 0.001 | 0.1 0.1 | 0.1 0.1 | 0.1 0.1 | V | $I_{OUT} = 50 \mu A$ | |
| | T TVOV povise V | 4.5 5.5 | | 0.36 0.36 | 0.50 0.50 | 0.44 0.44 | Val wol | ${^*V_{IN} = V_{IL} \text{ or } V_{IH}} $ ${^{24} \text{ mA}} $ ${^{24} \text{ mA}} $ | |
| I _{IN} | Maximum Input Leakage Current | 5.5 | | ±0.1 | 28 ±1.0 08 | 00 S ± 1.0 | μА | $V_I = V_{CC}$, GND | |
| ГССТ | Maximum I _{CC} /Input | 5.5 | 0.6 | | 1.6 | 1.5 | mA | $V_I = V_{CC} - 2.1V$ | |
| lold | †Minimum Dynamic | 5.5 | | | 50 | 75 | mA | V _{OLD} = 1.65V Max | |
| I _{OHD} | Output Current | 5.5 | | | -50 988 | -75 | mA | V _{OHD} = 3.85V Min | |
| lcc | Maximum Quiescent Supply Current | 5.5 | | 8.0 | 160.0 | 80.0 | μΑ | V _{IN} = V _{CC} or GND | |

^{*}All outputs loaded; thresholds on input associated with output under test.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

[†]Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC} . I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

[†]Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics

| Symbol | | | | 74AC | | 54 | AC | 74 | AC | | |
|------------------|--|--------------------------|------------|-----------------------|-------------|---|--------------|--|--------------|-------|-------------|
| | Parameter | V _{CC} * (V) | | C _L = +25° | | $T_A = -55^{\circ}C$ to $+125^{\circ}C$ $C_L = 50 pF$ | | T _A = -40°C to +85°C C _L = 50 pF | | Units | Fig. No. |
| | | | Min | Тур | Max | Min | Max | Min | Max | iuar | 11-8 |
| t _{PLH} | Propagation Delay A_n to \overline{O}_n | 3.3 5.0 | 4.0 3.0 | 8.0 6.5 | 11.5 8.5 | 1.0 1.0 | 14.5 11.0 | 3.5 2.5 | 13.0 9.5 | ns | 2-6 |
| t _{PHL} | Propagation Delay A_n to \overline{O}_n | 3.3 5.0 | 3.0 2.5 | 7.0 5.5 | 10.0 7.5 | 1.0 1.0 | 12.5 10.0 | 2.5 2.0 | 11.0 8.5 | ns | 2-6 |
| t _{PLH} | Propagation Delay \overline{E}_n to \overline{O}_n | 3.3 5.0 | 4.5 3.5 | 9.5 7.0 | 12.0 8.5 | 1.0 1.0 | 14.5 11.0 | 3.5 3.0 | 13.0 10.0 | ns | 2-6 |
| t _{PHL} | Propagation Delay \overline{E}_n to \overline{O}_n | 3.3 5.0 | 4.0 2.5 | 8.0 6.0 | 10.0 7.5 | 1.0 1.0 | 12.5 10.0 | 3.0 2.5 | 11.0 8.5 | ns | 2-6 |

*Voltage Range 3.3 is 3.3V ± 0.3 V Voltage Range 5.0 is 5.0V ± 0.5 V

AC Electrical Characteristics

| | Assignment | 119 | | 74ACT | | 54ACT 74ACT | | | | | |
|------------------|--|-----------------------|-----|-----------------------|------|-------------|-------------------------|------|------------------------|-------|-----------|
| Symbol | Parameter | V _{CC} * (V) | | C _L = +25° | | to + | -55°C 125°C 50 pF | to + | -40°C 85°C 50 pF | Units | Fig. |
| | 41E 20 | W 121 | Min | Тур | Max | Min | Max | Min | Max | | 15 passes |
| t _{PLH} | Propagation Delay A_n to \overline{O}_n | 5.0 | 1.5 | 6.0 | 8.5 | 1.0 | 12.0 | 1.5 | 9.5 | ns | 2-6 |
| t _{PHL} | Propagation Delay A_n to \overline{O}_n | 5.0 | 1.5 | 6.0 | 9.5 | 1.0 | 11.0 | 1.5 | 10.5 | ns | 2-6 |
| t _{PLH} | Propagation Delay \overline{E}_n to \overline{O}_n | 5.0 | 2.5 | 7.0 | 10.0 | 1.0 | 12.5 | 2.0 | 11.0 | ns | 2-6 |
| t _{PHL} | Propagation Delay \overline{E}_n to \overline{O}_n | 5.0 | 2.0 | 7.0 | 9.5 | 1.0 | 12.0 | 1.5 | 10.5 | ns | 2-6 |

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

| Symbol | Parameter | AC/ACT | Units | Conditions | |
|-----------------|----------------------------------|--------|--------|------------------------|--|
| Symbol | H X | Тур | Office | | |
| C _{IN} | Input Capacitance | 4.5 | pF | V _{CC} = 5.0\ | |
| C _{PD} | Power Dissipation Capacitance | 40.0 | pF | $V_{CC} = 5.0V$ | |



54AC/74AC151 ● 54ACT/74ACT151 8-Input Multiplexer

General Description

The 'AC/'ACT151 is a high-speed 8-input digital multiplexer. It provides, in one package, the ability to select one line of data from up to eight sources. The 'AC/'ACT151 can be used as a universal function generator to generate any logic function of four variables. Both true and complementary outputs are provided.

Features

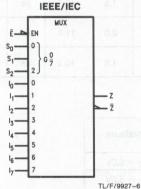
- Outputs source/sink 24 mA
- 'ACT151 has TTL-compatible inputs

Ordering Code: See Section 5

Logic Symbol

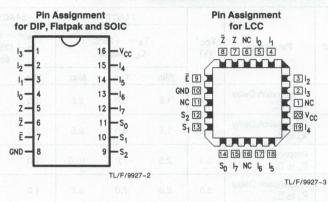
E lo l₁ l₂ l₃ l₄ l₅ l₆ l₇

TL/F/9927-1



| Pin Names | Description | | | | | |
|--------------------------------|----------------------|--|--|--|--|--|
| 10-17 | Data Inputs | | | | | |
| S ₀ -S ₂ | Select Inputs | | | | | |
| Ē | Enable Input | | | | | |
| Z | Data Output | | | | | |
| Z | Inverted Data Output | | | | | |

Connection Diagrams



Truth Table

| | Inp | | Outputs | | | | | |
|---|----------------|----------------|----------------|----------------|----------------|--|--|--|
| Ē | S ₂ | S ₁ | S ₀ | Z | Z | | | |
| Н | X | Х | Х | н | L | | | |
| L | L | L | L | Īo | I ₀ | | | |
| L | L | L | H | Ī1 | 11 | | | |
| L | L | Hossa | Law | Ī ₂ | 12 | | | |
| L | L | Н | Н | Ī ₃ | 13 | | | |
| L | H | L | L | Ī ₄ | 14 | | | |
| L | H | L | Н | Ī ₅ | 15 | | | |
| L | H | Н | L | Ī ₆ | 16 | | | |
| L | H | Н | Н | Ī ₇ | 17 | | | |

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

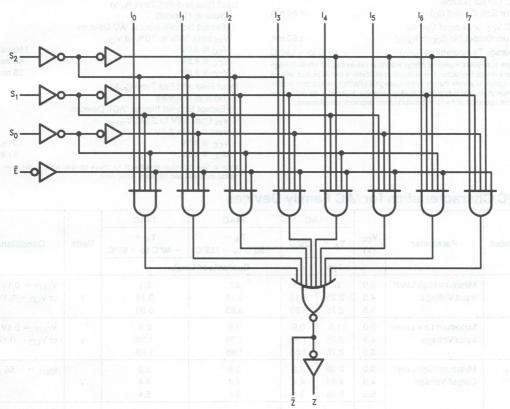
Functional Description

The 'AC/'ACT151 is a logic implementation of a single pole, 8-position switch with the switch position controlled by the state of three Select inputs, S_0 , S_1 , S_2 . Both true and complementary outputs are provided. The Enable input (\overline{E}) is active LOW. When it is not activated, the complementary output is HIGH and the true output is LOW regardless of all other inputs. The logic function provided at the output is:

$$\begin{split} Z &= \overline{E} \bullet (I_0 \bullet \overline{S}_0 \bullet \overline{S}_1 \bullet \overline{S}_2 + I_1 \bullet S_0 \bullet \overline{S}_1 \bullet \overline{S}_2 + I_2 \bullet \overline{S}_1 \bullet \overline{S}_2 + \overline{S}_2 \bullet \overline{S}_1 \bullet \overline{S}_1 \bullet \overline{S}_2 + \overline{S}_2 \bullet \overline{S}_2 \bullet \overline{S}_1 \bullet \overline{S}_2 + \overline{S}_2 \bullet \overline{S}_2$$

The 'AC/'ACT151 provides the ability, in one package to select from eight sources of data or control information. By proper manipulation of the inputs, the 'AC/'ACT151 can provide any logic function of four variables and its complement

Logic Diagram



TL/F/9927-4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Supply Voltage (V _{CC}) | -0.5V to $+7.0$ V |
|---|---------------------------------|
| DC Input Diode Current (I _{IK}) | |
| $V_{I} = -0.5V$ | -20 mA |
| $V_I = V_{CC} + 0.5V$ | + 20 mA |
| DC Input Voltage (V _I) | $-0.5V$ to $V_{CC} + 0.5V$ |
| DC Output Diode Current (IOK) | |
| $V_{O} = -0.5V$ | -20 mA |
| $V_O = V_{CC} + 0.5V$ | + 20 mA |
| DC Output Voltage (V _O) | -0.5 V to to $V_{CC} + 0.5$ V |
| DC Output Source | |
| or Sink Current (IO) | ± 50 mA |
| DC V _{CC} or Ground Current | |
| per Output Pin (I _{CC} or I _{GND}) | ± 50 mA |
| Storage Temperature (T _{STG}) | -65°C to +150°C |
| | |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

Recommended Operating Conditions

| Supply Voltage (V _{CC}) 'AC 'ACT | 1 5\/ to 5 5\/ |
|---|-----------------------------------|
| Input Voltage (V _I) | 01/1 1/ |
| Output Voltage (V _O) | 0V to V _{CC} |
| Operating Temperature (T _A) 74AC/ACT 54AC/ACT | -40°C to +85°C -55°C to +125°C |
| Junction Temperature (T _J) CDIP PDIP | 175°C 140°C |

Input Rise and Fall Time (t_r, t_f)
(Note 2) (Typical)

(Except Schmitt Inputs) 'AC Devices V_{IN} from 30% to 70% of V_{CC}

 VCC @ 3.0V
 150 ns/V

 VCC @ 4.5V
 40 ns/V

 VCC @ 5.5V
 25 ns/V

Input Rise and Fall Time (t_r, t_f)

(Note 2) (Typical)
(Except Schmitt Inputs) 'ACT Devices

V_{IN} from 0.8V to 2.0V, V_{meas} from 0.8V to 2.0V

typical input rise and fall times noted here.

 $$V_{CC}$ @ 4.5V $$10\ ns/V$$ $$V_{CC}$ @ 5.5V $$8\ ns/V$$ Note 2: See individual datasheets for those devices which differ from the

DC Characteristics for 'AC Family Devices

| Symbol | Parameter | | 74. | AC | 54AC | 74AC | | |
|-----------------|--------------------------------------|-------------------|-------------------------|----------------------|-----------------------------------|---------------------------------|-------|---|
| | | V _{CC} | T _A = +25°C | | T _A = -55°C to + 125°C | T _A = -40°C to +85°C | Units | Conditions |
| | | | Тур | | Guaranteed L | imits | | |
| V _{IH} | Minimum High Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ |
| V _{IL} | Maximum Low Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ |
| V _{OH} | Minimum High Level Output Voltage | 3.0 4.5 5.5 | 2.99 4.49 5.49 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | ٧ | $I_{OUT} = -50 \mu\text{A}$ |
| | ut ayelua nafalladora etsteve va | 3.0 4.5 5.5 | ion Lachs | 2.56 3.86 4.86 | 2.4 3.7 4.7 | 2.46 3.76 4.76 | V | $\label{eq:VIN} \begin{split} * V_{\text{IN}} &= V_{\text{IL}} \text{or} V_{\text{IH}} \\ &- 12 \text{mA} \\ I_{\text{OH}} &- 24 \text{mA} \\ &- 24 \text{mA} \end{split}$ |
| V _{OL} | Maximum Low Level Output Voltage | 3.0 4.5 5.5 | 0.002 0.001 0.001 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | ٧ | $I_{OUT} = 50 \mu A$ |
| | | 3.0 4.5 5.5 | | 0.36 0.36 0.36 | 0.50 0.50 0.50 | 0.44 0.44 0.44 | V | $\begin{tabular}{ll} *V_{IN} &= V_{IL} \mbox{ or } V_{IH} \\ &= 12 \mbox{ mA} \\ I_{OL} &= 24 \mbox{ mA} \\ &= 24 \mbox{ mA} \\ \end{tabular}$ |
| I _{IN} | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | ±1.0 | μΑ | $V_{I} = V_{CC}$, GND |

DC Characteristics for 'AC Family Devices (Continued)

| | TARC | | 74AC | | 54AC | 74AC | | | |
|------------------|-------------------------------------|-----|-----------------------------------|---------------------------------|---------------|------------|----|--|--|
| Symbol | | | T _A = -55°C to + 125°C | T _A = -40°C to +85°C | Units | Conditions | | | |
| | | | Тур | 75 | Guaranteed L | | | | |
| lold | †Minimum Dynamic | 5.5 | 100 | FRENT | 50 | 75 | mA | V _{OLD} = 1.65V Max | |
| I _{OHD} | Output Current | 5.5 | 1 | 0.1 | 0 8 € −50 a 8 | as -75 aa | mA | V _{OHD} = 3.85V Min | |
| Icc | Maximum Quiescent Supply Current | 5.5 | 13 | 8.0 | 160.0 | 80.0 | μА | V _{IN} = V _{CC} or GND | |

^{*}All outputs loaded; thresholds on input associated with output under test.

DC Characteristics for 'ACT Family Devices

| Symbol | Parameter | | 744 | CT | 54ACT | 74ACT | le faction | Canada S |
|------------------|--------------------------------------|---------------------|----------------------------|--------------|--------------------------|---------------------------------|-------------------------|---|
| | | V _{CC} (V) | T _A = + 25°C | | -55°C to +125°C | T _A = -40°C to +85°C | Units | Conditions |
| | | | Тур | | Guaranteed L | V8 03: V0 | Voltago Runge 5.0 is \$ | |
| V _{IH} | Minimum High Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 2.0 2.0 | 2.0 2.0 | 2.0 2.0 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ |
| V _{IL} | Maximum Low Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 0.8 0.8 | 0.8 0.8 | 0.8 0.8 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ |
| V _{OH} | Minimum High Level Output Voltage | 4.5 5.5 | 4.49 5.49 | 4.4 5.4 | 4.4 5.4 | 4.4 5.4 | V | $I_{OUT} = -50 \mu\text{A}$ |
| | 3.0 17.0 | 4.5 5.5 | .61 | 3.86 4.86 | 3.70 4.70 | 3.76 4.76 | on Delay | $\begin{tabular}{ll} *V_{IN} = V_{IL} \mbox{ or } V_{IH} \\ -24 \mbox{ mA} \\ -24 \mbox{ mA} \end{tabular}$ |
| V _{OL} | Maximum Low Level Output Voltage | 4.5 5.5 | 0.001 0.001 | 0.1 0.1 | 0.1 0.1 0.5 16.6 0.1 | 0.1 0.1 0.1 | V | I _{OUT} = 50 μA |
| | a. 18,5 m | 4.5 5.5 | er as | 0.36 0.36 | 0.50 0.50 0.50 | 0.44 0.44 | V | $\begin{tabular}{ll} *V_{IN} = V_{IL} \mbox{ or } V_{IH} \\ I_{OL} & 24 \mbox{ mA} \\ & 24 \mbox{ mA} \\ \end{tabular}$ |
| I _{IN} | Maximum Input Leakage Current | 5.5 | St | ±0.1 | a.g ±1.0 _{0.01} | ±1.0 | μΑ | $V_{I} = V_{CC}$, GND |
| ГССТ | Maximum I _{CC} /Input | 5.5 | 0.6 | 0.1 | 0.0 1.6 8.01 | 1.5 | mA | $V_{\rm I} = V_{\rm CC} - 2.1V$ |
| I _{OLD} | †Minimum Dynamic | 5.5 | | | 50 | 75 | mA | V _{OLD} = 1.65V Max |
| I _{OHD} | Output Current | 5.5 | | 17.1 | -50 | -75 | mA | V _{OHD} = 3.85V Min |
| Icc | Maximum Quiescent Supply Current | 5.5 | S1 | 8.0 | 160.0 | 80.0 | μА | V _{IN} = V _{CC} or GND |

^{*}All outputs loaded; thresholds on input associated with output under test.

[†]Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC} . I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C

[†]Maximum test duration 2.0 ms, one output loaded at a time.

Note: ICC for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

| | | 0. | 70 | 74AC | | 54 | AC | 74 | AC | | |
|------------------|--|-----------------------|--|-------------|--------------|---|--------------|--|--------------|-------|-------------|
| Symbol | | V _{CC} * (V) | $T_A = +25^{\circ}C$ $C_L = 50 \text{ pF}$ | | | $T_A = -55^{\circ}C$ to + 125°C $C_L = 50 \text{ pF}$ | | T _A = -40°C to +85°C C _L = 50 pF | | Units | Fig. No. |
| | | | Min | Тур | Max | Min | Max | Min | Max | | |
| t _{PLH} | Propagation Delay S_n to Z or \overline{Z} | 3.3 5.0 | 3.0 2.5 | 11.5 8.5 | 18.0 13.0 | 1.0 1.0 | 22.0 15.5 | 3.0 2.0 | 20.0 15.0 | ns | 2-6 |
| t _{PHL} | Propagation Delay S_n to Z or \overline{Z} | 3.3 5.0 | 2.5 2.0 | 12.0 8.5 | 18.0 13.0 | 1.0 1.0 | 22.0 15.5 | 2.5 1.5 | 20.0 15.0 | ns | 2-6 |
| t _{PLH} | Propagation Delay E to Z or Z | 3.3 5.0 | 2.5 2.0 | 8.0 6.0 | 13.0 10.0 | 1.0 | 15.5 12.0 | 2.0 1.5 | 14.0 11.0 | ns | 2-6 |
| t _{PHL} | Propagation Delay E to Z or Z | 3.3 5.0 | 1.5 1.5 | 8.5 6.5 | 13.0 10.0 | 1.0 1.0 | 15.5 12.0 | 1.5 1.5 | 14.0 11.0 | ns | 2-6 |
| t _{PLH} | Propagation Delay I_n to Z or \overline{Z} | 3.3 5.0 | 2.5 1.5 | 9.5 7.0 | 14.0 10.5 | 1.0 | 16.0 12.0 | 2.0 1.5 | 15.5 11.0 | ns | 2-5 |
| t _{PHL} | Propagation Delay | 3.3 5.0 | 2.5 1.5 | 9.5 7.0 | 15.0 11.0 | 1.0 1.0 | 18.0 13.0 | 2.0 | 16.0 12.0 | ns | 2-5 |

^{*}Voltage Range 3.3 is 3.3V ± 0.3 V Voltage Range 5.0 is 5.0V ± 0.5 V

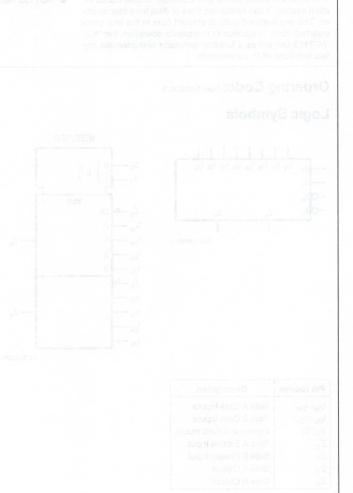
AC Electrical Characteristics

| | 034.0 | | | 74ACT | | 54 | ACT | 74/ | ACT | | - | |
|------------------|---|-----|-----|--|------|-----|---|-----|--|-------|-------|-------------|
| Symbol | Parameter | (V) | | T _A = +25°C C _L = 50 pF | | | $T_A = -55^{\circ}C$ to + 125°C $C_L = 50 pF$ | | $T_A = -40^{\circ}C$ to $+85^{\circ}C$ $C_L = 50 \text{ pF}$ | | Units | Fig. No. |
| | | | Min | Тур | Max | Min | Max | Min | Max | DUAL! | - | |
| tpLH | Propagation Delay S _n to Z | 5.0 | 3.5 | 12.5 | 15.5 | 1.0 | 19.5 | 3.0 | 17.0 | ns | 2-6 | |
| t _{PHL} | Propagation Delay S _n to Z | 5.0 | 3.5 | 12.5 | 15.5 | 1.0 | 20.0 | 3.0 | 16.5 | ns | 2-6 | |
| t _{PLH} | Propagation Delay S_n to \overline{Z} | 5.0 | 3.5 | 12.5 | 15.0 | 1.0 | 19.5 | 3.0 | 16.5 | ns | 2-6 | |
| t _{PHL} | Propagation Delay S_n to \overline{Z} | 5.0 | 4.0 | 12.5 | 16.5 | 1.0 | 20.0 | 3.5 | 18.5 | ns | 2-6 | |
| t _{PLH} | Propagation Delay | 5.0 | 2.5 | 10.0 | 9.5 | 1.0 | 12.0 | 2.5 | 10.0 | ns | 2-6 | |
| t _{PHL} | Propagation Delay E to Z | 5.0 | 2.5 | 10.5 | 9.0 | 1.0 | 12.5 | 2.5 | 10.0 | ns | 2-6 | |
| t _{PLH} | Propagation Delay E to Z | 5.0 | 2.5 | 10.0 | 8.5 | 1.0 | 12.0 | 2.5 | 9.5 | ns | 2-6 | |
| t _{PHL} | Propagation Delay E to Z | 5.0 | 3.0 | 10.5 | 10.0 | 1.0 | 12.5 | 2.5 | 10.5 | ns | 2-6 | |
| t _{PLH} | Propagation Delay In to Z | 5.0 | 3.5 | 11.0 | 11.5 | 1.0 | 15.0 | 3.0 | 12.5 | ns | 2-6 | |
| t _{PHL} | Propagation Delay In to Z | 5.0 | 3.5 | 11.0 | 12.0 | 1.0 | 16.0 | 3.0 | 13.5 | ns | 2-6 | |
| t _{PLH} | Propagation Delay I_n to \overline{Z} | 5.0 | 3.5 | 11.0 | 12.0 | 1.0 | 15.0 | 3.0 | 13.0 | ns | 2-6 | |
| t _{PHL} | Propagation Delay | 5.0 | 4.0 | 11.0 | 12.5 | 1.0 | 16.0 | 3.0 | 14.0 | ns | 2-6 | |

^{*}Voltage Range 5.0 is 5.0V ± 0.5 V

Capacitance

| Symbol | Parameter | AC/ACT | Units | Conditions | Maria Die |
|-----------------|----------------------------------|--------|--------|-----------------|-------------|
| Зуппоп | raiameter | Тур | Ollits | Collations | |
| C _{IN} | Input Capacitance | 4.5 | pF | $V_{CC} = 5.0V$ | MARKINA |
| C _{PD} | Power Dissipation Capacitance | 70.0 | pF | $V_{CC} = 5.0V$ | tueni-A isi |





54AC/74AC153 • 54ACT/74ACT153 **Dual 4-Input Multiplexer**

General Description

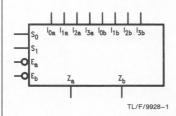
The 'AC/'ACT153 is a high-speed dual 4-input multiplexer with common select inputs and individual enable inputs for each section. It can select two lines of data from four sources. The two buffered outputs present data in the true (noninverted) form. In addition to multiplexer operation, the 'AC/ 'ACT153 can act as a function generator and generate any two functions of three variables.

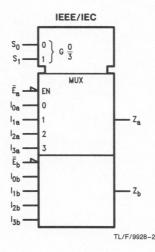
Features

- Outputs source/sink 24 mA
- 'ACT153 has TTL-compatible inputs

Ordering Code: See Section 5

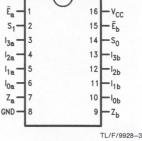
Logic Symbols



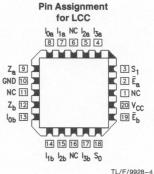


| | Assignr Flatpak | | DIC |
|-------------------|--------------------|----|------------------|
| Ē _a —1 | 0 | 16 | -v _{cc} |
| S ₁ -2 | | 15 | -Ē _b |
| | | | |

Connection Diagrams



| Pin Names | Description |
|----------------------------------|----------------------|
| I _{0a} -I _{3a} | Side A Data Inputs |
| I _{0b} -I _{3b} | Side B Data Inputs |
| S ₀ , S ₁ | Common Select Inputs |
| Ēa | Side A Enable Input |
| Ēb | Side B Enable Input |
| Za | Side A Output |
| Zb | Side B Output |



Functional Description

The 'AC/'ACT153 is a dual 4-input multiplexer. It can select two bits of data from up to four sources under the control of the common Select inputs $(S_0,\,S_1)$. The two 4-input multiplexer circuits have individual active-LOW Enables $(\overline{\mathbb{E}}_a,\,\overline{\mathbb{E}}_b)$ which can be used to strobe the outputs indepedently. When the Enables $(\overline{\mathbb{E}}_a,\,\overline{\mathbb{E}}_b)$ are HIGH, the corresponding outputs $Z_a,\,Z_b)$ are forced LOW. The 'ACT'ACT153 is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the Select inputs. The logic equations for the outputs are shown below.

$$\begin{split} Z_{a} &= \overline{E}_{a} \bullet (I_{0a} \bullet \overline{S}_{1} \bullet \overline{S}_{0} + I_{1a} \bullet \overline{S}_{1} \bullet S_{0} + I_{2a} \bullet S_{1} \bullet S_{0}) \\ I_{2a} \bullet S_{1} \bullet S_{0} + I_{3a} \bullet S_{1} \bullet S_{0}) \\ Z_{b} &= \overline{E}_{b} \bullet (I_{0b} \bullet \overline{S}_{1} \bullet \overline{S}_{0} + I_{1b} \bullet \overline{S}_{1} \bullet S_{0} + I_{2b} \bullet S_{1} \bullet S_{0} + I_{3b} \bullet S_{1} \bullet S_{0}) \end{split}$$

Truth Table

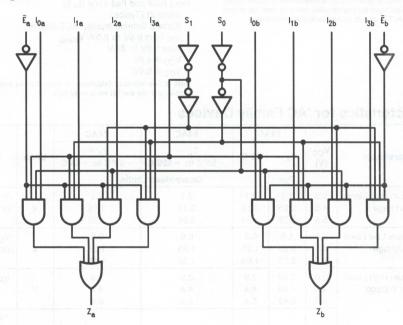
| | ect uts | HEDER HEDER HE BOX | Inpi | uts (a | or b) | | Output |
|----------------|----------------|--------------------------|----------------|------------|----------------|----------------|-------------------------|
| S ₀ | S ₁ | Ē | I ₀ | 11 | l ₂ | l ₃ | stov Z ig |
| X | Х | Н | X | X | X | X | iC Jogni C |
| L | L | L | L | Х | X | X | 0 2 E / |
| L | L | L | Н | Х | X | X | Н |
| Н | □ L' | L | Х | L (NOI) | X | X | evalunis Lituata 0 3 |
| Н | L | L | Х | Н | X | X | н |
| L | Н | L | Х | X | L | X | L |
| L | ○H ○ | L/c | X | X | Н | X | Н |
| Н | Н | L | Х | X | X | 90೬೦ | F. |
| Н | Н | L | X | X | X | Н | Н |

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Logic Diagram



TL/F/9928-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required. please contact the National Semiconductor Sales Office/Distributors for availability and specifications

| Office/ Distributors for availab | ility and specifications. |
|---|---|
| Supply Voltage (V _{CC}) | -0.5V to $+7.0V$ |
| DC Input Diode Current (I_{IK}) $V_I = -0.5V$ $V_I = V_{CC} + 0.5V$ | −20 mA +20 mA |
| DC Input Voltage (V _I) | -0.5V to V _{CC} + 0.5V |
| DC Output Diode Current (I_{OK}) $V_O = -0.5V$ $V_O = V_{CC} + 0.5V$ DC Output Voltage (V_O) | - 20 mA + 20 mA - 0.5V to to V _{CC} + 0.5V |
| DC Output Source or Sink Current (I _O) | ±50 mA |
| DC V _{CC} or Ground Current per Output Pin (I _{CC} or I _{GND}) | ± 50 mA |
| Storage Temperature (T _{STG}) | -65°C to +150°C |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

| Supply Voltage (V _{CC}) | |
|---|-----------------|
| 'AC | 200 to 600 |
| 'ACT | 4 5V to 5 5V |
| Input Voltage (V _I) | 01/1-1/ |
| Output Voltage (V _O) | |
| Operating Temperature (T _A) | |
| 74AC/ACT | -40°C to +85°C |
| 54AC/ACT | -55°C to +125°C |
| Junction Temperature (T _{.I}) | |
| CDIP | 175°C |
| PDIP | 140°C |
| input thoo and tall time (4, 4) | |
| (Note 2) (Typical) | |
| (Except Schmitt Inputs) 'AC Device | ces |
| V_{IN} from 30% to 70% of V_{CC} | |
| V _{CC} @ 3.0V | 150 ns/V |
| V _{CC} @ 4.5V | 40 ns/V |
| V _{CC} @ 5.5V | 25 ns/V |
| Input Rise and Fall Time (t _r , t _f) | |

(Note 2) (Typical)

(Except Schmitt Inputs) 'ACT Devices

VIN from 0.8V to 2.0V, Vmeas

from 0.8V to 2.0V

V_{CC} @ 4.5V V_{CC} @ 5.5V

10 ns/V 8 ns/V

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

| | | Proposition re- | 74 | AC | 54AC | 74AC | | |
|-----------------|--------------------------------------|------------------------|-------------------------|----------------------|-----------------------------------|---------------------------------|-------|---|
| Symbol | Parameter | V _{CC} (V) | T _A = | + 25°C | T _A = -55°C to + 125°C | T _A = -40°C to +85°C | Units | Conditions |
| | | | Тур | | Guaranteed L | imits | | |
| V _{IH} | Minimum High Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ |
| V _{IL} | Maximum Low Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ |
| V _{OH} | Minimum High Level Output Voltage | 3.0 4.5 5.5 | 2.99 4.49 5.49 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | ٧ | $I_{OUT} = -50 \mu\text{A}$ |
| | ngstep ngilupanna atsinusa a | 3.0 4.5 5.5 | son blands | 2.56 3.86 4.86 | 2.4 3.7 4.7 | 2.46 3.76 4.76 | v | $\label{eq:VIN} \begin{split} * V_{\text{IN}} &= V_{\text{IL}} \text{or} V_{\text{IH}} \\ &- 12 \text{mA} \\ I_{\text{OH}} &- 24 \text{mA} \\ &- 24 \text{mA} \end{split}$ |
| V _{OL} | Maximum Low Level Output Voltage | 3.0 4.5 5.5 | 0.002 0.001 0.001 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | V | $I_{OUT} = 50 \mu A$ |
| | | 3.0 4.5 5.5 | | 0.36 0.36 0.36 | 0.50 0.50 0.50 | 0.44 0.44 0.44 | v | $\label{eq:VIN} \begin{array}{c} *V_{\text{IN}} = V_{\text{IL}} \text{or} V_{\text{IH}} \\ & 12 \text{mA} \\ I_{\text{OL}} & 24 \text{mA} \\ & 24 \text{mA} \end{array}$ |
| I _{IN} | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | ±1.0 | μА | $V_{I} = V_{CC}$, GND |

DC Characteristics for 'AC Family Devices (Continued) is a second of the continued of the c

| | TARC | | 74 | AC | 54AC CART | 74AC | | |
|--------|-------------------------------------|------------------------|--------------------|----------|----------------------------------|---------------------------------|-------|--|
| Symbol | Parameter | V _{CC} (V) | T _A + 2 | = 5°C | T _A = -55°C to +125°C | T _A = -40°C to +85°C | Units | Conditions |
| | 3q 90 = 10 | - | Тур | 19 | Guaranteed I | Limits | | |
| lold | †Minimum Dynamic | 5.5 | 120 | nien | 50 | 75 | mA | V _{OLD} = 1.65V Max |
| IOHD | Output Current | 5.5 | | 0.1 | -50 | 0 × −75 0 8 | mA | V _{OHD} = 3.85V Min |
| Icc | Maximum Quiescent Supply Current | 5.5 | Br | 8.0 | 160.0 | 80.0 | μΑ | V _{IN} = V _{CC} or GND |

^{*}All outputs loaded; thresholds on input associated with output under test.

DC Characteristics for 'ACT Family Devices

| | 1.5 10.5 1 | | 744 | СТ | 54ACT | 74ACT | | ny or a |
|------------------|--------------------------------------|------------------------|-----------------------|--------------|----------------------------------|---------------------------------|-----------|---|
| Symbol | Parameter | V _{CC} (V) | T _A + 2 | = 5°C | T _A = -55°C to +125°C | T _A = -40°C to +85°C | Units | Conditions |
| | | | Тур | | Guaranteed L | imits | Va.o.t V | Vottage Ranga 5.0 is 5. |
| V _{IH} | Minimum High Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 2.0 | 2.0 | 2.0 2.0 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ |
| V _{IL} | Maximum Low Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 0.8 | 0.8 0.8 | 0.8 0.8 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ |
| Vон | Minimum High Level Output Voltage | 4.5 5.5 | 4.49 5.49 | 4.4 5.4 | 4.4 5.4 | 4.4 (V) 5.4 | V | $I_{OUT} = -50 \mu A$ |
| | msw niw | 4.5 5.5 | ld: | 3.86 4.86 | 3.70 4.70 | 3.76 4.76 | rsio O na | $V_{\text{IN}} = V_{\text{IL}} \text{ or } V_{\text{IH}}$ -24 mA -24 mA |
| V _{OL} | Maximum Low Level Output Voltage | 4.5 5.5 | 0.001 | 0.1 | 7.0 1.0 11.5 | 0.8 0.1 0.0 0.1 | V | I _{OUT} = 50 μA |
| | an 3.S1 0.S an -0.11 3.S | 4.5 5.5 | 18. | 0.36 0.36 | 0.50 0.50 | 0.44 | V | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IN} = V_{IL} \text{ or } V_{IH}$ |
| I _{IN} | Maximum Input Leakage Current | 5.5 | \$1 | ±0.1 | ±1.0 | ± 1.0 | μΑ | $V_I = V_{CC}$, GND |
| ГССТ | Maximum I _{CC} /Input | 5.5 | 0.6 | 0.1 | 8.8 1.6 A.B | 0.5 1.5 | mA | $V_{\rm I} = V_{\rm CC} - 2.1V$ |
| I _{OLD} | †Minimum Dynamic | 5.5 | | | 50 | 75 | mA | V _{OLD} = 1.65V Max |
| IOHD | Output Current | 5.5 | | | -50 | −75 | mA | V _{OHD} = 3.85V Min |
| Icc | Maximum Quiescent Supply Current | 5.5 | 3 | 8.0 | 160.0 | 80.0 | μА | V _{IN} = V _{CC} or GND |

^{*}All outputs loaded; thresholds on input associated with output under test.

[†]Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}. I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

[†]Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

| | | 0 | 7.5 | 74AC | 68A | 54 | AC | 74 | AC | | |
|------------------|--|-------------------|--|-----------------------|--------------|------------|-------------------------|------------|------------------------|-------|-------------|
| Symbol | Parameter | V _{CC} * | The state of the s | C _L = +25° | | to + | -55°C 125°C 50 pF | to + | -40°C 85°C 50 pF | Units | Fig. No. |
| | | | Min | Тур | Max | Min | Max | Min | Max | | |
| t _{PLH} | Propagation Delay S _n to Z _n | 3.3 5.0 | 2.5 2.0 | 9.5 6.5 | 15.0 11.0 | 1.0 1.0 | 19.5 14.0 | 2.5 2.0 | 17.5 12.5 | ns | 2-6 |
| t _{PHL} | Propagation Delay S _n to Z _n | 3.3 5.0 | 3.0 2.5 | 8.5 6.5 | 14.5 11.0 | 1.0 1.0 | 18.0 13.5 | 2.5 2.0 | 16.5 12.0 | ns | 2-6 |
| t _{PLH} | Propagation Delay E to Z _n | 3.3 5.0 | 2.5 1.5 | 8.0 5.5 | 13.5 9.5 | 1.0 1.0 | 16.5 12.5 | 2.0 1.5 | 16.0 11.0 | ns | 2-6 |
| t _{PHL} | Propagation Delay E to Z _n | 3.3 5.0 | 2.5 2.0 | 7.0 5.0 | 11.0 8.0 | 1.0 1.0 | 14.0 10.0 | 2.0 1.5 | 12.5 9.0 | ns | 2-6 |
| t _{PLH} | Propagation Delay | 3.3 5.0 | 2.5 1.5 | 7.5 5.5 | 12.5 9.0 | 1.0 1.0 | 16.0 11.5 | 2.0 1.5 | 14.5 10.5 | ns | 2-5 |
| t _{PHL} | Propagation Delay | 3.3 5.0 | 1.5 1.5 | 7.0 5.0 | 11.5 8.5 | 1.0 1.0 | 14.5 10.5 | 1.5 1.5 | 13.0 10.0 | ns | 2-5 |

^{*}Voltage Range 3.3 is 3.3V ± 0.3 V Voltage Range 5.0 is 5.0V ± 0.5 V

AC Electrical Characteristics

| | | | | 74ACT | | 54 | ACT | 74/ | ACT | Les N | 1 |
|------------------|---|-----------------------|-----|------------------------|------|------|---------------------------|------|------------------------|-------|------|
| Symbol | Parameter | V _{CC} * (V) | | C _L = +25°C | | to + | −55°C 125°C = 50 pF | to + | -40°C 85°C 50 pF | Units | Fig. |
| | | ** | Min | Тур | Max | Min | Max | Min | Max | 2170 | |
| t _{PLH} | Propagation Delay S _n to Z _n | 5.0 | 3.0 | 7.0 | 11.5 | 1.0 | 15.0 | 2.0 | 13.5 | ns | 2-6 |
| t _{PHL} | Propagation Delay S _n to Z _n | 5.0 | 3.0 | 7.0 | 11.5 | 1.0 | 14.5 | 2.5 | 13.5 | ns | 2-6 |
| t _{PLH} | Propagation Delay \overline{E}_n to Z_n | 5.0 | 2.0 | 6.5 | 10.5 | 1.0 | 13.5 | 2.0 | 12.5 | ns | 2-6 |
| t _{PHL} | Propagation Delay \overline{E}_n to Z_n | 5.0 | 3.0 | 6.0 | 9.5 | 1.0 | 11.5 | 2.5 | 11.0 | ns | 2-6 |
| t _{PLH} | Propagation Delay | 5.0 | 2.5 | 5.5 | 9.5 | 1.0 | 12.5 | 2.0 | 11.0 | ns | 2-5 |
| t _{PHL} | Propagation Delay | 5.0 | 2.0 | 5.5 | 9.5 | 1.0 | 12.0 | 2.0 | 11.0 | ns | 2-5 |

^{*}Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

| Symbol | Parameter | AC/ACT | Units | Conditions |
|-----------------|----------------------------------|--------|------------------|------------------------|
| Symbol | rarameter | Тур | Jeét repnir Ards | |
| CIN | Input Capacitance | 4.5 | pF | $V_{CC} = 5.0V$ |
| C _{PD} | Power Dissipation Capacitance | 65.0 | pF | V _{CC} = 5.0V |



54AC/74AC157 • 54ACT/74ACT157 Quad 2-Input Multiplexer

General Description

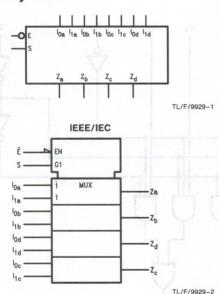
The 'AC/'ACT157 is a high-speed quad 2-input multiplexer. Four bits of data from two sources can be selected using the common Select and Enable inputs. The four outputs present the selected data in the true (noninverted) form. The 'AC/'ACT157 can also be used as a function generator.

Features

- Outputs source/sink 24 mA
- 'ACT157 has TTL-compatible inputs

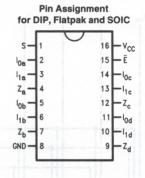
Ordering Code: See Section 5

Logic Symbols

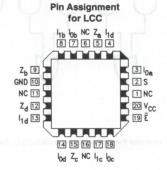


| Pin Names | Description |
|----------------------------------|----------------------|
| $I_{0a} - I_{0d}$ | Source 0 Data Inputs |
| I _{1a} -I _{1d} | Source 1 Data Inputs |
| Ē | Enable Input |
| S | Select Input |
| $Z_a - Z_d$ | Outputs |

Connection Diagrams



TL/F/9929-3



TL/F/9929-4

Functional Description

The 'AC/'ACT157 is a quad 2-input multiplexer. It selects four bits of data from two sources under the control of a common Select input (S). The Enable input (Ē) is active-LOW. When Ē is HIGH, all of the outputs (Z) are forced LOW regardless of all other inputs. The 'AC/'ACT157 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$$Z_a = \overline{E} \bullet (I_{1a} \bullet S + I_{0a} \bullet \overline{S})$$

$$Z_b = \overline{E} \bullet (I_{1b} \bullet S + I_{0b} \bullet \overline{S})$$

$$Z_c = \overline{E} \bullet (I_{1c} \bullet S + I_{0c} \bullet \overline{S})$$

$$Z_d = \overline{E} \bullet (I_{1d} \bullet S + I_{0d} \bullet \overline{S})$$

A common use of the 'AC/ACT157 is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select input. A less obvious use is

as a function generator. The 'AC/'ACT157 can generate any four of the sixteen different functions of two variables with one variable common. This is useful for implementing gating functions.

Truth Table

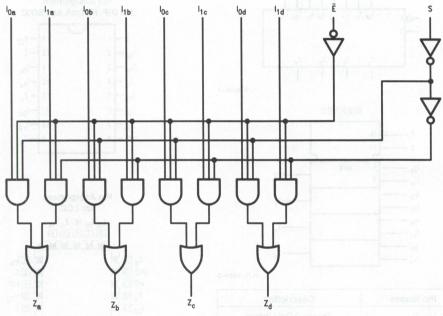
| | Outputs | | | | |
|-----------|-------------|----------------|----------------|--------------|--|
| Ē | S | I ₀ | l ₁ | Z | |
| Н | X | X | X | ANDA LIT | |
| set Liles | of H | X | coul Lates | o alid L | |
| L of | H | X | H | ommos Hrd | |
| P. Lange | ou, Enter | nt nLates | X | eru ineagard | |
| Logo | nul area ba | Н | X | A SOA HILL | |

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Logic Diagram



TL/F/9929-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1) Recommended Operating

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Supply Voltage (V _{CC}) | -0.5V to $+7.0$ V |
|---|--|
| DC Input Diode Current (I_{IK}) $V_I = -0.5V$ $V_I = V_{CC} + 0.5V$ | -20 mA +20 mA |
| DC Input Voltage (V _I) | -0.5 V to $V_{CC} + 0.5$ V |
| DC Output Diode Current (I_{OK}) $V_O = -0.5V$ $V_O = V_{CC} + 0.5V$ DC Output Voltage (V_O) DC Output Source or Sink Current (I_O) | $-20 \text{ mA} + 20 \text{ mA} -0.5 \text{V to to V}_{CC} + 0.5 \text{V}$ |
| DC V _{CC} or Ground Current per Output Pin (I _{CC} or I _{GND}) | |
| Storage Temperature (T _{STG}) | -65°C to +150°C |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

Recommended Operating Conditions

| Supply Voltage (V _{CC}) | |
|---|-----------------------------|
| 'AC | 2.0V to 6.0V |
| 'ACT | 4.5V to 5.5V |
| Input Voltage (V _I) | 0V to V _{CC} |
| Output Voltage (V _O) | 0V to V _{CC} |
| Operating Temperature (| |
| 74AC/ACT | -40°C to +85°C |
| 54AC/ACT | -55°C to +125°C |
| Junction Temperature (T | (L' |
| CDIP | 175°C |
| PDIP | 140°C |
| Input Rise and Fall Time (Note 2) (Typical) (Except Schmitt Inputs V _{IN} from 30% to 70% | s) 'AC Devices |
| V _{CC} @ 3.0V | 150 ns/V |
| V _{CC} @ 4.5V | 40 ns/V |
| V _{CC} @ 5.5V | 25 ns/V |
| Input Rise and Fall Time (Note 2) (Typical) (Except Schmitt Inputs | s) 'ACT Devices |
| V _{IN} from 0.8V to 2.0V, from 0.8V to 2.0V | V meas |
| V _{CC} @ 4.5V | 10 ns/V |
| V _{CC} @ 5.5V | 9 no /\/ |
| | level woul mumbss. 6 1157 V |

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

| Symbol | Parameter | V _{CC} (V) | 74AC | | 54AC | 74AC | Units | |
|----------------------------------|--------------------------------------|---------------------|-------------------------|----------------------|----------------------------------|---|---------------------|--|
| | | | | | T _A = -55°C to +125°C | T _A = -40°C to +85°C | | Conditions |
| | | | Тур | | Guaranteed L | imits | SLI WO I S Anado | Martines I JoV |
| V _{IH} _{IV} so | Minimum High Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ |
| V _{IL} | Maximum Low Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | teant n | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ |
| V _{OH} | Minimum High Level Output Voltage | 3.0 4.5 5.5 | 2.99 4.49 5.49 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | V | $I_{OUT} = -50 \mu\text{A}$ |
| | - OMOV Ans | 7.5 | | | 08- | 2.3 | METER | *VIN = VIL or VIH |
| | OV = 101V A41 J = VO | 3.0 4.5 5.5 | 8 | 2.56 3.86 4.86 | 2.4 3.7 4.7 | 2.46 3.76 4.76 | V | -12 mA I _{OH} -24 mA -24 mA |
| V _{OL} | Maximum Low Level Output Voltage | 3.0 4.5 5.5 | 0.002 0.001 0.001 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | oracle is 6.0.1 hashed or 0.1 V or hashed 0.1 | 1 | $I_{OUT} = 50 \mu A$ |
| | | 3.0 4.5 5.5 | | 0.36 0.36 0.36 | 0.50 0.50 0.50 | 0.44 0.44 0.44 | ٧ | $\begin{tabular}{ll} *V_{\mbox{\scriptsize IN}} &= V_{\mbox{\scriptsize IL}} \mbox{\scriptsize or} \mbox{\scriptsize $V_{\mbox{\scriptsize IH}}$} \\ &= 12 \mbox{\scriptsize mA} \\ I_{\mbox{\scriptsize OL}} &= 24 \mbox{\scriptsize mA} \\ &= 24 \mbox{\scriptsize mA} \\ \end{tabular}$ |
| I _{IN} | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | ± 1.0 | μΑ | $V_{I} = V_{CC}$, GND |

DC Characteristics for 'AC Family Devices (Continued) Parish Continued (Continued)

| Symbol | Parameter | V _{CC} (V) | 74AC T _A = + 25°C | | 54AC | 74AC T _A = -40°C to +85°C | Units | Conditions |
|------------------|-------------------------------------|---------------------|------------------------------------|------------------|----------------------------------|--|----------|--|
| | | | | | T _A = -55°C to +125°C | | | |
| | | | Тур | gátlov | Guaranteed | Limits | (AL) the | PO Inpot Bigde Cum |
| I _{OLD} | †Minimum Dynamic Output Current | 5.5 | (OA) a6 | stleV | 50 Am 05 - | 75 | mA | V _{OLD} = 1.65V Max |
| IOHD | | 5.5 | ENGREE | or group GANO | -50 | √ 0 V −75 | mA | V _{OHD} = 3.85V Min |
| Icc | Maximum Quiescent Supply Current | 5.5 | T tipperati | 8.0 | 160.0 100 | 80.0 | μА | V _{IN} = V _{CC} or GND |

^{*}All outputs loaded; thresholds on input associated with output under test.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}. I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

| Symbol | Parameter (a | | 744 | CT | 54ACT | 74ACT | acrida m | mixem etitlowith it allow |
|------------------|--------------------------------------|---------------------|-------------------------|--------------|----------------------------------|---------------------------------|----------|--|
| | | V _{CC} (V) | T _A = + 25°C | | T _A = -55°C to +125°C | T _A = -40°C to +85°C | Units | Conditions |
| | | | Тур | S Ideox | Guaranteed L | imits | andone 4 | ikan io notsiago bisam |
| V _{IH} | Minimum High Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 2.0 2.0 | 2.0 2.0 | 2.0 2.0 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ |
| V _{IL} | Maximum Low Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 0.8 0.8 | 0.8 0.8 | 0.8 0.8 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ |
| V _{OH} | Minimum High Level Output Voltage | 4.5 5.5 | 4.49 5.49 | 4.4 5.4 | 4.4 5.4 | 4.4 5.4 | V | $I_{OUT} = -50 \mu\text{A}$ |
| encil | units Cons | 4.5 5.5 | S . | 3.86 4.86 | 3.70 4.70 | 3.76 4.76 | V | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IOH} = -24 \text{ mA}$ $V_{IOH} = -24 \text{ mA}$ |
| V _{OL} | Maximum Low Level Output Voltage | 4.5 5.5 | 0.001 0.001 | 0.1 0.1 | 0.1 0.1 | 0.1 0.1 | ٧ | $I_{OUT} = 50 \mu A$ |
| V: 0 | TipuoV apV-1p V | 4.5 5.5 | | 0.36 0.36 | 0.50 0.50 | 0.44 0.44 | egs V | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ |
| I _{IN} | Maximum Input Leakage Current | 5.5 | | ±0.1 | e.0 e.0 | 38 ± 1.0 | μА | $V_I = V_{CC}$, GND |
| Ісст | Maximum I _{CC} /Input | 5.5 | 0.6 | | 8.5 1.6 | 99.9. 1.50.8 | mA | $V_{\rm I} = V_{\rm CC} - 2.1V$ |
| I _{OLD} | †Minimum Dynamic | 5.5 | | | 50 | 75 | mA | V _{OLD} = 1.65V Max |
| IOHD | Output Current | 5.5 | | | -50 | -75 | mA | V _{OHD} = 3.85V Min |
| lcc | Maximum Quiescent Supply Current | 5.5 | | 8.0 | NS 160.0 88.3 | 80.0 | μА | V _{IN} = V _{CC} or GND |

^{*}All outputs loaded; thresholds on input associated with output under test.

[†]Maximum test duration 2.0 ms, one output loaded at a time.

[†]Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

| Symbol | | | | 74AC | | 54 | AC | 74 | AC | | |
|------------------|--|--------------------------|--|------------|-------------|--|--------------|--|--------------|-------|-------------|
| | Parameter | V _{CC} * (V) | T _A = +25°C C _L = 50 pF | | | $T_A = -55^{\circ}C$ to $+ 125^{\circ}C$ $C_L = 50 pF$ | | T _A = -40°C to +85°C C _L = 50 pF | | Units | Fig. No. |
| | | | Min | Тур | Max | Min | Max | Min | Max | o ha | 110 |
| t _{PLH} | Propagation Delay S to Z _n | 3.3 5.0 | 1.5 1.5 | 7.0 5.5 | 11.5 9.0 | 1.0 1.0 | 16.0 12.0 | 1.5 1.5 | 13.0 10.0 | ns | 2-6 |
| t _{PHL} | Propagation Delay S to Z _n | 3.3 5.0 | 1.5 1.5 | 6.5 5.0 | 11.0 8.5 | 1.0 1.0 | 14.0 11.5 | 1.5 1.0 | 12.0 9.5 | ns | 2-6 |
| t _{PLH} | Propagation Delay E to Z _n | 3.3 5.0 | 1.5 1.5 | 7.0 5.5 | 11.5 9.0 | 1.0 1.0 | 16.0 12.0 | 1.5 1.5 | 13.0 | ns | 2-6 |
| t _{PHL} | Propagation Delay E to Z _n | 3.3 5.0 | 1.5 1.5 | 6.5 5.5 | 11.0 9.0 | 1.0 1.0 | 14.0 11.5 | 1.5 1.0 | 12.0 9.5 | ns | 2-6 |
| t _{PLH} | Propagation Delay | 3.3 5.0 | 1.5 1.5 | 5.0 4.0 | 8.5 6.5 | 1.0 1.0 | 11.0 9.0 | 1.0 1.0 | 9.0 7.0 | ns | 2-5 |
| t _{PHL} | Propagation Delay | 3.3 5.0 | 1.5 1.5 | 5.0 4.0 | 8.0 6.5 | 1.0 1.0 | 11.0 9.0 | 1.0 1.0 | 9.0 7.0 | ns | 2-5 |

*Voltage Range 3.3 is 3.3V \pm 0.3V Voltage Range 5.0 is 5.0V \pm 0.5V

AC Electrical Characteristics

| Symbol | .d (1) 20 10 10 10 10 10 10 10 10 10 10 10 10 10 | V _{CC} * (V) | | 74ACT | | | 54ACT | | ACT | | |
|------------------|--|--------------------------|------------------------------------|-------|------|---|-------|--|------|-------|-------------|
| | Parameter | | $T_{A}=+25^{\circ}C$ $C_{L}=50$ pF | | | $T_A = -55^{\circ}C$ to + 125°C $C_L = 50 pF$ | | T _A = -40°C to +85°C C _L = 50 pF | | Units | Fig. No. |
| | MANA | | Min | Тур | Max | Min | Max | Min | Max | | |
| t _{PLH} | Propagation Delay S to Z _n | 5.0 | 2.0 | 5.5 | 9.0 | 1.0 | 11.5 | 1.5 | 10.0 | ns | 2-6 |
| t _{PHL} | Propagation Delay S to Z _n | 5.0 | 2.0 | 5.5 | 9.5 | 1.0 | 11.5 | 2.0 | 10.5 | ns | 2-6 |
| t _{PLH} | Propagation Delay | 5.0 | 1.5 | 6.0 | 10.0 | 1.0 | 12.0 | 1.5 | 11.5 | ns | 2-6 |
| t _{PHL} | Propagation Delay E to Z _n | 5.0 | 1.5 | 5.0 | 8.5 | 1.0 | 10.0 | 1.0 | 9.0 | ns | 2-6 |
| t _{PLH} | Propagation Delay | 5.0 | 1.5 | 4.0 | 7.0 | 1.0 | 8.5 | 1.0 | 8.5 | ns | 2-5 |
| t _{PHL} | Propagation Delay In to Zn | 5.0 | 1.5 | 4.5 | 7.5 | 1.0 | 9.0 | 1.0 | 8.5 | ns | 2-5 |

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

| Symbol | Parameter | AC/ACT | Units | Conditions |
|-----------------|----------------------------------|--------|-------|-----------------|
| Symbol | rarameter | Тур | Onits | Conditions |
| C _{IN} | Input Capacitance | 4.5 | pF | $V_{CC} = 5.0V$ |
| C _{PD} | Power Dissipation Capacitance | 50.0 | pF | $V_{CC} = 5.0V$ |



54AC/74AC158 • 54ACT/74ACT158 Quad 2-Input Multiplexer

General Description

The 'AC/'ACT158 is a high-speed quad 2-input multiplexer. It selects four bits of data from two sources using the common Select and Enable inputs. The four buffered outputs present the selected data in the inverted form. The 'AC/'ACT158 can also be used as a function generator.

Features

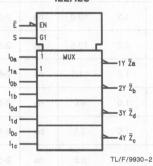
- Outputs source/sink 24 mA
- 'ACT158 has TTL-compatible inputs

Ordering Code: See Section 5

Logic Symbols

IEE/IEC

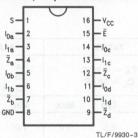
TL/F/9930-1



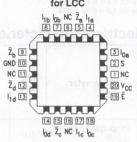
| Pin Names | Description |
|----------------------------------|----------------------|
| l _{0a} -l _{0d} | Source 0 Data Inputs |
| l _{1a} -l _{1d} | Source 1 Data Inputs |
| Ē | Enable Input |
| S | Select Input |
| Z _a -Z̄ _d | Inverted Outputs |

Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



Pin Assignment for LCC



TL/F/9930-4

Functional Description

The 'AC/'ACT158 quad 2-input multiplexer selects four bits of data from two sources under the control of a common Select input (S) and presents the data in inverted form at the four outputs. The Enable input (\overline{E}) is active-LOW. When \overline{E} is HIGH, all of the outputs (\overline{Z}) are forced HIGH regardless of all other inputs. The 'AC/'ACT158 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input.

A common use of the 'AC/'ACT158 is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select input. A less obvious use is as a function generator. The 'AC/'ACT158 can generate four functions of two variables with one variable common. This is useful for implementing gating functions.

Truth Table

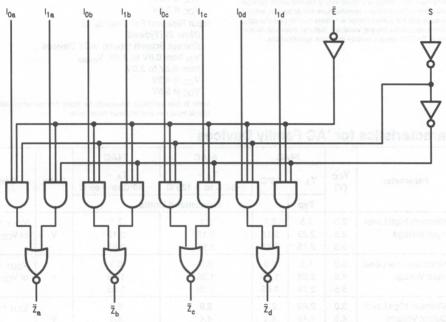
| | Inp | Outputs | | |
|------|-----|----------------|--------------|-------------------|
| E | S S | I ₀ | liova 191 es | midhie Z |
| H | X | X | X | V) egali H vigotu |
| L | L | L | X | O short Hoom Of |
| L | L | Н | X | A8.0 L - W |
| L | Н | X | L | Н |
| VO Q | H | X | H (19) | aberron Indut or |

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Logic Diagram



TL/F/9930-

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications

| Office/ Distributors for availab | mity and specifications. |
|--|-----------------------------------|
| Supply Voltage (V _{CC}) | -0.5V to $+7.0V$ |
| DC Input Diode Current (I_{IK}) $V_I = -0.5V$ | -20 mA |
| $V_{I} = V_{CC} + 0.5V$ | + 20 mA |
| DC Input Voltage (V _I) | $-0.5V$ to $V_{CC} + 0.5V$ |
| DC Output Diode Current (I_{OK}) $V_O = -0.5V$ $V_O = V_{CC} + 0.5V$ | −20 mA +20 mA |
| DC Output Voltage (V _O) | -0.5 V to to V_{CC} + 0.5 V |
| DC Output Source or Sink Current (I _O) | ±50 mA |
| DC V _{CC} or Ground Current per Output Pin (I _{CC} or I _{GND}) | ±50 mA |
| Storage Temperature (T _{STG}) | -65°C to +150°C |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

| Supply Voltage (V _{CC}) | |
|--|-----------------|
| 'AC | 2 UV TO B UV |
| 'ACT | 4.5V TO 5.5V |
| Input Voltage (V _I) | 01/4-1/ |
| Output Voltage (V _O) | |
| Operating Temperature (T _A) | |
| 74AC/ACT | -40°C to +85°C |
| 54AC/ACT | -55°C to +125°C |
| Junction Temperature (T _J) | |
| CDIP | 175°C |
| PDIP GIVGO aset A duotil hosted entitle | 140°C |
| input Rise and Fall Time (L. G) | |
| (Except Schmitt Inputs) 'AC Devices | |
| V _{IN} from 30% to 70% of V _{CC} | |
| V _{CC} @ 3.0V | 150 ns/V |
| V _{CC} @ 4.5V | 40 ns/V |
| V _{CC} @ 5.5V | 25 ns/V |
| Input Rise and Fall Time (t _r , t _f) (Note 2) (Typical) | |
| (Except Schmitt Inputs) 'ACT Devices | |
| V _{IN} from 0.8V to 2.0V, V _{meas} | |
| III IIIeas | |

V_{CC} @ 5.5V Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

10 ns/V

8 ns/V

from 0.8V to 2.0V V_{CC} @ 4.5V

DC Characteristics for 'AC Family Devices

| | | | 74 | AC | 54AC | 74AC | at many | | |
|-----------------|--------------------------------------|---------------------|-------------------------|----------------------|----------------------------------|---------------------------------|---------|---|--|
| Symbol | Parameter | V _{CC} (V) | T _A = +25°C | | T _A = -55°C to +125°C | T _A = -40°C to +85°C | Units | Conditions | |
| | | | Тур | and the | Guaranteed L | imits | | V | |
| V _{IH} | Minimum High Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | V | V _{OUT} = 0.1V or V _{CC} - 0.1V | |
| V _{IL} | Maximum Low Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{OH} | Minimum High Level Output Voltage | 3.0 4.5 5.5 | 2.99 4.49 5.49 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | V | $I_{OUT} = -50 \mu\text{A}$ | |
| | | 3.0 4.5 5.5 | | 2.56 3.86 4.86 | 2.4 3.7 4.7 | 2.46 3.76 4.76 | ٧ | $*V_{IN} = V_{IL} \text{ or } V_{IH} - 12 \text{ m/s}$ $I_{OH} - 24 \text{ m/s}$ -24 m/s | |
| V _{OL} | Maximum Low Level Output Voltage | 3.0 4.5 5.5 | 0.002 0.001 0.001 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | V | I _{OUT} = 50 μA | |
| | | 3.0 4.5 5.5 | | 0.36 0.36 0.36 | 0.50 0.50 0.50 | 0.44 0.44 0.44 | V | $V_{IN} = V_{IL} \text{ or } V_{IH}$ 12 m/s $I_{OL} \qquad 24 \text{ m/s}$ 24 m/s | |
| I _{IN} | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | ±1.0 | μΑ | $V_{I} = V_{CC}$, GND | |

DC Characteristics for 'AC Family Devices (Continued)

| Symbol | Parameter | | 74AC | | 54AC | 74AC | | |
|------------------|-------------------------------------|---------------------|------------------|--------|----------------------------------|---------------------------------|-------|--|
| | | V _{CC} (V) | T _A = | + 25°C | T _A = -55°C to +125°C | T _A = -40°C to +85°C | Units | Conditions |
| | | | Тур | jul | Guaranteed Li | mits | | |
| IOLD | †Minimum Dynamic | 5.5 | SALES | ANTINE | 50 | 75 | mA | V _{OLD} = 1.65V Max |
| I _{OHD} | Output Current | 5.5 | | 0.1 | -50 | -75 | mA | V _{OHD} = 3.85V Min |
| Icc | Maximum Quiescent Supply Current | 5.5 | | 8.0 | 160.0 | 80.0 | μА | V _{IN} = V _{CC} or GND |

^{*}All outputs loaded; thresholds on input associated with output under test.

DC Characteristics for 'ACT Family Devices

| | | | 74A | СТ | 54ACT | 74ACT | | 11/2 (21) | |
|------------------|-------------------------------------|---------------------|------------------------|--------------|----------------------------------|---------------------------------|---------|--|--|
| Symbol | Parameter | V _{CC} (V) | T _A = +25°C | | T _A = -55°C to +125°C | T _A = -40°C to +85°C | Units | Conditions | |
| | | | Тур | | Guaranteed L | imits | ASOF AS | 3 Place Reson S.D 1916 | |
| V _{IH} | Minimum High Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 2.0 | 2.0 2.0 | 2.0 2.0 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{IL} | Maximum Low Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 0.8 | 0.8 0.8 | 0.8 0.8 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{OH} | Minimum High Level Output Voltage | 4.5 5.5 | 4.49 5.49 | 4.4 5.4 | 4.4 5.4 | 4.4 5.4 | V | $I_{OUT} = -50 \mu\text{A}$ | |
| | en 0,51 0.5 | 4.5 5.5 | 0.51 | 3.86 4.86 | 3.70 4.70 | 3.76 4.76 | V | $\begin{tabular}{ll} *V_{IN} &= V_{IL} \mbox{ or } V_{IH} \\ &-24 \mbox{ mA} \\ &-24 \mbox{ mA} \end{tabular}$ | |
| V _{OL} | Maximum Low Level Output Voltage | 4.5 5.5 | 0.001 | 0.1 | 0.8 0.1 d.d 0.1 | 0.1 | V | I _{OUT} = 50 μA | |
| | 1.5 10.5 na | 4.5 5.5 | 0.11 | 0.36 0.36 | 0.50 0.50 | 0.44 0.44 | ٧ | $\begin{tabular}{ll} *V_{IN} &= V_{IL} \mbox{ or } V_{IH} \\ I_{OL} & 24 \mbox{ mA} \\ & 24 \mbox{ mA} \\ \end{tabular}$ | |
| I _{IN} | Maximum Input Leakage Current | 5.5 | 8.6 | ±0.1 | ±1.0 | ±1.0 | μΑ | $V_I = V_{CC}$, GND | |
| Ісст | Maximum I _{CC} /Input | 5.5 | 0.6 | 0.1 | 1.6 _{0.8} | 1.5 | mA | $V_I = V_{CC} - 2.1V$ | |
| IOLD | †Minimum Dynamic | 5.5 | | | 50 | 75 | mA | V _{OLD} = 1.65V Max | |
| I _{OHD} | Output Current | 5.5 | | | -50 | -75 | mA | V _{OHD} = 3.85V Min | |
| Icc | Maximum Quiescent Supply Current | 5.5 | | 8.0 | 160.0 | 80.0 | μΑ | V _{IN} = V _{CC} or GND | |

^{*}All outputs loaded; thresholds on input associated with output under test.

[†]Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

[†]Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

| Symbol | | V _{CC} * | | 74AC | | 54 | AC | 74 | AC | | |
|------------------|--|-------------------|--|------------|-------------|--|--------------|--|--------------|-------|------|
| | Parameter | | T _A = +25°C C _L = 50 pF | | | $T_A = -55^{\circ}C$ to $+ 125^{\circ}C$ $C_L = 50 pF$ | | $T_A = -40^{\circ}C$ to $+85^{\circ}C$ $C_L = 50 pF$ | | Units | Fig. |
| | | | Min | Тур | Max | Min | Max | Min | Max | | |
| t _{PLH} | Propagation Delay S to \overline{Z}_n | 3.3 5.0 | 1.5 1.5 | 7.0 5.5 | 11.5 9.0 | 1.0 1.0 | 14.0 11.0 | 1.5 1.0 | 12.5 9.5 | ns | 2-6 |
| t _{PHL} | Propagation Delay S to \overline{Z}_n | 3.3 5.0 | 1.5 1.5 | 7.0 5.5 | 11.5 9.0 | 1.0 | 14.0 11.0 | 1.5 1.5 | 12.5 10.0 | ns | 2-6 |
| t _{PLH} | Propagation Delay \overline{E} to \overline{Z}_n | 3.3 5.0 | 1.5 1.5 | 7.5 6.0 | 12.0 9.5 | 1.0 1.0 | 15.0 12.0 | 1.5 1.5 | 13.0 10.5 | ns | 2-6 |
| t _{PHL} | Propagation Delay \overline{E} to \overline{Z}_n | 3.3 5.0 | 1.5 1.5 | 7.0 5.5 | 11.0 8.5 | 1.0 1.0 | 14.0 10.0 | 1.5 1.0 | 12.0 9.5 | ns | 2-6 |
| t _{PLH} | Propagation Delay I_n to \overline{Z}_n | 3.3 5.0 | 1.5 1.5 | 5.5 4.0 | 9.0 7.0 | 1.0 1.0 | 11.0 8.5 | 1.5 1.0 | 10.0 7.5 | ns | 2-5 |
| t _{PHL} | Propagation Delay I_n to \overline{Z}_n | 3.3 5.0 | 1.5 1.5 | 5.0 4.0 | 8.0 6.5 | 1.0 1.0 | 10.0 7.5 | 1.0 1.0 | 8.5 6.5 | ns | 2-5 |

^{*}Voltage Range 3.3 is 3.3V ± 0.3 V Voltage Range 5.0 is 5.0V ± 0.5 V

AC Electrical Characteristics

| Symbol | | | 74ACT T _A = +25°C C _L = 50 pF | | | 54/ | ACT | 74ACT | | and d | |
|------------------|--|-----------------------|--|-----|-----|---|------|--|------|-------|-------------|
| | Parameter | V _{CC} * (V) | | | | $T_A = -55^{\circ}C$ to $+125^{\circ}C$ $C_L = 50 pF$ | | $T_A = -40^{\circ}C$ to $+85^{\circ}C$ $C_L = 50 \text{ pF}$ | | Units | Fig. No. |
| | | | Min | Тур | Max | Min | Max | Min | Max | 2310 | |
| t _{PLH} | Propagation Delay S to \overline{Z}_n | 5.0 | 2.5 | 6.0 | 9.5 | 1.0 | 12.0 | 2.0 | 11.0 | ns | 2-6 |
| t _{PHL} | Propagation Delay S to \overline{Z}_n | 5.0 | 1.5 | 5.5 | 9.0 | 1.0 | 11.5 | 1.5 | 10.0 | ns | 2-6 |
| t _{PLH} | Propagation Delay \overline{E} to \overline{Z}_n | 5.0 | 1.5 | 5.5 | 9.5 | 1.0 | 11.0 | 1.5 | 10.5 | ns | 2-6 |
| t _{PHL} | Propagation Delay \overline{E} to \overline{Z}_n | 5.0 | 1.5 | 5.5 | 9.5 | 1.0 | 11.0 | 1.5 | 10.5 | ns | 2-6 |
| t _{PLH} | Propagation Delay I_n to \overline{Z}_n | 5.0 | 1.5 | 4.5 | 8.0 | 1.0 | 9.5 | 1.0 | 8.5 | ns | 2-6 |
| t _{PHL} | Propagation Delay I_n to \overline{Z}_n | 5.0 | 1.5 | 4.0 | 6.5 | 1.0 | 8.0 | 1.0 | 7.5 | ns | 2-6 |

^{*}Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

| Symbol | Parameter | AC/ACT | Units | Conditions | |
|-----------------|----------------------------------|--------|-------|-----------------|--|
| | T di dilliotoi | Тур | | | |
| C _{IN} | Input Capacitance | 4.5 | pF | $V_{CC} = 5.0V$ | |
| C _{PD} | Power Dissipation Capacitance | 45.0 | pF | $V_{CC} = 5.0V$ | |



54AC/74AC161 • 54ACT/74ACT161 **Synchronous Presettable Binary Counter**

General Description

The 'AC/'ACT161 are high-speed synchronous modulo-16 binary counters. They are synchronously presettable for application in programmable dividers and have two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multistage counters. The 'AC/ 'ACT161 has an asynchronous Master Reset input that overrides all other inputs and forces the outputs LOW.

Features

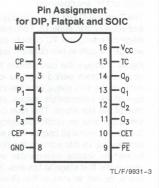
- Synchronous counting and loading
- High-speed synchronous expansion
- Typical count rate of 125 MHz
- Outputs source/sink 24 mA
- 'ACT161 has TTL-compatible inputs

Ordering Code: See Section 5

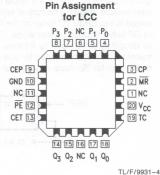
Logic Symbols

IEEE/IEC CTRDIV16 CT=0 M1 CET M2 3CT=15 CFT G3 CFP G4 > C5/2, 3, 4+ TL/F/9931-1 1,5D (1) Qo (2) Q1 (4) Q_2 (8) TL/F/9931-2

Connection Diagrams



| Pin Names | Description | | | | | |
|-------------|---------------------------------|--|--|--|--|--|
| CEP | Count Enable Parallel Input | | | | | |
| CET | Count Enable Trickle Input | | | | | |
| CP | Clock Pulse Input | | | | | |
| MR | Asynchronous Master Reset Input | | | | | |
| $P_0 - P_3$ | Parallel Data Inputs | | | | | |
| PE | Parallel Enable Inputs | | | | | |
| $Q_0 - Q_3$ | Flip-Flop Outputs | | | | | |
| TC | Terminal Count Output | | | | | |



Functional Description

The 'AC/'ACT161 count in modulo-16 binary sequence. From state 15 (HHHH) they increment to state 0 (LLLL). The clock inputs of all flip-flops are driven in parallel through a clock buffer. Thus all changes of the Q outputs (except due to Master Reset of the '161) occur as a result of, and synchronous with, the LOW-to-HIGH transition of the CP input signal. The circuits have four fundamental modes of operation, in order of precedence: asynchronous reset, parallel load, count-up and hold. Five control inputs-Master Reset, Parallel Enable (PE), Count Enable Parallel (CEP) and Count Enable Trickle (CET)—determine the mode of operation, as shown in the Mode Select Table. A LOW signal on MR overrides all other inputs and asynchronously forces all outputs LOW. A LOW signal on PE overrides counting and allows information on the Parallel Data (Pn) inputs to be loaded into the flip-flops on the next rising edge of CP. With PE and MR HIGH, CEP and CET permit counting when both are HIGH. Conversely, a LOW signal on either CEP or CET inhibits counting.

The 'AC/'ACT161 use D-type edge-triggered flip-flops and changing the PE, CEP and CET inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed.

The Terminal Count (TC) output is HIGH when CET is HIGH and counter is in state 15. To implement synchronous multistage counters, the TC outputs can be used with the CEP and CET inputs in two different ways.

Figure 1 shows the connections for simple ripple carry, in which the clock period must be longer than the CP to TC delay of the first stage, plus the cumulative CET to TC delays of the intermediate stages, plus the CET to CP setup time of the last stage. This total delay plus setup time sets the upper limit on clock frequency. For faster clock rates, the carry lookahead connections shown in Figure 2 are recommended. In this scheme the ripple delay through the intermediate stages commences with the same clock that causes the first stage to tick over from max to min in the Up mode, or min to max in the Down mode, to start its final cycle. Since this final cycle requires 16 clocks to complete, there is plenty of time for the ripple to progress through the intermediate stages. The critical timing that limits the clock period is the CP to TC delay of the first stage plus the CEP to CP setup time of the last stage. The TC output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, registers or counters.

For such applications, the Clocked Carry ($\overline{\text{CC}}$) output is provided. The $\overline{\text{CC}}$ output is normally HIGH. When $\overline{\text{CEP}}$, $\overline{\text{CET}}$, and $\overline{\text{TC}}$ are LOW, the $\overline{\text{CC}}$ output will go LOW when the clock next goes LOW and will stay LOW until the clock goes HIGH again, as shown in the $\overline{\text{CC}}$ Truth Table. When the Output Enable ($\overline{\text{OE}}$) is LOW, the parallel data outputs O_0-O_3 are active and follow the flip-flop Q outputs. A HIGH signal on $\overline{\text{OE}}$ forces O_0-O_3 to the High Z state but does not prevent counting, loading or resetting.

Logic Equations: Count Enable = CEP • CET • $\overline{\text{PE}}$ $TC = Q_0 • Q_1 • Q_2 • Q_3 • CET$

Mode Select Table

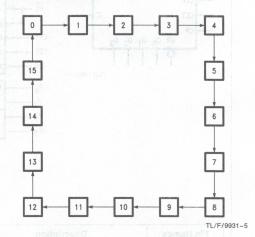
| | PE | CET | CEP | Action on the Rising Clock Edge () |
|---|----|-------|------|---------------------------------------|
| | X | X | X to | Reset (Clear) |
| - | L | X | X | Load $(P_n \rightarrow Q_n)$ |
| | Н | Н | Н | Count (Increment) |
| | Н | Facqu | X | No Change (Hold) |
| 1 | Н | X | L | No Change (Hold) |

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

State Diagram



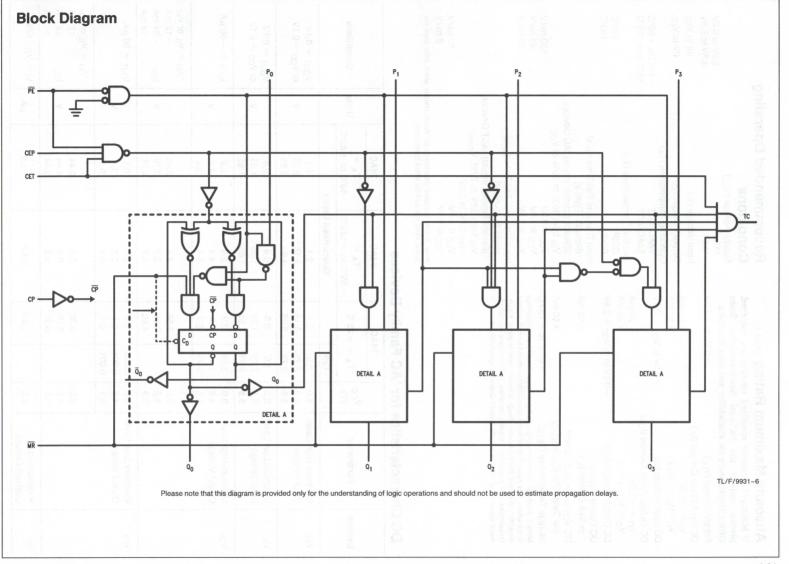
COUNT CET TC CET

FIGURE 1. Multistage Counter with Ripple Carry

COUNT CET TC CEP CEP CET TC CE

FIGURE 2. Multistage Counter with Lookahead Carry

TL/F/9931-9



Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Supply Voltage (V _{CC}) | -0.5V to $+7.0V$ |
|---|----------------------------------|
| DC Input Diode Current (I _{IK}) | |
| $V_{I} = -0.5V$ | -20 mA |
| $V_I = V_{CC} + 0.5V$ | + 20 mA |
| DC Input Voltage (V _I) | -0.5 V to $V_{CC} + 0.5$ V |
| DC Output Diode Current (IOK) | |
| $V_0 = -0.5V$ | -20 mA |
| $V_O = V_{CC} + 0.5V$ | + 20 mA |
| DC Output Voltage (V _O) | -0.5 V to to $V_{CC} + 0.5$ V |
| DC Output Source | |
| or Sink Current (IO) | ±50 mA |
| DC V _{CC} or Ground Current | |
| per Output Pin (I _{CC} or I _{GND}) | ±50 mA |
| Storage Temperature (T _{STG}) | -65°C to +150°C |
| Note 1: Absolute maximum ratings are t | those values beyond which damage |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

| Supply Voltage (V _{CC}) | |
|--|-----------------------------------|
| 'AC | 2.0V to 6.0V |
| 'ACT | 4.5V to 5.5V |
| Input Voltage (V _I) | 0V to V _{CC} |
| Output Voltage (VO) | 0V to V _{CC} |
| Operating Temperature (T _A) 74AC/ACT 54AC/ACT | -40°C to +85°C -55°C to +125°C |
| Junction Temperature (T _J) CDIP PDIP | 175°C 140°C |
| Input Rise and Fall Time (t _r , t _f) (Note 2) (Typical) (Except Schmitt Inputs) 'AC Devices V _{IN} from 30% to 70% of V _{CC} V _{CC} @ 3.0V V _{CC} @ 4.5V V _{CC} @ 5.5V | 150 ns/V 40 ns/V 25 ns/V |
| Input Rise and Fall Time (t _r , t _f) (Note 2) (Typical) (Except Schmitt Inputs) 'ACT Devices V _{IN} from 0.8V to 2.0V, V _{meas} from 0.8V to 2.0V | |
| V _{CC} @ 4.5V | 10 ns/V |
| V _{CC} @ 5.5V | 8 ns/V |
| Note 2: See individual datasheets for those device | es which differ from the |

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

| Symbol | | 74AC | | AC | 54AC | 74AC | | Conditions | |
|-----------------|--|---------------------|-------------------------|----------------------|-----------------------------------|---------------------------------|-------|--|--|
| | Parameter | V _{CC} (V) | T _A = +25°C | | T _A = -55°C to + 125°C | T _A = -40°C to +85°C | Units | | |
| | | a sylvenia a | Тур | ruscu. | Guaranteed Lir | mits | | | |
| V _{IH} | Minimum High Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{IL} | Maximum Low Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{OH} | Minimum High Level Output Voltage | 3.0 4.5 5.5 | 2.99 4.49 5.49 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | V | $I_{OUT} = -50 \mu\text{A}$ | |
| | 00 00 00 00 00 00 00 00 00 00 00 00 00 | 3.0 4.5 5.5 | | 2.56 3.86 4.86 | 2.4 3.7 4.7 | 2.46 3.76 4.76 | ٧ | $\begin{tabular}{ll} *V_{\text{IN}} &= V_{\text{IL}} \text{ or } V_{\text{IH}} \\ &- 12 \text{ mA} \\ &- 24 \text{ mA} \\ &- 24 \text{ mA} \\ \end{tabular}$ | |
| V _{OL} | Maximum Low Level Output Voltage | 3.0 4.5 5.5 | 0.002 0.001 0.001 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | V | Ι _{ΟUT} = 50 μΑ | |
| | | 3.0 4.5 5.5 | | 0.36 0.36 0.36 | 0.5 0.5 0.5 | 0.44 0.44 0.44 | V | $\begin{tabular}{ll} *V_{IN} &= V_{IL} \mbox{ or } V_{IH} \\ &= 12 \mbox{ mA} \\ I_{OL} &= 24 \mbox{ mA} \\ &= 24 \mbox{ mA} \\ \end{tabular}$ | |
| I _{IN} | Maximum Input Leakage Current | 5.5 | | ±0.1 | ± 1.0 | ± 1.0 | μА | $V_I = V_{CC}$, GND | |

| Symbol | 7450 | | 74AC T _A = +25°C | | 54AC | 74AC | Units | Conditions | |
|--------|-------------------------------------|---------------------|--------------------------------|---------|----------------------------------|---------------------------------|-------|------------------------------|--|
| | Parameter | V _{CC} (V) | | | T _A = -55°C to +125°C | T _A = -40°C to +85°C | | | |
| | To 08 = 30 | 19 | Тур | -13-0-1 | Guaranteed Li | mits | | | |
| IOLD | †Minimum Dynamic | 5.5 | \$151 | 1 K.15 | 50 | 75 | mA | V _{OLD} = 1.65V Max | |
| IOHD | Output Current | 5.5 | 0.0 | | -50 | 75 | mA | V _{OHD} = 3.85V Min | |
| Icc | Maximum Quiescent Supply Current | 5.5 | 0. | 4.0 | 80.0 | 40.0 | μА | $V_{IN} = V_{CC}$ or GND | |

^{*}All outputs loaded; thresholds on input associated with output under test.

DC Characteristics for 'ACT Family Devices

| | W.11 V.2 | 74ACT | | СТ | 54ACT | 74ACT | | 70.000 | |
|------------------|--------------------------------------|------------------------|------------------|--------------|-----------------------------------|---------------------------------|-------------|---|--|
| Symbol | Parameter | V _{CC} (V) | T _A = | + 25°C | T _A = -55°C to + 125°C | T _A = -40°C to +85°C | Units | Conditions | |
| 8-S a | 1 6 9.5 | 0.71 | Тур | | Guaranteed L | imits | A STREET AT | OT of IEO | |
| V _{IH} | Minimum High Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 2.0 | 2.0 0.5 | 2.0 2.0 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| VIL | Maximum Low Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 0.8 | 0.8 | 0.8 0.8 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{OH} | Minimum High Level Output Voltage | 4.5 5.5 | 4.49 5.49 | 4.4 5.4 | 4.4 5.4 | 4.4 5.4 | ٧ | $I_{OUT} = -50 \mu\text{A}$ | |
| | | 4.5 5.5 | | 3.86 4.86 | 3.70 4.70 | 3.76 4.76 | ٧ | $\begin{tabular}{ll} *V_{IN} &= V_{IL} \mbox{ or } V_{IH} \\ &-24 \mbox{ mA} \\ &-24 \mbox{ mA} \end{tabular}$ | |
| V _{OL} | Maximum Low Level Output Voltage | 4.5 5.5 | 0.001 0.001 | 0.1 0.1 | 0.1 0.1 | 0.1 0.1 | ٧ | I _{OUT} = 50 μA | |
| | | 4.5 5.5 | | 0.36 0.36 | 0.50 0.50 | 0.44 0.44 | ٧ | $\begin{tabular}{ll} *V_{IN} = V_{IL} \mbox{ or } V_{IH} \\ I_{OL} & 24 \mbox{ mA} \\ 24 \mbox{ mA} \\ \end{tabular}$ | |
| I _{IN} | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | ±1.0 | μА | $V_{I} = V_{CC}$, GND | |
| Ісст | Maximum I _{CC} /Input | 5.5 | 0.6 | | 1.6 | 1.5 | mA | $V_{\rm I} = V_{\rm CC} - 2.1V$ | |
| I _{OLD} | †Minimum Dynamic | 5.5 | | | 50 | 75 | mA | V _{OLD} = 1.65V Max | |
| IOHD | Output Current | 5.5 | | | -50 | -75 | mA | V _{OHD} = 3.85V Min | |
| Icc | Maximum Quiescent Supply Current | 5.5 | | 4.0 | 80.0 | 40.0 | μΑ | V _{IN} = V _{CC} or GND | |

^{*}All outputs loaded; thresholds on input associated with output under test.

[†]Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC} . I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

 $[\]dagger \text{Maximum}$ test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics Applied Vime 7 OA not solve to see a solve of Vime 7 OA not solve of

| | 5.4 | | | 74AC | | 54 | AC | 74 | AC | | |
|------------------|--|--------------------------|------------|------------|------------|---|--------------|--|--------------|-------|-------------|
| Symbol | Parameter | V _{CC} * (V) | | | | $T_A = -55^{\circ}C$ to $+125^{\circ}C$ $C_L = 50 \text{ pF}$ | | T _A = -40°C to +85°C C _L = 50 pF | | Units | Fig. No. |
| | | \$ B | Min | Тур | Max | Min | Max | Min | Max | | |
| f _{max} | Maximum Count Frequency | 3.3 5.0 | 70 110 | 111 167 | | 55 80 | i e a | 60 95 | por Cures | MHz | 2-3 |
| t _{PLH} | Propagation Delay CP to Q _n (PE Input HIGH or LOW) | 3.3 5.0 | 2.0 1.5 | 7.0 5.0 | 12 9.0 | 1.0 1.0 | 15.0 11.0 | 1.5 1.0 | 13.5 9.5 | ns | 2-6 |
| t _{PHL} | Propagation Delay CP to Q _n (PE Input HIGH or LOW) | 3.3 5.0 | 1.5 1.5 | 7.0 5.0 | 12 9.5 | 1.0 1.0 | 15.0 11.0 | 1.5 1.5 | 13 10 | ns | 2-6 |
| t _{PLH} | Propagation Delay CP to TC | 3.3 5.0 | 3.0 2.0 | 9 | 15 10.5 | 1.0 1.0 | 18.5 13.0 | 2.5 1.5 | 16.5 11.5 | ns | 2-6 |
| t _{PHL} | Propagation Delay CP to TC | 3.3 5.0 | 3.5 2.0 | 8.5 6.5 | 14 11 | 1.0 1.0 | 17.5 13.0 | 2.5 | 15.5 11.5 | ns | 2-6 |
| t _{PLH} | Propagation Delay CET to TC | 3.3 5.0 | 2.0 1.5 | 5.5 3.5 | 9.5 6.5 | 1.0 1.0 | 13.0 8.5 | 1.5 1.0 | 11 7.5 | ns | 2-6 |
| t _{PHL} | Propagation Delay CET to TC | 3.3 5.0 | 2.5 | 6.5 5 | 11 8.5 | 1.0 1.0 | 14.5 11.0 | 2.0 1.5 | 12.5 9.5 | ns | 2-6 |
| t _{PLH} | Propagation Delay MR to Qn | 3.3 5.0 | 2.0 1.5 | 6.5 5.5 | 12 9.5 | 1.0 1.0 | 14.5 10.5 | 1.5 1.5 | 13.5 10 | ns | 2-6 |
| t _{PHL} | Propagation Delay MR to TC | 3.3 5.0 | 3.5 2.5 | 10 8.5 | 15 13 | 1.0 | 18.5 14.0 | 3.0 2.5 | 17.5 13.5 | ns | 2-6 |

*Voltage Range 3.3 is 3.3V ± 0.3 V Voltage Range 5.0 is 5.0V ± 0.5 V

AC Operating Requirements

| Symbol | T PARCY | TARE | CC* T _A = +25°C | | 54AC | 74AC | Units | Fig. |
|------------------|---|-----------------------|----------------------------|-------------|---|--|-------|------|
| | Parameter | V _{CC} * (V) | | | $T_A = -55^{\circ}C$ to $+125^{\circ}C$ $C_L = 50 pF$ | $T_A = -40^{\circ}C$ to $+85^{\circ}C$ $C_L = 50 pF$ | | |
| | asseminist he | atria sgui | Тур | auT | Guaranteed Min | imum | | |
| t _s | Setup Time, HIGH or LOW | 3.3 5.0 | 6.0 3.5 | 13.5 8.5 | 16.0 10.5 | 16 10.5 | ns | 2-9 |
| t _h | Hold Time, HIGH or LOW | 3.3 5.0 | -7.0 -4.0 | -1 0 | 0.5 1.5 | -0.5 0 | ns | 2-9 |
| t _s | Setup Time, HIGH or LOW PE to CP | 3.3 5.0 | 6.5 4.0 | 11.5 7.5 | 15.0 10.5 | 14 8.5 | ns | 2-9 |
| t _h | Hold Time, HIGH or LOW | 3.3 5.0 | -6.0 -3.5 | 0 0.5 | -1.0 0.0 | J 10 HO 0 Leaff to L | ns | 2-9 |
| ts | Setup Time, HIGH or LOW CEP or CET to CP | 3.3 5.0 | 3.0 2.0 | 6.0 4.5 | 7.5 5.5 | 7 5 | ns | 2-9 |
| t _h | Hold Time, HIGH or LOW CEP or CET to CP | 3.3 5.0 | -3.5 -2 | 0 | 2.0 2.0 | 0 0.5 | ns | 2-9 |
| t _w | Clock Pulse Width (Load) HIGH or LOW | 3.3 5.0 | 2.0 2.0 | 3.5 2.5 | 5.0 5.0 | 4 3 | ns | 2-6 |
| t _w | Clock Pulse Width (Count) HIGH or LOW | 3.3 5.0 | 2.0 | 4.0 3.0 | 5.0 5.0 | 4.5 3.5 | ns | 2-6 |
| t _w | MR Pulse Width, LOW | 3.3 5.0 | 3.0 2.5 | 5.5 4.5 | 5.0 5.0 | 7.5 6.0 | ns | 2-6 |
| t _{rec} | Recovery Time MR to CP | | -2 -1 | -0.5 0 | 1.5 2.0 | 0 0.5 | ns | 2-9 |

^{*}Voltage Range 3.3 is 3.3V ±0.3V Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics

| | 1500 | 74ACT T _A = +25°C C _L = 50 pF | | | 54/ | ACT | 74ACT | | ght/8 | |
|---|--|---|------|--|---|--|---|---|--|---|
| | V _{CC} * | | | | $T_A = -55^{\circ}C$ $to + 125^{\circ}C$ $C_L = 50 pF$ | | $T_A = -40^{\circ}C$ $to +85^{\circ}C$ $C_L = 50 pF$ | | Units | Fig. No. |
| | | Min | Тур | Max | Min | Max | Min | Max | | |
| Maximum Count Frequency | 5.0 | 115 | 125 | | | | 100 | | MHz | 2-3 |
| Propagation Delay CP to Q _n (PE Input HIGH or LOW) | 5.0 | 1.5 | 8.0 | 10.0 | | | 1.5 | 13.5 | ns | 2-6 |
| Propagation Delay CP to Q _n (PE Input HIGH or LOW) | 5.0 | 1.5 | 8.0 | 10.0 | | | 1.5 | 12.5 | ns | 2-6 |
| Propagation Delay CP to TC | 5.0 | 2.0 | 11.0 | 13.5 | | | 1.5 | 16.5 | ns | 2-6 |
| Propagation Delay CP to TC | 5.0 | 1.5 | 11.0 | 13.0 | | | 1.5 | 15.5 | ns | 2-6 |
| Propagation Delay CET to TC | 5.0 | 1.5 | 7.5 | 9.0 | | | 1.5 | 11.5 | ns | 2-6 |
| Propagation Delay CET to TC | 5.0 | 1.5 | 8.0 | 10.0 | | | 1.5 | 13.0 | ns | 2-6 |
| Propagation Delay MR to Qn | 5.0 | 1.5 | 8.0 | 9.5 | | | 1.5 | 12.0 | ns | 2-6 |
| Propagation Delay MR to TC | 5.0 | 2.5 | 10.0 | 11.5 | | | 2.0 | 14.5 | ns | 2-6 |
| | Parameter Maximum Count Frequency Propagation Delay CP to Qn (PE Input HIGH or LOW) Propagation Delay CP to Qn (PE Input HIGH or LOW) Propagation Delay CP to TC Propagation Delay CP to TC Propagation Delay CET to TC Propagation Delay RETOR | Parameter VCC* (V) Maximum Count Frequency 5.0 Propagation Delay CP to Qn (PE Input HIGH or LOW) 5.0 Propagation Delay CP to Qn (PE Input HIGH or LOW) 5.0 Propagation Delay CP to TC Propagation Delay CP to TC Propagation Delay 5.0 Propagation Delay 5.0 | Name | Parameter V _{CC} * (V) T _A = +25° C _L = 50 pl Maximum Count Frequency 5.0 I15 I25 Propagation Delay CP to Qn (PE Input HIGH or LOW) 5.0 I.5 8.0 Propagation Delay CP to Qn (PE Input HIGH or LOW) 5.0 I.5 8.0 Propagation Delay CP to TC 5.0 I.5 I1.0 Propagation Delay CP to TC 5.0 I.5 I1.0 Propagation Delay CET to TC 5.0 I.5 8.0 Propagation Delay CET to TC Propagation Delay MR to Qn 5.0 I.5 8.0 Propagation Delay MR to Qn Propagation Delay < | Parameter VCC* (V) TA = +25°C CL = 50 pF Max Maximum Count Frequency 5.0 115 125 Propagation Delay CP to Qn (PE Input HIGH or LOW) 5.0 1.5 8.0 10.0 Propagation Delay CP to TC 5.0 2.0 11.0 13.5 Propagation Delay CET to TC 5.0 1.5 7.5 9.0 Propagation Delay CET to TC 5.0 1.5 8.0 10.0 Propagation Delay MR to Qn 5.0 1.5 8.0 9.5 Propagation Delay MR to Qn 5.0 1.5 8.0 9.5 | Parameter TA = +25°C CL = 50 pF TA = +25°C CL = 50 pF TA = to + to | Parameter V _{CC} * (V) T _A = −55°C to +125°C cL = 50 pF T _A = −55°C to +125°C cL = 50 pF Min Typ Max Min Max Max Min Max < | Parameter V _{CC} * (V) T _A = −55°C to +125°C to +125°C to +125°C to +125°C c _L = 50 pF T _A = −55°C to +125°C to +125°C c _L = 50 pF T _A = −55°C to +125°C c _L = 50 pF T _A = −55°C to +125°C c _L = 50 pF T _A = −55°C to +125°C c _L = 50 pF T _L = 50 pF | $ \begin{array}{c ccccccccccccccccccccccccccccccccccc$ | Parameter VCC* (V) T _A = +25°C CL = 50 pF T _A = −55°C to +85°C to +85°C CL = 50 pF Units Maximum Count Frequency 5.0 115 125 100 MHz Propagation Delay CP to Qn (PE Input HIGH or LOW) 5.0 1.5 8.0 10.0 1.5 13.5 ns Propagation Delay CP to Qn (PE Input HIGH or LOW) 5.0 1.5 8.0 10.0 1.5 12.5 ns Propagation Delay CP to TC 5.0 1.5 11.5 15.5 15.5 ns Propagation Delay CET to TC 5.0 1.5 8.0 10.0 1.5 11.5 11.5 11.5 11.5 11.5 11.5 11.5 11.5 11.5 11.5 11.5 <t< td=""></t<> |

^{*}Voltage Range 5.0 is 5.0V $\pm 0.5 \text{V}$

AC Operating Requirements

| | CAST | IAO A | 74A | СТ | 54ACT | 74ACT | | |
|------------------|--|-----------------------|------|------|---|--|-------|------|
| Symbol | Parameter | V _{CC} * (V) | | | $T_A = -55^{\circ}C$ to $+125^{\circ}C$ $C_L = 50 pF$ | $T_A = -40^{\circ}C$ $to +85^{\circ}C$ $C_L = 50 pF$ | Units | Fig. |
| | morning by | eknerenk. | Тур | CD-7 | Guaranteed Min | imum | | |
| ts | Setup Time, HIGH or LOW Pn to CP | 5.0 | 7.0 | 8.5 | 8.8 1 W.). 6.0 | 11.5 | ns | 2-9 |
| th | Hold Time, HIGH or LOW P _n to CP | 5.0 | -3.0 | -1 | 0.8 WC | 0.5 90 6 | ns | 2-9 |
| ts | Setup Time, HIGH or LOW PE to CP | 5.0 | 6.0 | 7.5 | 8.5-1 We. | 10.5 | ns | 2-9 |
| th | Hold Time, HIGH or LOW PE to CP | 5.0 | -3.5 | 0 | 5.0 J | 0.5 | ns | 2-9 |
| ts | Setup Time, HIGH or LOW CEP or CET to CP | 5.0 | 4.0 | 5.5 | 8.8 WC. | 9.5 | ns | 2-9 |
| th | Hold Time, HIGH or LOW CEP or CET to CP | 5.0 | -2.0 | 0 | 0.8 | 0.5 | ns | 2-9 |
| t _w | Clock Pulse Width (Load) HIGH or LOW | 5.0 | 2.0 | 4.5 | 0.00 | 6.5 | ns | 2-6 |
| t _w | Clock Pulse Width (Count) HIGH or LOW | 5.0 | 2.0 | 4.5 | 8.8 | 7500W 90M908 | ns | 2-6 |
| t _w | MR Pulse Width, LOW | 5.0 | 3.0 | 4.5 | Section 1 | 6.5 | ns | 2-6 |
| t _{rec} | Recovery Time MR to CP | 5.0 | 0 | 0 | | 0.5 | ns | 2-9 |

^{*}Voltage Range 5.0 is 5.0V ± 0.5 V

Capacitance

| Symbol C _{IN} C _{PD} | Parameter | AC/ACT | Units | Conditions | | |
|--|----------------------------------|--------|--------|-----------------|--|--|
| | raiameter 3,555 | Тур | Oilles | Conditions | | |
| C _{IN} | Input Capacitance | 4.5 | pF | $V_{CC} = 5.0V$ | | |
| C _{PD} | Power Dissipation Capacitance | 45.0 | pF | $V_{CC} = 5.0V$ | | |



54AC/74AC163 • 54ACT/74ACT163 Synchronous Presettable Binary Counter

General Description

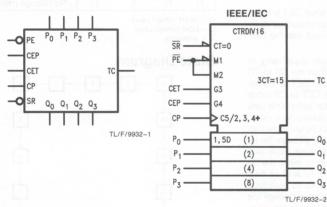
The 'AC/'ACT163 are high-speed synchronous modulo-16 binary counters. They are synchronously presettable for application in programmable dividers and have two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multistage counters. The 'AC/' ACT163 has a Synchronous Reset input that overrides counting and parallel loading and allows the outputs to be simultaneously reset on the rising edge of the clock.

Features

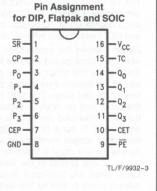
- Synchronous counting and loading
- High-speed synchronous expansion
- Typical count rate of 125 MHz
- Outputs source/sink 24 mA
- 'ACT163 has TTL-compatible inputs

Ordering Code: See Section 5

Logic Symbols



Connection Diagrams



| Pin Names | Description | | | | | | |
|--------------------------------|-----------------------------|--|--|--|--|--|--|
| CEP | Count Enable Parallel Input | | | | | | |
| CET | Count Enable Trickle Input | | | | | | |
| CP | Clock Pulse Input | | | | | | |
| SR | Synchronous Reset Input | | | | | | |
| P ₀ -P ₃ | Parallel Data Inputs | | | | | | |
| PE | Parallel Enable Input | | | | | | |
| $Q_0 - Q_3$ | Flip-Flop Outputs | | | | | | |
| TC | Terminal Count Output | | | | | | |

| Pin Assignment for LCC | ar bohet |
|--|---|
| P ₃ P ₂ NC P ₁ P ₀ 8 7 6 5 4 | |
| CEP 9 GND 10 NC 11 PE 12 CET 13 | 3 CP 2 SR 1 NC 20 V _{CC} 19 TC |
| 14 15 16 17 18 Q ₃ Q ₂ NC Q ₁ Q ₀ | ·/ |
| | TL/F/9932-4 |

Functional Description

The 'AC/'ACT163 counts in modulo-16 binary sequence. From state 15 (HHHH) it increments to state 0 (LLLL). The clock inputs of all flip-flops are driven in parallel through a clock buffer. Thus all changes of the Q outputs occur as a result of, and synchronous with, the LOW-to-HIGH transition of the CP input signal. The circuits have four fundamental modes of operation, in order of precedence: synchronous reset, parallel load, count-up and hold. Four control inputs-Synchronous Reset (SR), Parallel Enable (PE), Count Enable Parallel (CEP) and Count Enable Trickle (CET)-determine the mode of operation, as shown in the Mode Select Table. A LOW signal on SR overrides counting and parallel loading and allows all outputs to go LOW on the next rising edge of CP. A LOW signal on PE overrides counting and allows information on the Parallel Data (Pn) inputs to be loaded into the flip-flops on the next rising edge of CP. With PE and SR HIGH, CEP and CET permit counting when both are HIGH. Conversely, a LOW signal on either CEP or CET inhibits counting.

The 'AC/'ACT163 uses D-type edge-triggered flip-flops and changing the SR, PE, CEP and CET inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed.

The Terminal Count (TC) output is HIGH when CET is HIGH and counter is in state 15. To implement synchronous multistage counters, the TC outputs can be used with the CEP and CET inputs in two different ways.

Figure 1 shows the connections for simple ripple carry, in which the clock period must be longer than the CP to TC delay of the first stage, plus the cumulative CET to TC delays of the intermediate stages, plus the CET to CP setup time of the last stage. This total delay plus setup time sets the upper limit on clock frequency. For faster clock rates, the carry lookahead connections shown in Figure 2 are recommended. In this scheme the ripple delay through the intermediate stages commences with the same clock that causes the first stage to tick over from max to min in the Up mode, or min to max in the Down mode, to start its final cycle. Since this final cycle takes 16 clocks to complete, there is plenty of time for the ripple to progress through the intermediate stages. The critical timing that limits the clock period is the CP to TC delay of the first stage plus the CEP to CP setup time of the last stage. The TC output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, registers or counters. For such applications, the Clocked Carry (\overline{CC}) output is provided. The \overline{CC} output is normally HIGH. When \overline{CEP} , \overline{CET} , and \overline{TC} are LOW, the \overline{CC} output will go LOW when the clock next goes LOW and will stay LOW until the clock goes HIGH again, as shown in the \overline{CC} Truth Table. When the Output Enable (\overline{CE}) is LOW, the parallel data outputs O_0-O_3 are active and follow the flip-flop Q outputs. A HIGH signal on \overline{OE} forces O_0-O_3 to the High Z state but does not prevent counting, loading or resetting.

Logic Equations: Count Enable = CEP • CET • \overline{PE} $TC = Q_0 • Q_1 • Q_2 • Q_3 • CET$

Mode Select Table

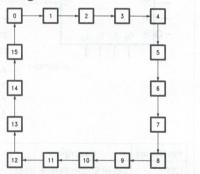
| SR | L X X H L X H H H | CET | CEP | Action on the Rising Clock Edge () |
|----|-------------------------|-----|-----|---------------------------------------|
| L | X | X | X | Reset (Clear) |
| Н | L | X | X | Load $(P_n \rightarrow Q_n)$ |
| Н | Н | Н | Н | Count (Increment) |
| Н | Н | L | X | No Change (Hold) |
| Н | Н | X | L | No Change (Hold) |

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

State Diagram



TL/F/9932-5

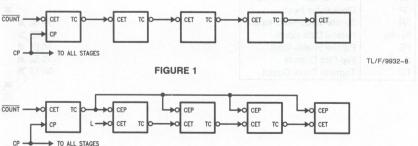
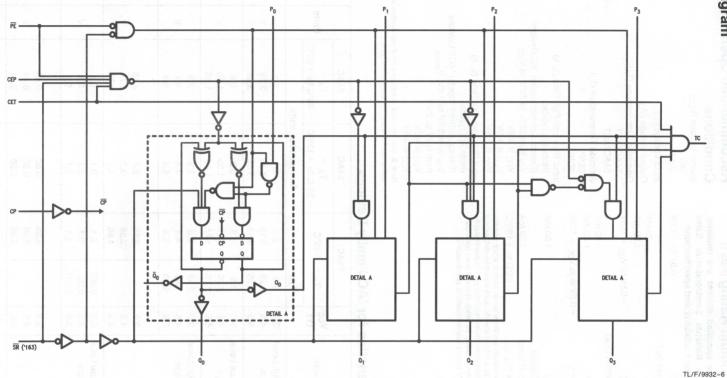


FIGURE 2



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications

| Office/Distributors for availab | ility and specifications. |
|---|-----------------------------------|
| Supply Voltage (V _{CC}) | -0.5V to $+7.0V$ |
| DC Input Diode Current (I _{IK}) | |
| $V_{I} = -0.5V$ | -20 mA |
| $V_I = V_{CC} + 0.5V$ | + 20 mA |
| DC Input Voltage (V _I) | -0.5 V to $V_{CC} + 0.5$ V |
| DC Output Diode Current (IOK) | |
| $V_0 = -0.5V$ | -20 mA |
| $V_O = V_{CC} + 0.5V$ | + 20 mA |
| DC Output Voltage (V _O) | -0.5 V to to V_{CC} + 0.5 V |
| DC Output Source | |
| or Sink Current (IO) | ±50 mA |
| DC V _{CC} or Ground Current | |
| per Output Pin (I _{CC} or I _{GND}) | ±50 mA |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Storage Temperature (TSTG)

Recommended Operating Conditions Supply Voltage (V_{CC})

| AO | 2.0 4 10 0.0 4 |
|--|-----------------------|
| 'ACT | 4.5V to 5.5V |
| Input Voltage (V _I) | 0V to V _{CC} |
| Output Voltage (V _O) | 0V to V _{CC} |
| Operating Temperature (T _A) | |
| 74AC/ACT | -40°C to +85°C |
| 54AC/ACT | -55°C to +125°C |
| Junction Temperature (T _J) | |
| CDIP | 175°C |
| PDIP | 140°C |
| Input Rise and Fall Time (t _r , t _f) (Note 2) (Typical) | |

2.0V to 6.0V

(Except Schmitt Inputs) 'AC Devices VIN from 30% to 70% of VCC

V_{CC} @ 3.0V 150 ns/V V_{CC} @ 4.5V 40 ns/V V_{CC} @ 5.5V 25 ns/V

Input Rise and Fall Time (tr, tf) (Note 2) (Typical)

(Except Schmitt Inputs) 'ACT Devices

VIN from 0.8V to 2.0V, V_{meas}

typical input rise and fall times noted here.

from 0.8V to 2.0V

V_{CC} @ 4.5V 10 ns/V V_{CC} @ 5.5V 8 ns/V Note 2: See individual datasheets for those devices which differ from the

DC Characteristics for 'AC Family Devices

-65°C to +150°C

| | | | $\begin{array}{c c} & 74AC \\ \hline V_{CC} & \\ (V) & T_A = +25^{\circ}C \end{array}$ | | 54AC | 74AC | | Conditions | |
|-----------------|--------------------------------------|-------------------|--|----------------------|----------------------------------|---------------------------------|-------|--|--|
| Symbol | Parameter | | | | T _A = -55°C to +125°C | T _A = -40°C to +85°C | Units | | |
| | | y 600 th | Тур | | Guaranteed Lir | nits | | | |
| V _{IH} | Minimum High Level Input Voltage | 3.0 4.5 5.5 | 4.5 2.25 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{IL} | Maximum Low Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | v | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{OH} | Minimum High Level Output Voltage | 3.0 4.5 5.5 | 2.99 4.49 5.49 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | V | $I_{OUT} = -50 \mu\text{A}$ | |
| | | 3.0 4.5 5.5 | er en de en de en e | 2.56 3.86 4.86 | 2.4 3.7 4.7 | 2,46 3,76 4,76 | ٧ | $\label{eq:VIN} \begin{split} *V_{IN} &= V_{IL} or V_{IH} \\ &- 12 mA \\ I_{OH} &- 24 mA \\ &- 24 mA \end{split}$ | |
| V _{OL} | Maximum Low Level Output Voltage | 3.0 4.5 5.5 | 0.002 0.001 0.001 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | ٧ | $I_{OUT} = 50 \mu A$ | |
| | | 3.0 4.5 5.5 | and the security of | 0.36 0.36 0.36 | 0.50 0.50 0.50 | 0.44 0.44 0.44 | V | $V_{IN} = V_{IL} \text{ or } V_{IH}$ 12 mA V_{IOL} 24 mA 24 mA | |
| I _{IN} | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | ±1.0 | μΑ | $V_{I} = V_{CC}$, GND | |

| Symbol | 7440 | | 74A | C | 54AC | 74AC | | | |
|------------------|-------------------------------------|---------------------|------------------------|-----|-----------------------------------|---------------------------------|-------|--|--|
| | Parameter | V _{CC} (V) | T _A = +25°C | | T _A = -55°C to + 125°C | T _A = -40°C to +85°C | Units | Conditions | |
| | Fe 06 = 13 | | Тур | | Guaranteed Lin | nits | | | |
| I _{OLD} | †Minimum Dynamic | 5.5 | M sile | xaM | 50 AND | 75 | mA | V _{OLD} = 1.65V Max | |
| IOHD | Output Current | 5.5 | aa | | -50 | E.E -75 | mA | V _{OHD} = 3.85V Min | |
| Icc | Maximum Quiescent Supply Current | 5.5 | 1 0.1 | 8.0 | 160.0 | 80.0 0.00 | μА | V _{IN} = V _{CC} or GND | |

^{*}All outputs loaded; thresholds on input associated with output under test.

DC Characteristics for 'ACT Family Devices

| | Parameter | 0.11 | 74ACT VCC (V) TA = +25°C | | 54ACT | 74ACT | (Section) | Conditions | |
|------------------|--|------------------------|-----------------------------|---------------------|-------------------------------------|---------------------------------|-------------|---|--|
| Symbol | | V _{CC} (V) | | | T _A = -55°C to + 125°C | T _A = -40°C to +85°C | Units | | |
| | 88: 08 | 0.51 | Тур | p Guaranteed Limits | | | | otanagon9 sud | |
| V _{IH} | Minimum High Level Input Voltage | 4.5 5.5 | 1.5 | 2.0 2.0 | 2.0 | 2.0 2.0 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{IL} | Maximum Low Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 0.8 0.8 | 0.8 0.8 | 0.8 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{OH} | Minimum High Level Output Voltage | 4.5 5.5 | 4.49 5.49 | 4.4 5.4 | 4.4 5.4 | 4.4 5.4 | ٧ | $I_{OUT} = -50 \mu\text{A}$ | |
| | 0.64 = A) 0.65 = 0 0. | 4.5 5.5 | 198 1983 - 1 1988 - 1 | 3.86 4.86 | 0.783 + = A.7 40 00 3.70 4.70 | 3.76 4.76 | ٧ | $\begin{tabular}{ll} *V_{\text{IN}} &= V_{\text{IL}} \text{ or } V_{\text{IH}} \\ &-24 \text{ mA} \\ &-24 \text{ mA} \end{tabular}$ | |
| V _{OL} | Maximum Low Level Output Voltage | 4.5 5.5 | 0.001 0.001 | 0.1 0.1 | 0.1 ³ 0.1 3.3 | 0.1 0.1 | V | $I_{OUT} = 50 \mu\text{A}$ | |
| | 0.5. -0.5 -0.5 -0.5 | 4.5 5.5 | 8:0- | 0.36 0.36 | 0.50 0.50 | 0.44 0.44 | V | ${*V_{\text{IN}} = V_{\text{IL}} \text{ or } V_{\text{IH}}} $ ${}^{\text{24 mA}} $ ${}^{\text{10L}} $ ${}^{\text{24 mA}} $ | |
| IIN | Maximum Input Leakage Current | 5.5 | 9.51 0.81 | ±0.1 | 1.0 ± 1.0 ± | ± 1.0 | μА | $V_{I} = V_{CC}$, GND | |
| ICCT | Maximum I _{CC} /Input | 5.5 | 0.6 | | 1.6.3 | 8.8 WOJ 10 | mA | $V_I = V_{CC} - 2.1V$ | |
| lold | †Minimum Dynamic | 5.5 | 16.0 | | 5.5 00 | 75 75 | mA | V _{OLD} = 1.65V Max | |
| I _{OHD} | Output Current | 5.5 | 0.8 | | -50 | -75 | mA | V _{OHD} = 3.85V Min | |
| Icc | Maximum Quiescent Supply Current | 5.5 | 6 | 8.0 | 160.0 | 80.0 | μΑ | V _{IN} = V _{CC} or GND | |

^{*}All outputs loaded; thresholds on input associated with output under test.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

[†]Maximum test duration 2.0 ms, one output loaded at a time.

Note: $I_{\rm IN}$ and $I_{\rm CC}$ @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}. $I_{\rm CC}$ for 54AC @ 25°C is identical to 74AC @ 25°C.

[†]Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics and applied with a CA in the applied as a second second

| Symbol | 2/48 | 4 | | 74AC | | 54 | AC | 74 | 4AC | | |
|------------------|---|--------------------------|--|-------------|--------------|---|--------------|--|--------------|-------|-------|
| | Parameter | V _{CC} * (V) | T _A = +25°C C _L = 50 pF | | | $T_A = -55^{\circ}C$ to $+125^{\circ}C$ $C_L = 50 pF$ | | $T_A = -40^{\circ}C$ $to +85^{\circ}C$ $C_L = 50 pF$ | | Units | Fig. |
| zaki Vaa | Fe may Am 37 | | Min | Тур | Max | Min | Max | Min | Max | Mil | 77.79 |
| f _{max} | Maximum Clock Frequency | 3.3 5.0 | 70 110 | 95 140 | | 55 90 | 8,0 | 60 95 | inariuO ju | MHz | 2-3 |
| t _{PLH} | Propagation Delay, CP to Q _n (PE Input HIGH or LOW) | 3.3 5.0 | 2.0 | 7.5 5.5 | 12.5 9.0 | 1.0 1.0 | 13.5 9.5 | 1.5 1.0 | 13.5 9.5 | ns | 2-6 |
| t _{PHL} | Propagation Delay, CP to Q _n (PE Input HIGH or LOW) | 3.3 5.0 | 1.5 1.5 | 8.5 6.0 | 12.0 9.5 | 1.0 | 12.5 9.5 | 1.5 1.5 | 13.0 10.0 | ns | 2-6 |
| t _{PLH} | Propagation Delay CP to TC | 3.3 5.0 | 3.0 2.0 | 9.5 7.0 | 15.0 10.5 | 1.0 | 16.5 11.0 | 2.5 1.5 | 16.5 11.5 | ns | 2-6 |
| t _{PHL} | Propagation Delay CP to TC | 3.3 5.0 | 3.5 2.0 | 11.0 8.0 | 14.0 11.0 | 1.0 | 15.0 11.0 | 2.5 2.0 | 15.5 11.5 | ns | 2-6 |
| t _{PLH} | Propagation Delay CET to TC | 3.3 5.0 | 2.0 1.5 | 7.5 5.5 | 9.5 6.5 | 1.0 | 11.0 7.5 | 1.5 1.0 | 11.0 7.5 | ns | 2-6 |
| t _{PHL} | Propagation Delay CET to TC | 3.3 5.0 | 2.5 2.0 | 8.5 6.0 | 11.0 8.5 | 1.0 | 12.0 9.0 | 2.0 1.5 | 12.5 9.5 | ns | 2-6 |

^{*}Voltage Range 3.3 is 3.3V ± 0.3 V Voltage Range 5.0 is 5.0V ± 0.5 V

AC Operating Requirements

| Symbol | THUCK V | | 74. | AC | 54AC | 74AC | HG CAN | HO |
|--------------------|---|--------------------------|-----------------------------------|-----------------|---|--|--------|-------------|
| | Parameter | V _{CC} * (V) | T _A = C _L = | + 25°C 50 pF | $T_A = -55^{\circ}C$ to $+125^{\circ}C$ $C_L = 50 pF$ | $T_A = -40^{\circ}C$ to $+85^{\circ}C$ $C_L = 50 \text{ pF}$ | Units | Fig. No. |
| | | | Тур | | Guaranteed Min | imum | | |
| t _s | Setup Time, HIGH or LOW P _n to CP | 3.3 5.0 | 5.5 4.0 | 13.5 8.5 | 17.0 11.0 | 16.0 10.5 | ns | |
| th | Hold Time, HIGH or LOW P _n to CP | 3.3 5.0 | -7.0 -5.0 | -1.0 0 | -0.5 0 | -0.5 0 | ns | 2-9 |
| t _s | Setup Time, HIGH or LOW SR to CP | 3.3 5.0 | 5.5 4.0 | 14.0 9.5 | | | ns | 2-9 |
| th | Hold Time, HIGH or LOW | 3.3 5.0 | -7.5 -5.5 | -1.0 -0.5 | -0.5 0 | -0.5 0 | ns | 2-9 |
| t _s ver | Setup Time, HIGH or LOW PE to CP | 3.3 5.0 | 5.5 4.0 | 11.5 7.5 | 16.0 9.5 | 14.0 8.5 | ns | 2-9 |
| t _h | Hold Time, HIGH or LOW PE to CP | 3.3 5.0 | -7.5 -5.0 | -1.0 -0.5 | -0.5 0 | -0.5 0 | ns | 2-9 |
| t _s | Setup Time, HIGH or LOW CEP or CET to CP | 3.3 5.0 | 3.5 2.5 | 6.0 4.5 | 8.0 5.5 | 7.0 5.0 | ns | 2-9 |
| t _h | Hold Time, HIGH or LOW CEP or CET to CP | 3.3 5.0 | -4.5 -3.0 | 0 | 0 0.5 | 0.5 | ns | 2-9 |
| t _w | Clock Pulse Width (Load) HIGH or LOW | 3.3 5.0 | 3.0 2.0 | 3.5 2.5 | 5.0 5.0 | 4.0 3.0 | ns | 2-6 |
| t _w | Clock Pulse Width (Count) HIGH or LOW | 3.3 5.0 | 3.0 2.0 | 4.0 3.0 | 5.0 5.0 | 4.5 3.5 | ns | 2-6 |

^{*}Voltage Range 3.3 is 3.3V ± 0.3 V Voltage Range 5.0 is 5.0V ± 0.5 V

AC Electrical Characteristics

| | anolihi | 000 | 2510 | 74ACT | TOKIO | 54 | ACT | 74 | CT | logimy | |
|------------------|---|-------------------|--|-------|-------|---|-----|--|------|--------|-------------|
| Symbol | Parameter | V _{CC} * | T _A = +25°C C _L = 50 pF | | | $T_A = -55^{\circ}C$ to $+125^{\circ}C$ $C_L = 50 pF$ | | T _A = -40°C to +85°C C _L = 50 pF | | Units | Fig. No. |
| | V0.8 = | DOV | Min | Тур | Max | Min | Max | Min | Max | | |
| f _{max} | Maximum Clock Frequency | 5.0 | 120 | 140 | | | | 105 | | MHz | 2-3 |
| t _{PLH} | Propagation Delay, CP to Q _n (PE Input HIGH or LOW) | 5.0 | 1.5 | 5.5 | 10.0 | | | 1.5 | 11.0 | ns | 2-6 |
| t _{PHL} | Propagation Delay, CP to Q _n (PE Input HIGH or LOW) | 5.0 | 1.5 | 6.0 | 11.0 | | | 1.5 | 12.0 | ns | 2-6 |
| t _{PLH} | Propagation Delay CP to TC | 5.0 | 2.5 | 7.0 | 11.5 | | | 2.0 | 13.5 | ns | 2-6 |
| t _{PHL} | Propagation Delay CP to TC | 5.0 | 3.0 | 8.0 | 13.5 | | | 2.0 | 15.0 | ns | 2-6 |
| t _{PLH} | Propagation Delay CET to TC | 5.0 | 2.0 | 5.5 | 9.0 | | | 1.5 | 10.5 | ns | 2-6 |
| t _{PHL} | Propagation Delay CET to TC | 5.0 | 2.0 | 6.0 | 10.0 | | | 2.0 | 11.0 | ns | 2-6 |

^{*}Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

| | | | 74 | ACT | 54ACT | 74ACT | | |
|----------------|--|--------------------------|------|-----------------|---|--|-------|-------------|
| Symbol | Parameter | V _{CC} * (V) | | + 25°C 50 pF | $T_A = -55^{\circ}C$ to $+125^{\circ}C$ $C_L = 50 pF$ | $T_A = -40^{\circ}C$ to $+85^{\circ}C$ $C_L = 50 \text{ pF}$ | Units | Fig. No. |
| | | | Тур | | Guaranteed Min | imum | | |
| t _s | Setup Time, HIGH or LOW Pn to CP | 5.0 | 4.0 | 10.0 | | 12.0 | ns | 2-9 |
| t _h | Hold Time, HIGH or LOW P _n to CP | 5.0 | -5.0 | 0.5 | | 0.5 | ns | 2-9 |
| ts | Setup Time, HIGH or LOW SR to CP | 5.0 | 4.0 | 10.0 | | 11.5 | ns | 2-9 |
| t _h | Hold Time, HIGH or LOW SR to CP | 5.0 | -5.5 | -0.5 | | -0.5 | ns | 2-9 |
| t _s | Setup Time, HIGH or LOW PE to CP | 5.0 | 4.0 | 8.5 | | 10.5 | ns | 2-9 |
| t _h | Hold Time, HIGH or LOW PE to CP | 5.0 | -5.5 | -0.5 | | 0 | ns | 2-9 |
| t _s | Setup Time, HIGH or LOW CEP or CET to CP | 5.0 | 2.5 | 5.5 | | 6.5 | ns | 2-9 |
| t _h | Hold Time, HIGH or LOW CEP or CET to CP | 5.0 | -3.0 | 0 | | 0.5 | ns | 2-9 |
| t _w | Clock Pulse Width (Load) HIGH or LOW | 5.0 | 2.0 | 3.5 | | 3.5 | ns | 2-6 |
| t _w | Clock Pulse Width (Count) HIGH or LOW | 5.0 | 2.0 | 3.5 | | 3.5 | ns | 2-6 |

^{*}Voltage Range 5.0 is 5.0V ± 0.5 V

Capacitance

| Symbol | Parameter | AC/ACT | Units | Conditions | |
|-----------------|----------------------------------|--------|-------|------------------------|--|
| Symbol | 2*06 - AT 2*23- | Тур | Omto | | |
| CIN | Input Capacitance | 4.5 | pF | V _{CC} = 5.0V | |
| C _{PD} | Power Dissipation Capacitance | 45.0 | pF | $V_{CC} = 5.0V$ | |

| | | | | lod |
|--|--|--|--|-----|
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | 000 |

ADVANCE INFORMATION



54AC/74AC164 • 54ACT/74ACT164 Serial-In, Parallel-Out Shift Register

General Description

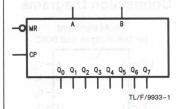
The 'AC/'ACT164 is a high-speed 8-bit serial-in/parallel-out shift register. Serial data is entered through a 2-input AND gate synchronous with the LOW-to-HIGH transition of the clock. The device features an asynchronous Master Reset which clears the register, setting all outputs LOW independent of the clock.

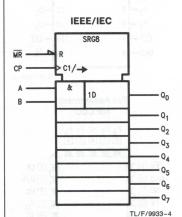
Features

- Asynchronous Master Reset
- Gated serial data input
- Fully synchronous data transfers
- 'ACT164 has TTL-compatible inputs

Logic Symbols

Connection Diagrams

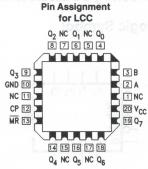




| A - 1 | 14 | -v _{cc} |
|------------------|------------------|------------------|
| B — 2 | Omnass 13 | -Q ₇ |
| $Q_0 - 3$ | 12 | -Q ₆ |
| Q ₁ 4 | (DACJ) 41 | -Q ₅ |
| $Q_2 - 5$ | (14000) 10 | -Q ₄ |
| $Q_3 - 6$ | e 100, Z . 50T = | - MR |
| GND - 7 | 102.4 (MAGE) 18 | -CP |
| - | 30 | TL/F/99 |

Pin Assignment for

DIP, SOIC and Flatpak



TL/F/9933-3

| Pin Names | Description |
|-------------|--|
| A, B | Data Inputs |
| CP | Clock Pulse Input (Active Rising Edge) |
| MR | Master Reset Input (Active LOW) |
| $Q_0 - Q_7$ | Outputs |



54AC/74AC169 4-Stage Synchronous Bidirectional Counter

General Description

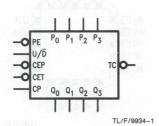
The 'AC169 is fully synchronous 4-stage up/down counter. The 'AC169 is a modulo-16 binary counter. It features a preset capability for programmable operation, carry lookahead for easy cascading and a U/D input to control the direction of counting. All state changes, whether in counting or parallel loading, are initiated by the LOW-to-HIGH transition of the Clock.

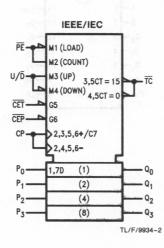
Features

- Synchronous counting and loading
- Built-In lookahead carry capability
- Presettable for programmable operation
- Outputs source/sink 24 mA

Ordering Code: See Section 5

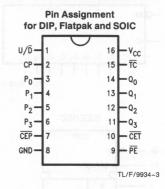
Logic Symbol

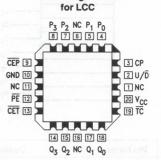




| Pin Names | Dascription | | | | | |
|--------------------------------|-----------------------------|--|--|--|--|--|
| CEP | Count Enable Parallel Input | | | | | |
| CET | Count Enable Trickle Input | | | | | |
| CP | Clock Pulse Input | | | | | |
| P ₀ -P ₃ | Parallel Data Inputs | | | | | |
| PE | Parallel Enable Input | | | | | |
| U/D | Up-Down Count Control Input | | | | | |
| $Q_0 - Q_3$ | Flip-Flop Outputs | | | | | |
| TC | Terminal Count Output | | | | | |

Connection Diagrams

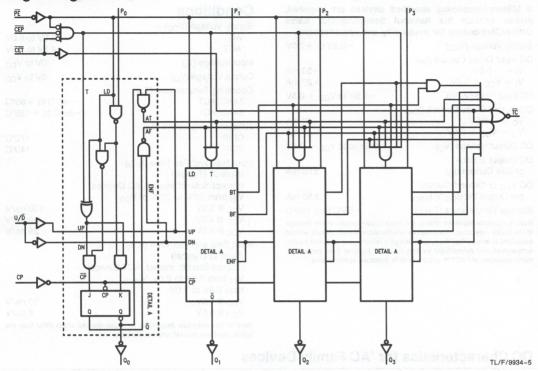




Pin Assignment

TL/F/9934-4

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Functional Description

The 'AC169 uses edge-triggered J-K-type flip-flops and have no constraints on changing the control or data input signals in either state of the Clock. The only requirement is that the various inputs attain the desired state at least a setup time before the rising edge of the clock and remain valid for the recommended hold time thereafter. The parallel load operation takes precedence over the other operations, as indicated in the Mode Select Table. When PE is LOW, the data on the Po-P3 inputs enters the flip-flops on the next rising edge of the Clock. In order for counting to occur, both CEP and CET must be LOW and PE must be HIGH; the U/D input then determines the direction of counting. The Terminal Count (TC) output is normally HIGH and goes LOW, provided that CET is LOW, when a counter reaches zero in the Count Down mode or reaches 15 in the Count Up mode. The TC output state is not a function of the Count Enable Parallel (CEP) input level. If an illegal state occurs, the 'AC169 will return to the legitimate sequence within two counts. Since the TC signal is derived by decoding the flipflop states, there exists the possibility of decoding spikes on TC. For this reason the use of TC as a clock signal is not recommended (see logic equations below).

- 1) Count Enable = CEP•CET•PE
- 2) Up: $\overline{TC} = Q_0 \cdot Q_1 \cdot Q_2 Q_3 \cdot (Up) \cdot \overline{CET}$
- 3) Down: $\overline{TC} = \overline{Q}_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet \overline{Q}_3 \bullet (Down) \bullet \overline{CET}$

Mode Select Table

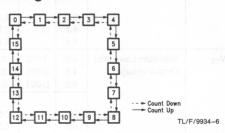
| PE | CEP | CET | U/D | Action on Rising Clock Edge |
|----|-------|-----|-----|--------------------------------|
| La | X | X | X | Load (Pn to Qn) |
| H | esL a | L | H | Count Up (Increment) |
| Н | L | L | L | Count Down (Decrement) |
| Н | Н | X | X | No Change (Hold) |
| H | X | Н | X | No Change (Hold) |

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

State Diagrams



Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Supply Voltage (V _{CC}) | -0.5V to $+7.0$ V |
|---|-----------------------------------|
| DC Input Diode Current (I _{IK}) | |
| $V_{I} = -0.5V$ | -20 mA |
| $V_I = V_{CC} + 0.5V$ | + 20 mA |
| DC Input Voltage (V _I) | -0.5 V to $V_{CC} + 0.5$ V |
| DC Output Diode Current (IOK) | |
| $V_0 = -0.5V$ | -20 mA |
| $V_O = V_{CC} + 0.5V$ | + 20 mA |
| DC Output Voltage (V _O) | -0.5 V to to V_{CC} + 0.5 V |
| DC Output Source | |
| or Sink Current (I _O) | ±50 mA |
| DC V _{CC} or Ground Current | |
| per Output Pin (ICC or IGND) | ±50 mA |
| Storage Temperature (T _{STG}) | -65°C to +150°C |
| | |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

Recommended Operating Conditions

| Conditions | |
|---|-----------------------------------|
| Supply Voltage (V _{CC}) | |
| 'AC' 'ACT | 2.0V to 6.0V 4.5V to 5.5V |
| Input Voltage (V _I) | 0V to V _{CC} |
| Output Voltage (VO) | 0V to V _{CC} |
| Operating Temperature (T _A) 74AC/ACT 54AC/ACT | -40°C to +85°C -55°C to +125°C |
| Junction Temperature (T _J) CDIP PDIP | 175°C 140°C |
| Input Rise and Fall Time (t _r , t _f) (Note 2) (Typical) (Except Schmitt Inputs) 'AC Devices V _{IN} from 30% to 70% of V _{CC} | |
| V _{CC} @ 3.0V | 150 ns/V |
| V _{CC} @ 4.5V V _{CC} @ 5.5V | 40 ns/V 25 ns/V |
| Input Rise and Fall Time (t _r , t _f) (Note 2) (Typical) (Except Schmitt Inputs) 'ACT Devices V _{IN} from 0.8V to 2.0V, V _{meas} | |
| from 0.8V to 2.0V V _{CC} @ 4.5V V _{CC} @ 5.5V | 10 ns/V 8 ns/V |

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

| | est relegropagakon da laya | | 74 | AC | 54AC | 74AC | rab sint lari | olon eass!" | |
|-----------------|---|-------------------|-------------------------|----------------------|-------------------------------------|---------------------------------|--|--|--|
| Symbol | Parameter | V _{CC} | T _A = | + 25°C | T _A = -55°C to + 125°C | T _A = -40°C to +85°C | Units | Conditions | |
| 91 | lali-ino noiseA | | Тур | 90 X | Guaranteed L | imits of other proper | do no at | have no constrain | |
| V _{IH} | Minimum High Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | ins V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{IL} | Maximum Low Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{OH} | Minimum High Level Output Voltage | 3.0 4.5 5.5 | 2.99 4.49 5.49 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | ed Journ en Victor alud (01 | $I_{OUT} = -50 \mu\text{A}$ | |
| | 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - | 3.0 4.5 5.5 | | 2.56 3.86 4.86 | 2.4 3.7 4.7 | 2.46 3.76 4.76 | Open in a second | $\begin{tabular}{ll} *V_{\mbox{\scriptsize IN}} &= V_{\mbox{\scriptsize IL}} \mbox{ or } V_{\mbox{\scriptsize IH}} \\ &- 12 \mbox{ mA} \\ I_{\mbox{\scriptsize OH}} &- 24 \mbox{ mA} \\ &- 24 \mbox{ mA} \\ \end{tabular}$ | |
| V _{OL} | Maximum Low Level Output Voltage | 3.0 4.5 5.5 | 0.002 0.001 0.001 | 0.1 0.1 0.1 | 0.1 an fige p 0.1 an fige 0.1 | 0.1 0.1 0.1 | sni stax c. Vi o e logic e | I _{OUT} = 50 μA | |
| | (10 Mars) = 1 1 1 1 1 1 1 1 1 1 | 3.0 4.5 5.5 | | 0.36 0.36 0.36 | 0.50 0.50 0.50 | 0.44 0.44 0.44 | ٧ | ${\rm *V_{IN} = V_{IL} or V_{IH}} \\ {\rm 12 mA} \\ {\rm I_{OL}} \qquad 24 {\rm mA} \\ 24 {\rm mA} \\ }$ | |
| I _{IN} | Maximum Input Leakage Current | 5.5 | | ±0.1 | ± 1.0 | ±1.0 | μА | $V_{I} = V_{CC}$, GND | |

DC Characteristics for 'AC Family Devices (Continued)

| Symbol | Parameter at | | 74/ | AC | 54AC | 74AC | | | |
|--------|-------------------------------------|---------------------|---------------|------|----------------------------------|---------------------------------|----------|---|--|
| | | V _{CC} (V) | CRURAL COLUMN | | T _A = -55°C to +125°C | T _A = -40°C to +85°C | Units | Conditions | |
| | | | Тур | 0 | Guaranteed I | Limits | asins m. | Symbol | |
| lold | †Minimum Dynamic | 5.5 | 5-eine | Guar | 50 | 75 | mA | V _{OLD} = 1.65V Max | |
| IOHD | Output Current | 5.5 | | | -50 | -75 | mA | V _{OHD} = 3.85V Min | |
| Icc | Maximum Quiescent Supply Current | 5.5 | 4.5 | 8.0 | 160.0 | 80.0 | μΑ | V _{IN} = V _{CC} or GND | |

^{*}All outputs loaded; thresholds on input associated with output under test.

AC Electrical Characteristics

| Symbol | Parameter | | 2.0 | 74AC16 | 9 | 54A | C169 | 74A | C169 | | 15 |
|------------------|---|-------------------|------------|-------------|--------------|---|--------------|--|--------------|-------|-------------|
| | | V _{CC} * | | | | $T_A = -55^{\circ}C$ to $+125^{\circ}C$ $C_L = 50 pF$ | | $T_A = -40^{\circ}C$ $to +85^{\circ}C$ $C_L = 50 pF$ | | Units | Fig. No. |
| | | | Min | Тур | Max | Min | Max | Min | Max | | |
| f _{max} | Maximum Clock Frequency | 3.3 5.0 | 75 100 | 118 154 | i.o | 55 75 | | 65 90 | | MHz | 2-3 |
| t _{PLH} | Propagation Delay CP to Qn (PE HIGH or LOW) | 3.3 5.0 | 2.5 1.5 | 9.5 7.0 | 13.0 10.0 | 1.0 | 15.0 12.0 | 2.0 1.5 | 14.5 11.0 | ns | 2-6 |
| t _{PHL} | Propagation Delay CP to Qn (PE HIGH or LOW) | 3.3 5.0 | 2.5 1.5 | 10.5 7.5 | 14.5 11.0 | 1.0 1.0 | 16.5 13.0 | 2.0 1.5 | 16.0 12.0 | ns | 2-6 |
| t _{PLH} | Propagation Delay CP to TC | 3.3 5.0 | 4.5 3.0 | 13.5 9.5 | 18.0 13.0 | 1.0 1.0 | 22.0 16.0 | 3.5 2.0 | 22.0 14.0 | ns | 2-6 |
| t _{PHL} | Propagation Delay CP to TC | 3.3 5.0 | 3.5 2.5 | 13.5 9.5 | 18.0 13.0 | 1.0 | 22.0 16.0 | 3.0 2.0 | 20.5 14.5 | ns | 2-6 |
| t _{PLH} | Propagation Delay CET to TC | 3.3 5.0 | 3.5 3.0 | 11.0 | 15.0 10.5 | 1.0 | 18.5 13.0 | 3.0 2.5 | 16.5 12.0 | ns | 2-6 |
| t _{PHL} | Propagation Delay CET to TC | 3.3 5.0 | 3.0 2.0 | 9.5 7.0 | 12.5 9.0 | 1.0 1.0 | 16.0 11.0 | 2.5 1.5 | 14.5 10.0 | ns | 2-6 |
| ^t PLH | Propagation Delay U/D to TC | 3.3 5.0 | 3.5 2.5 | 11.0 8.0 | 15.0 10.5 | 1.0 1.0 | 18.5 13.0 | 3.0 2.0 | 17.0 12.0 | ns | 2-6 |
| t _{PHL} | Propagation Delay | 3.3 5.0 | 2.5 1.5 | 10.0 7.0 | 13.5 9.5 | 1.0 | 16.5 12.0 | 2.0 1.5 | 15.5 10.5 | ns | 2-6 |

^{*}Voltage Range 3.3 is 3.3V ±0.3V

[†]Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}. I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

Voltage Range 5.0 is 5.0V ± 0.5 V

AC Operating Requirements

| | | | 744 | C169 | 54AC169 | 74AC169 | | |
|----------------------|--|-------------------|--|-------------|---|--|---------|-----------|
| Symbol | Parameter | V _{CC} * | T _A = +25°C C _L = 50 pF | | $T_A = -55^{\circ}C$ to $+125^{\circ}C$ $C_L = 50 pF$ | $T_A = -40^{\circ}C$ to $+85^{\circ}C$ $C_L = 50 \text{ pF}$ | Units | Fig No |
| uski vebu | e yok Am | | Тур | ā - | Guaranteed Mini | mum | aniko 1 | 1.040 |
| t _s vas.s | Setup Time, HIGH or LOW P _n to CP | 3.3 5.0 | 3.0 1.5 | 4.5 2.5 | 7.0 4.5 | 5.0 2.5 | ns | 2- |
| t _h | Hold Time, HIGH or LOW P _n to CP | 3.3 5.0 | 1.5 0.5 | 0.5 1.5 | 2.0 2.5 | 0.5 1.5 | ns | 2- |
| t _s | Setup Time, HIGH or LOW CEP to CP | 3.3 5.0 | 7.5 4.5 | 10.5 7.0 | 13.5 9.0 | 12.5 8.0 | ns | 2- |
| t _h | Hold Time, HIGH or LOW CEP to CP | 3.3 5.0 | 4.5 2.0 | 0 0.5 | 0.5 2.5 | 0 1.0 | ns | 2- |
| t _s | Setup Time, HIGH or LOW CET to CP | 3.3 5.0 | 7.0 4.0 | 10.0 6.5 | 13.5 9.5 | 12.0 8.0 | ns | 2- |
| th | Hold Time, HIGH or LOW CET to CP | 3.3 5.0 | 6.0 4.0 | 0 0.5 | 0.5 2.5 | 0 | ns | 2- |
| t _s | Setup Time, HIGH or LOW PE to CP | 3.3 5.0 | 3.5 2.0 | 5.5 3.5 | 8.5 6.5 | 6.5 4.0 | ns | 2- |
| th | Hold Time, HIGH or LOW PE to CP | 3.3 5.0 | 3.5 1.5 | 0 | 0.5 2.0 | 0 0.5 | ns | 2- |
| t _s | Setup Time, HIGH or LOW U/D to CP | 3.3 5.0 | 7.0 4.5 | 10.0 6.5 | 13.0 9.0 | 7.5 | ns | 2- |
| t _h | Hold Time, HIGH or LOW U/D to CP | 3.3 5.0 | 7.0 4.0 | 0 0.5 | 0.5 2.0 | 0 0.5 | ns | 2- |
| t _w | CP Pulse Width, HIGH or LOW | 3.3 5.0 | 2.0 2.0 | 3.0 3.0 | 5.0 5.0 | 4.0 | ns | 2- |

*Voltage Range 3.3 is 3.3V ± 0.3 V Voltage Range 5.0 is 5.0V ± 0.5 V

Capacitance

| Symbol | Parameter | AC/ACT | Units | Conditions |
|-----------------|----------------------------------|--------|-------|------------------------|
| - Cymbol | 18.5 20 16.5 | Тур | 0.01 | S S S Ve |
| CIN | Input Capacitance | 4.5 | pF | $V_{CC} = 5.0V$ |
| C _{PD} | Power Dissipation Capacitance | 60.0 | pF | V _{CC} = 5.0V |



54AC/74AC174 • 54ACT/74ACT174 **Hex D Flip-Flop with Master Reset**

General Description

The 'AC/'ACT174 is a high-speed hex D flip-flop. The device is used primarily as a 6-bit edge-triggered storage register. The information on the D inputs is transferred to storage during the LOW-to-HIGH clock transition. The device has a Master Reset to simultaneously clear all flip-flops.

Features

- Outputs source/sink 24 mA
- 'ACT174 has TTL-compatible inputs

Ordering Code: See Section 5

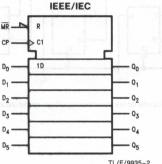
Logic Symbols

D₁ D₁ D₃ DA Da C1 1D Q₁ Q_2 Q_3 Q_4 D_2 TL/F/9935-1

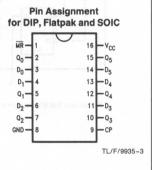
Pin Names Description D₀-D₅ Data Inputs CP Clock Pulse Input MR Master Reset Input

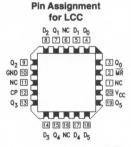
Outputs

Q0-Q5



Connection Diagrams





TL/F/9935-4

Functional Description

The 'AC/'ACT174 consists of six edge-triggered D flip-flops with individual D inputs and Q outputs. The Clock (CP) and Master Reset (MR) are common to all flip-flops. Each D input's state is transferred to the corresponding flip-flop's output following the LOW-to-HIGH Clock (CP) transition. A LOW input to the Master Reset (MR) will force all outputs LOW independent of Clock or Data inputs. The 'AC/'ACT174 is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

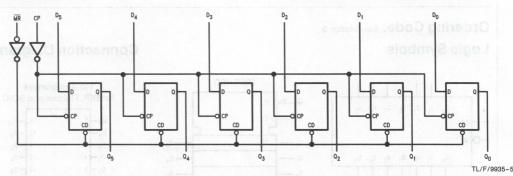
Truth Table

| The second of | Inputs | #3645 TVS | Output | | |
|---------------|--------|-----------|-------------|--|--|
| MR | СР | D | Q | | |
| L | X | X | A L | | |
| Н | _ | Н | H | | |
| Н | | L | The seal of | | |
| Н | F | X | Q | | |

- H = HIGH Voltage Level
- L = LOW Voltage Level
- X = Immaterial

 _ = LOW-to-HIGH Transition

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

8 ns/V

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Supply Voltage (V _{CC}) | -0.5V to $+7.0$ V |
|---|------------------------------|
| DC Input Diode Current (I _{IK}) | |
| $V_{I} = -0.5V$ | -20 mA |
| $V_I = V_{CC} + 0.5V$ | + 20 mA |
| DC Input Voltage (V _I) | -0.5 V to $V_{CC} + 0.5$ V |
| DC Outsid Diada Oussant (L.) | |

DC Output Diode Current (IOK) $V_0 = -0.5V$ -20 mA $V_O = V_{CC} + 0.5V$ +20 mA

DC Output Voltage (VO) -0.5V to to V_{CC} + 0.5V DC Output Source or Sink Current (IO) ±50 mA

DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND}) \pm 50 mA Storage Temperature (T_{STG}) -65°C to +150°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

Recommended Operating Conditions

| Supply Voltage (V _{CC}) 'AC 'ACT | | 2.0V to 6.0V 4.5V to 5.5V |
|---|------------------------|--|
| Input Voltage (V _I) | | 0V to V _{CC} |
| Output Voltage (V _O) | | OF THE CONTRACT OF THE CONTRAC |
| Operating Temperature 74AC/ACT | (T _A) | -40°C to +85°C |
| 54AC/ACT | 2.7 | -55°C to +125°C |
| PDIP | oosee 1 | 175°C 140°C |
| (Except Schmitt Inpu | ie (t _r , t | f) Belging the Vote of the last of the Control of t |
| V _{IN} from 30% to 709 V _{CC} @ 3.0V | % OT V | CC 150 ns/V |
| V _{CC} @ 4.5V V _{CC} @ 5.5V | | 40 ns/V 25 ns/V |
| Input Rise and Fall Tim (Note 2) (Typical) (Except Schmitt Inpu | ts) 'AC | CT Devices |
| V _{IN} from 0.8V to 2.0V from 0.8V to 2.0V | V, V _{me} | |
| V _{CC} @ 4.5V | | 10 ns/V |

V_{CC} @ 5.5V Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

| | $V = y_0 V^*$ | | 74 | AC | 54AC | 74AC | | | |
|---|--------------------------------------|---------------------|-------------------------|----------------------|-----------------------------------|---------------------------------|-------------------------------|--|--|
| Symbol | Parameter | V _{CC} (V) | T _A = +25°C | | T _A = -55°C to + 125°C | T _A = -40°C to +85°C | Units | Conditions | |
| | 19 = 190) A | 1. | Тур | | Guaranteed L | imits | all woll a | Minnxsivi 30V | |
| V _{IH} _{IV 10} J Am AS | Minimum High Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| VIL GNO | Maximum Low Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{OH} | Minimum High Level Output Voltage | 3.0 4.5 5.5 | 2.99 4.49 5.49 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | v n Dynan | $I_{OUT} = -50 \mu\text{A}$ | |
| | MA VOIGE NO | 3.0 | | 2.56 | 2.4 | 2.46 | uren: Duiesc | $V_{IN} = V_{IL} \text{ or } V_{IH} - 12 \text{ mA}$ | |
| | or GND | 4.5 5.5 | | 3.86 4.86 | 3.7 4.7 | 3.76 4.76 | V V | I _{OH} -24 mA -24 mA | |
| V _{OL} | Maximum Low Level Output Voltage | 3.0 4.5 5.5 | 0.002 0.001 0.001 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | 2.6 ms, o 25 V s to | $I_{OUT} = 50 \mu\text{A}$ | |
| | | 3.0 4.5 5.5 | | 0.36 0.36 0.36 | 0.50 0.50 0.50 | 0.44 0.44 0.44 | ٧ | $\begin{tabular}{ll} *V_{IN} &= V_{IL} \mbox{ or } V_{IH} \\ &= 12 \mbox{ mA} \\ I_{OL} &= 24 \mbox{ mA} \\ &= 24 \mbox{ mA} \\ \end{tabular}$ | |
| I _{IN} | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | ±1.0 | μА | $V_{I} = V_{CC}$, GND | |

DC Characteristics for 'AC Family Devices (Continued)

| | | | 7 | 4AC | 54AC | 74AC | Se sou | tostroo seesto | |
|------------------|-------------------------------------|---------------------|------------------------|--------------|----------------------------------|---|-------------------|------------------------------|--|
| Symbol Parameter | Parameter | V _{CC} (V) | T _A = +25°C | | T _A = -55°C to +125°C | $T_A = -40^{\circ}C \text{ to } +85^{\circ}C$ | Units | Conditions | |
| | V0 | | Тур | por Voices | Guaranteed Lin | al) men | DO Input Digde Ou | | |
| IOLD | †Minimum Dynamic | 5.5 | - (nV) e | estieV regit | 50 | 75 | mA | V _{OLD} = 1.65V Max | |
| IOHD | Output Current | 5.5 | niesedin | TOALCAST | -50 | or V3.0 -75 | mA | V _{OHD} = 3.85V Min | |
| Icc | Maximum Quiescent Supply Current | ent 5.5 8.0 | | 8.0 | 160.0 | 80.0 | μА | $V_{IN} = V_{CC}$ or GND | |

^{*}All outputs loaded; thresholds on input associated with output under test.

DC Characteristics for 'ACT Family Devices

| | | | 74 | CT | 54ACT | 74ACT | spriter of | Moral of Abrol (dominion |
|----------------------|--------------------------------------|------------------------|------------------------|--------------|-----------------------------------|---------------------------------|------------|---|
| Symbol | Parameter | V _{CC} (V) | T _A = +25°C | | T _A = -55°C to + 125°C | T _A = -40°C to +85°C | Units | Conditions |
| | CT Devices | A^ (8100 | Тур | 8 fuebx: | Guaranteed L | imits | Shippio W | EOA 3 to consuder on a re- |
| V _{IH} | Minimum High Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 2.0 2.0 | 2.0 2.0 | 2.0 2.0 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ |
| VIL | Maximum Low Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 0.8 0.8 | 0.8 0.8 | 0.8 0.8 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ |
| V _{OH} | Minimum High Level Output Voltage | 4.5 5.5 | 4.49 5.49 | 4.4 5.4 | 4.4 5.4 | 4.4 5.4 | V | $I_{OUT} = -50 \mu\text{A}$ |
| | none Gran | 4.5 5.5 | Y T | 3.86 4.86 | 3.70 4.70 | 3.76 4.76 | ٧ | $V_{\text{IN}} = V_{\text{IL}} \text{ or } V_{\text{IH}}$ -24 mA -24 mA |
| V _{OL} | Maximum Low Level Output Voltage | 4.5 5.5 | 0.001 0.001 | 0.1 0.1 | 0.1 0.1 | 0.1 0.1 | ٧ | $I_{OUT} = 50 \mu A$ |
| | = 51.0V 00V 10 V | 4.5 5.5 | | 0.36 0.36 | 0.50 0.50 | 0.44 0.44 | ٧ | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $I_{OL} \qquad 24 \text{ mA}$ 24 mA |
| I _{IN} VI.0 | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 agr | 85.5 ±1.0 | μΑ | $V_I = V_{CC}$, GND |
| Ісст | Maximum I _{CC} /Input | 5.5 | 0.6 | | 95 1.6 85 | 00.5 1.5 | mA | $V_{I} = V_{CC} - 2.1V$ |
| I _{OLD} | †Minimum Dynamic | 5.5 | | | 50 | 75 | mA | V _{OLD} = 1.65V Max |
| IOHD | Output Current | 5.5 | | | -50 | -75 | mA | V _{OHD} = 3.85V Min |
| lcc | Maximum Quiescent Supply Current | 5.5 | | 8.0 | 160.0 | 80.0 | μΑ | $V_{IN} = V_{CC}$ or GND |

^{*}All outputs loaded; thresholds on input associated with output under test.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

[†]Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC} . I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

[†]Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics

| Symbol | TOANT | 1 | 3A48 | 74AC | | | 54AC | | AC | | |
|------------------|---|-------------------|--|------------|-------------|--|--------------|--|--------------------|-------|------|
| | Parameter of | V _{CC} * | T _A = +25°C C _L = 50 pF | | | T _A = -55°C to + 125°C C _L = 50 pF | | T _A = -40°C to +85°C C _L = 50 pF | | Units | Fig. |
| | | olniki ba | Min | Тур | Max | Min | Max | Min | Max | | |
| f _{max} | Maximum Clock Frequency | 3.3 5.0 | 90 100 | 100 125 | 0.6 | 65 90 | - W(| 70 100 | i saiT qu i | MHz | 2-3 |
| t _{PLH} | Propagation Delay CP to Q _n | 3.3 5.0 | 2.0 1.5 | 9.0 6.0 | 11.5 8.5 | 1.0 1.0 | 14.0 10.5 | 1.5 1.0 | 12.5 9.5 | ns | 2-6 |
| t _{PHL} | Propagation Delay CP to Q _n | 3.3 5.0 | 2.0 1.5 | 8.5 6.0 | 11.0 8.0 | 1.0 1.0 | 13.0 10.0 | 1.5 1.0 | 12.0 9.0 | ns | 2-6 |
| t _{PHL} | Propagation Delay MR to Qn | 3.3 5.0 | 2.5 1.5 | 9.0 7.0 | 11.5 9.0 | 1.0 1.0 | 13.5 11.0 | 2.0 1.5 | 12.5 10.5 | 5 ns | 2-6 |

^{*}Voltage Range 3.3 is 3.3V ±0.3V Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

| Symbol | Parameter Vol. 8 - 3 - 3 - 3 | | 74 | AC | 54AC | 74AC | | Fig. |
|------------------|---|--------------------------|------------|-----------------|--|--|-------|------|
| | | V _{CC} * (V) | | + 25°C 50 pF | $T_A = -55^{\circ}C$ to $+ 125^{\circ}C$ $C_L = 50 pF$ | T _A = -40°C to +85°C C _L = 50 pF | Units | |
| | 1/0.2 | | Тур | 0.30 | Guaranteed Min | imum wo 3 | | |
| t _s | Setup Time, HIGH or LOW D _n to CP | 3.3 5.0 | 2.5 2.0 | 6.5 5.0 | 7.5 5.5 | 7.0 5.5 | ns | 2-9 |
| t _h | Hold Time, HIGH or LOW D _n to CP | 3.3 5.0 | 1.0 0.5 | 3.0 3.0 | 3.0 3.0 | 3.0 3.0 | ns | 2-9 |
| t _w | MR Pulse Width, LOW | 3.3 5.0 | 1.0 1.0 | 5.5 5.0 | 7.0 5.0 | 7.0 5.0 | ns | 2-6 |
| t _w | CP Pulse Width | 3.3 5.0 | 1.0 1.0 | 5.5 5.0 | 7.0 5.0 | 7.0 5.0 | ns | 2-6 |
| t _{rec} | Recovery Time MR to CP | 3.3 5.0 | 0 | 2.5 2.0 | 3.0 2.0 | 2.5 2.0 | ns | 2-6 |

^{*}Voltage Range 3.3 is 3.3V ±0.3V Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics

| | Parameter | V _{CC} * | | 74ACT | | 54 | ACT | 74/ | ACT | | |
|------------------|---|-------------------|--|-------|------|--|------|--|------|-------|-------------|
| Symbol | | | T _A = +25°C C _L = 50 pF | | | T _A = -55°C to + 125°C C _L = 50 pF | | T _A = -40°C to +85°C C _L = 50 pF | | Units | Fig. No. |
| | | | Min | Тур | Max | Min | Max | Min | Max | | |
| f _{max} | Maximum Clock Frequency | 5.0 | 165 | 200 | | 95 | | 140 | | MHz | 2-3 |
| t _{PLH} | Propagation Delay CP to Q _n | 5.0 | 1.5 | 7.0 | 10.5 | 1.0 | 12.5 | 1.5 | 11.5 | ns | 2-6 |
| t _{PHL} | Propagation Delay CP to Q _n | 5.0 | 1.5 | 7.0 | 10.5 | 1.0 | 13.0 | 1.5 | 11.5 | ns | 2-6 |
| t _{PHL} | Propagation Delay | 5.0 | 1.5 | 6.5 | 9.5 | 1.0 | 12.0 | 1.5 | 11.0 | ns | 2-6 |

^{*}Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

| | C PARC | AAR | 744 | CT | 54ACT | 74ACT | | |
|------------------|---|-------------------|--|-----|--|--|-------|-------------|
| Symbol | Parameter | V _{CC} * | $T_A = +25^{\circ}C$ $C_L = 50 \text{ pF}$ | | $T_A = -55^{\circ}C$ $to + 125^{\circ}C$ $C_L = 50 pF$ | $T_A = -40^{\circ}C$ to $+85^{\circ}C$ $C_L = 50 pF$ | Units | Fig. No. |
| | reti nist usid | 71688 | Тур | QUI | Guaranteed Min | imum | | |
| ts | Setup Time, HIGH or LOW D _n to CP | 5.0 | 0.5 | 1.5 | 0013.0 | 1.5 years | ns | 2-9 |
| th | Hold Time, HIGH or LOW D _n to CP | 5.0 | 1.0 | 2.0 | 3.1 2.0 0.3 | 2.0 | ns | 2-9 |
| t _w | MR Pulse Width, LOW | 5.0 | 1.5 | 3.0 | 5.0 | 3.5 | ns | 2-6 |
| t _w | CP Pulse Width, HIGH OR LOW | 5.0 | 1.5 | 3.0 | 5.0 | 3.5 | ns | 2-6 |
| t _{rec} | Recovery Time MR to CP | 5.0 | -1.0 | 0.5 | 1.0 | 0.5 | ns | 2-9 |

^{*}Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

| Symbol | Parameter | AC/ACT | Units | Conditions |
|-----------------|-------------------------------|--------|--------|-----------------|
| Symbol | One Parameter | Тур | AT Too | V |
| C _{IN} | Input Capacitance | 4.5 | pF | $V_{CC} = 5.0V$ |
| C _{PD} | Power Dissipation Capacitance | 85.0 | pF | $V_{CC} = 5.0V$ |



54AC/74AC175 ● 54ACT/74ACT175 Quad D Flip-Flop

General Description

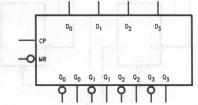
The 'AC/'ACT175 is a high-speed quad D flip-flop. The device is useful for general flip-flop requirements where clock and clear inputs are common. The information on the D inputs is stored during the LOW-to-HIGH clock transition. Both true and complemented outputs of each flip-flop are provided. A Master Reset input resets all flip-flops, independent of the Clock or D inputs, when LOW.

Features

- Edge-triggered D-type inputs
- Buffered positive edge-triggered clock
- Asynchronous common reset
- True and complement output
- Outputs source/sink 24 mA
- 'ACT175 has TTL-compatible inputs

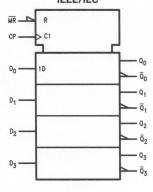
Ordering Code: See Section 5

Logic Symbols



TL/F/9936-1

IEEE/IEC



TL/F/9936-2

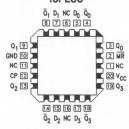
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/9936-3

Pin Assignment for LCC



TL/F/9936-4

| Pin Names | Description | |
|-----------------------------------|--------------------|--|
| D ₀ -D ₃ | Data Inputs | |
| CP | Clock Pulse Input | |
| MR | Master Reset Input | |
| Q ₀ -Q ₃ | True Outputs | |
| $\overline{Q}_0 - \overline{Q}_3$ | Complement Outputs | |

Functional Description

The 'AC/'ACT175 consists of four edge-triggered D flipflops with individual D inputs and Q and \overline{Q} outputs. The Clock and Master Reset are common. The four flip-flops will store the state of their individual D inputs on the LOW-to-HIGH clock (CP) transition, causing individual Q and \overline{Q} outputs to follow. A LOW input on the Master Reset (\overline{MR}) will force all Q outputs LOW and \overline{Q} outputs HIGH independent of Clock or Data inputs. The 'AC/'ACT175 is useful for general logic applications where a common Master Reset and Clock are acceptable.

Truth Table

| Inputs | Outputs | | |
|---------------------------|-------------------|----|--|
| @ t _n , MR = H | @ t _{n+} | -1 | |
| Dn | Qn | Qn | |
| L | ne Long and a | Н | |
| н 00 | Н | L | |

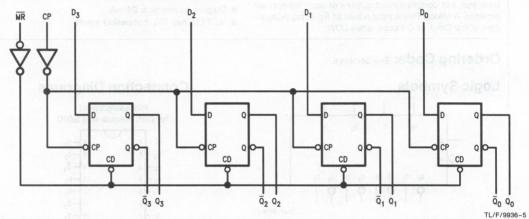
H = HIGH Voltage Level

L = LOW Voltage Level

t_n = Bit Time before Clock Pulse

t_{n+1} = Bit Time after Clock Pulse

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | my and operation |
|--|---------------------------------|
| Supply Voltage (V _{CC}) | -0.5V to $+7.0V$ |
| DC Input Diode Current (I_{IK}) $V_I = -0.5V$ $V_I = V_{CC} + 0.5V$ | −20 mA +20 mA |
| DC Input Voltage (V _I) | -0.5 V to $V_{CC} + 0.5$ V |
| DC Output Diode Current (I_{OK}) $V_O = -0.5V$ $V_O = V_{CC} + 0.5V$ | -20 mA +20 mA |
| DC Output Voltage (V _O) | -0.5 V to to $V_{CC} + 0.5$ V |
| DC Output Source or Sink Current (I _O) | ±50 mA |
| DC V _{CC} or Ground Current per Output Pin (I _{CC} or I _{GND}) | ±50 mA |

Storage Temperature (T_{STG}) Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

-65°C to +150°C

Recommended Operating Conditions

| Supply Voltage (V _{CC}) 'AC 'ACT | | 2.0V to 6.0V 4.5V to 5.5V |
|--|--------------------|------------------------------|
| 7.0. | | |
| Input Voltage (V _I) | | 0V to V _{CC} |
| Output Voltage (VO) | | 0V to V _{CC} |
| Operating Temperature | (T _A) | |
| 74AC/ACT | | -40°C to +85°C |
| 54AC/ACT | | -55°C to +125°C |
| Junction Temperature | (T _{.1}) | |
| CDIP | | 175°C |
| PDIP | | 140°C |
| Input Rise and Fall Tim (Note 2) (Typical) (Except Schmitt Inpu V _{IN} from 30% to 70° V _{CC} @ 3.0V | its) 'A | C Devices |
| V _{CC} @ 4.5V | | 40 ns/V |
| V _{CC} @ 5.5V | | 25 ns/V |
| Input Rise and Fall Tim (Note 2) (Typical) (Except Schmitt Inpu V _{IN} from 0.8V to 2.0 from 0.8V to 2.0V | its) 'A | CT Devices |
| V _{CC} @ 4.5V V _{CC} @ 5.5V | | 10 ns/V 8 ns/V |

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

| | 1/ | | 74 | AC | 54AC | 74AC | | | |
|---------------------|--------------------------------------|------------------------------|-------------------------|-----------------------|----------------------------------|---------------------------------|----------|---|--|
| Symbol | Parameter | arameter V _{CC} (V) | T _A = +25°C | | T _A = -55°C to +125°C | T _A = -40°C to +85°C | Units | Conditions | |
| | 8 01 | | Тур | Typ Guaranteed Limits | | | il water | | |
| V _{IH} | Minimum High Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{IL} | Maximum Low Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{OH} = - | Minimum High Level Output Voltage | 3.0 4.5 5.5 | 2.99 4.49 5.49 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | ٧ | $I_{OUT} = -50 \mu A$ | |
| niM Vas s | DV = NV AH | 3.0 4.5 5.5 | 3 | 2.56 3.86 4.86 | 2.4 3.7 4.7 | 2.46 3.76 4.76 | V | $*V_{IN} = V_{IL} \text{ or } V_{IH} -12 \text{ mA}$ $I_{OH} -24 \text{ mA}$ -24 mA | |
| V _{OL} | Maximum Low Level Output Voltage | 3.0 4.5 5.5 | 0.002 0.001 0.001 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | ٧ | I _{OUT} = 50 μA | |
| | | 3.0 4.5 5.5 | | 0.36 0.36 0.36 | 0.50 0.50 0.50 | 0.44 0.44 0.44 | ٧ | $*V_{IN} = V_{IL} \text{ or } V_{IH}$ 12 mA $I_{OL} \qquad 24 \text{ mA}$ 24 mA | |
| I _{IN} | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | ±1.0 | μΑ | $V_{I} = V_{CC}$, GND | |

DC Characteristics for 'AC Family Devices (Continued)

| | | | 74 | AC | 54AC | 74AC | age moga age outr | Conditions | |
|------------------|-------------------------------------|------------------------|------------------------------|------------|----------------------------------|---|----------------------|------------------------------|--|
| Symbol | Parameter | V _{CC} (V) | T _A = | + 25°C | T _A = -55°C to +125°C | $T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ | Units | | |
| | | | Тур | patieV tug | Guaranteed Lin | nits | yd) Jaen | DC Input Dicide Cu | |
| I _{OLD} | †Minimum Dynamic | 5.5 | (_O V) a n | dioV huglu | 50 | 75 | mA | V _{OLD} = 1.65V Max | |
| IOHD | Output Current | 5.5 | nutstadnie | I prosec | -50 | or ∀∂ 0 −75 | mA | V _{OHD} = 3.85V Min | |
| I _{CC} | Maximum Quiescent Supply Current | 5.5 | T Homeleich eine | 8.0 | 160.0 | 80.0 | μΑ | $V_{IN} = V_{CC}$ or GND | |

^{*}All outputs loaded; thresholds on input associated with output under test.

Note: $I_{|N}$ and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC} . I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

| Vian 83 | | | 744 | CT | 54ACT | 74ACT | na rating Salah | moder exposure or trust to the device may be out | |
|----------------------|--------------------------------------|------------------------|------------------|--------------|----------------------------------|---------------------------------|--------------------|--|--|
| Symbol | Parameter | V _{CC} (V) | T _A = | + 25°C | T _A = -55°C to +125°C | T _A = -40°C to +85°C | Units | Conditions | |
| | SSURVEQ 149 | n (6284) nV VO | Тур | emont is | Guaranteed L | imits | | | |
| V _{IH} | Minimum High Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 2.0 2.0 | 2.0 2.0 | 2.0 2.0 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{IL} | Maximum Low Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 0.8 | 0.8 0.8 | 0.8 0.8 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{OH} | Minimum High Level Output Voltage | 4.5 5.5 | 4.49 5.49 | 4.4 5.4 | 4.4 5.4 | 4.4 5.4 | ٧ | $I_{OUT} = -50 \mu\text{A}$ | |
| | FC Units Cons | 4.5 5.5 | Y 0104-4 | 3.86 4.86 | 3.70 4.70 | 3.76 4.76 | ٧ | $V_{\rm IN} = V_{\rm IL} \text{ or } V_{\rm IH}$ -24 mA -24 mA | |
| V _{OL} | Maximum Low Level Output Voltage | 4.5 5.5 | 0.001 | 0.1 | 0.1 | 0.1 0.1 | ٧ | $I_{OUT} = 50 \mu A$ | |
| | 00 V 30 V | 4.5 5.5 | | 0.36 0.36 | 0.50 0.50 | 0.44 0.44 | v V | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ | |
| I _{IN} VIII | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | 35.5 ±1.0 | μΑ | $V_{I} = V_{CC}$, GND | |
| ICCT | Maximum I _{CC} /Input | 5.5 | 0.6 | | 1.6 | 68 S 1.5 A | mA | $V_{\rm I} = V_{\rm CC} - 2.1V$ | |
| I _{OLD} | †Minimum Dynamic | 5.5 | | | 50 | 75 | mA | V _{OLD} = 1.65V Max | |
| I _{OHD} | Output Current | 5.5 | | | -50 | -75 | mA | V _{OHD} = 3.85V Mir | |
| Icc | Maximum Quiescent Supply Current | 5.5 | | 8.0 | 160.0 | 80.0 | μΑ | $V_{IN} = V_{CC}$ or GND | |

^{*}All outputs loaded; thresholds on input associated with output under test.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

[†]Maximum test duration 2.0 ms, one output loaded at a time.

[†]Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics

| | 74407 | | TOAR | 74AC | | AAY ! | 54AC | 74 | 74AC | | |
|------------------|---|--------------------------|--|------------|-------------|---|--------------|--|---------------------|-------|-------------|
| Symbol Parameter | | V _{CC} * (V) | T _A = +25°C C _L = 50 pF | | | $T_A = -55^{\circ}C$ to $+125^{\circ}C$ $C_L = 50 pF$ | | T _A = -40°C to +85°C C _L = 50 pF | | Units | Fig. No. |
| | noth of | | Min | Тур | Max | Min | Max | Min | Max | | |
| f _{max} | Maximum Clock Frequency | 3.3 5.0 | 149 187 | 214 244 | | 95 95 | 0 175 | 139 187 | oc O mumi yensu, | MHz | 2-3 |
| t _{PHL} | Propagation Delay CP to Q_n or \overline{Q}_n | 3.3 5.0 | 2.0 1.5 | 9.5 7.0 | 9.0 | 1.0 1.0 | 15.0 11.5 | 2.0 1.0 | 13.5 9.5 | ns | 2-6 |
| t _{PLH} | Propagation Delay CP to Q_n or \overline{Q}_n | 3.3 5.0 | 2.5 1.5 | 8.5 6.0 | 13.0 9.5 | 1.0 | 14.5 10.5 | 2.0 1.5 | 14.5 10.5 | ns | 2-6 |
| t _{PHL} | Propagation Delay | 3.3 5.0 | 3.0 2.0 | 7.5 5.5 | 12.5 9.0 | 1.0 1.0 | 13.5 10.5 | 2.5 1.5 | 13.5 10.0 | ns | 2-6 |
| t _{PLH} | Propagation Delay | 3.3 5.0 | 3.0 2.0 | 8.5 6.0 | 11.0 8.5 | 1.0 1.0 | 15.0 11.0 | 2.5 1.5 | 12.5 9.0 | ns | 2-6 |

*Voltage Range 3.3 is 3.3V ± 0.3 V Voltage Range 5.0 is 5.0V ± 0.5 V

AC Operating Requirements

| | 394 - 7 377 | 9 | 74. | AC | 54AC | 74AC | | |
|------------------|---|-------------------|--|------------|--|--|-------|-------------|
| Symbol | Parameter | V _{CC} * | T _A = +25°C C _L = 50 pF | | T _A = -55°C to + 125°C C _L = 50 pF | $T_A = -40^{\circ}C$ $to +85^{\circ}C$ $C_L = 50 pF$ | Units | Fig. No. |
| | SALUTANES W | 2.0 | Тур | 7.0 | Guaranteed Minimum | | | 7645 3 |
| ts | Setup Time, HIGH or LOW D _n to CP | 3.3 5.0 | 2.0 | 4.5 3.0 | 5.0 3.5 | 4.5 3.0 | ns | 2-9 |
| th S | Hold Time, HIGH or LOW D _n to CP | 3.3 5.0 | 1.0 1.0 | 1.0 1.0 | 2.0 2.5 | 1.0 1.0 | ns | 2-9 |
| t _w | CP Pulse Width HIGH or LOW | 3.3 5.0 | 5.5 4.0 | 4.5 3.5 | 6.0 5.0 | 4.5 3.5 | ns | 2-6 |
| t _w | MR Pulse Width, LOW | 3.3 5.0 | 5.5 4.0 | 4.5 3.5 | 5.5 5.0 | 5.0 3.5 | er ns | 2-6 |
| t _{rec} | Recovery Time MR to CP | 3.3 5.0 | 0 | 0 | 1.5 1.5 | 0 | ns | 2-9 |

*Voltage Range 3.3 is 3.3V ±0.3V Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics

| | DAAY | | | 74ACT | | 54 | ACT | 74ACT | | | |
|------------------|---|-------------------|--|-------|------|---|----------------|--|----------------------|-------|------|
| Symbol | Parameter | V _{CC} * | T _A = +25°C C _L = 50 pF | | | $T_A = -55^{\circ}C$ to + 125°C $C_L = 50 \text{ pF}$ | | $T_A = -40^{\circ}C$ to $+85^{\circ}C$ $C_L = 50 pF$ | | Units | Fig. |
| | as id 68 | | Min | Тур | Max | Min | Max | Min | Max | | |
| f _{max} | Maximum Clock Frequency | 5.0 | 175 | 236 | | 95 | 3 449 0 187 | 145 | ilmum Cled Juency | MHz | 2-3 |
| t _{PLH} | Propagation Delay CP to Q_n or \overline{Q}_n | 5.0 | 2.0 | 6.0 | 10.0 | 1.0 | 11.5 | 1.5 | 11.0 | ns | 2-6 |
| t _{PHL} | Propagation Delay CP to Q_n or \overline{Q}_n | 5.0 | 2.0 | 7.0 | 11.0 | 1.0 | 12.5 | 1.5 | 12.0 | ns | 2-6 |
| t _{PLH} | Propagation Delay MR to Qn | 5.0 | 2.0 | 6.0 | 9.5 | 1.0 | 11.5 | 1.5 | 10.5 | ns | 2-6 |
| t _{PHL} | Propagation Delay \overline{MR} to \overline{Q}_n | 5.0 | 2.0 | 5.5 | 9.5 | 1.0 | 11.0 | 1.5 | 10.5 | ns | 2-6 |

^{*}Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

| | | | 744 | CT | 54ACT | 74ACT | | |
|--|--|-------------------|--|------------|--|--|-------|-------------|
| Symbol | Parameter | V _{CC} * | $T_A = +25^{\circ}C$ $C_L = 50 \text{ pF}$ | | T _A = -55°C to + 125°C C _L = 50 pF | $T_A = -40^{\circ}C$ $to +85^{\circ}C$ $C_L = 50 pF$ | Units | Fig. No. |
| 30 02 30 1 30 | | 00 = 00 | Тур | | Guaranteed Min | | | |
| t _s (H) t _s (L) | Setup Time D _n to CP | 5.0 | 3.0 3.0 | 2.0 2.5 | 3.5 3.5 | 2.0 2.5 | ns | 2-9 |
| t _h | Hold Time, HIGH or LOW D _n to CP | 5.0 | 0 | 1.0 | 1.5 | 1.0 | ns | 2-9 |
| t _w | CP Pulse Width HIGH or LOW | 5.0 | 4.0 | 3.0 | 5.0 | 3.5 | ns | 2-6 |
| t _w | MR Pulse Width, LOW | 5.0 | 4.0 | 3.0 | 5.0 | 4.0 | ns | 2-6 |
| t _{rec} | Recovery Time, MR to CP | 5.0 | 0 | 0 | 1.5 | 0 | ns | 2-9 |

^{*}Voltage Range 5.0 is 5.0V \pm 0.5V

Capacitance

| Symbol | Parameter | AC/ACT | Units | Conditions | |
|-----------------|----------------------------------|--------|-------|-----------------|--|
| | raiailletei | Тур | Onits | | |
| CIN | Input Capacitance | 4.5 | pF | $V_{CC} = 5.0V$ | |
| C _{PD} | Power Dissipation Capacitance | 45.0 | pF | $V_{CC} = 5.0V$ | |





54ACT/74ACT181 **4-Bit Arithmetic Logic Unit**

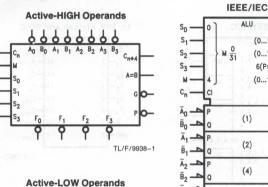
General Description

The 'ACT181 is a 4-bit Arithmetic Logic Unit (ALU) which can perform all the possible 16 logic operations on two variables and a variety of arithmetic operations.

Features

- Full lookahead for high-speed arithmetic operation on long words
- 'ACT181 has TTL-compatible inputs

Logic Symbols



(0...15) CP ē (0...15) CG 6(P=Q) △ (0...15) CO

TL/F/9938-4

Ā3 · (8)

Pin Assignment for DIP, SOIC and Flatpak

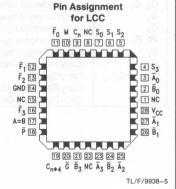
Connection Diagrams



TL/F/9938-3

TL/F/9938-2

| Pin Names | Description | | | | |
|-----------------------------------|-------------------------------------|--|--|--|--|
| $\overline{A}_0 - \overline{A}_3$ | A Operand Inputs (Active LOW) | | | | |
| $\overline{B}_0 - \overline{B}_3$ | B Operand Inputs (Active LOW) | | | | |
| S ₀ -S ₃ | Function Select Inputs | | | | |
| M | Mode Control Input | | | | |
| Cn | Carry Input | | | | |
| $\overline{F}_0 - \overline{F}_3$ | Function Outputs (Active LOW) | | | | |
| A = B | Comparator Output | | | | |
| G | Carry Generate Output (Active LOW) | | | | |
| P | Carry Propagate Output (Active LOW) | | | | |
| C_{n+4} | Carry Output | | | | |





ADVANCE INFORMATION

54ACT/74ACT182 **Carry Lookahead Generator**

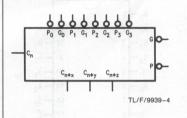
General Description

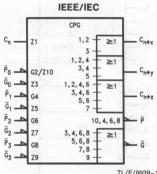
The 'ACT182 is a high-speed carry lookahead generator.

Features

- Provides lookahead carries across a group of four ALUS
- Multi-level lookahead high-speed arithmetic operation over long word lengths
- 'ACT182 has TTL-compatible inputs

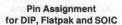
Logic Symbols

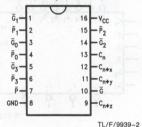




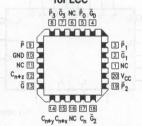
| | | IEEE/IE | | |
|-----------------------------------|--------------------|----------------------------------|------------|------------------|
| | THE REAL PROPERTY. | CPG | | |
| C _n | Z1 | 1,2 - | _ ≥1 | C _{n+x} |
| P ₀ | G2/Z10 | 3 - 1,2,4 - 3,4 - | ≥1 | c _{n+y} |
| Ğ ₀ → P ₁ → | Z3 G4 | 5 - 1, 2, 4, 6 - 3, 4, 6 - | ≥1 | C _{n+z} |
| G ₁ | Z5 | 5,6 - 7 - | | Silve of |
| P ₂ - | G6 | 1 | 0, 4, 6, 8 | P |
| G ₂ | Z7 | 3, 4, 6, 8 - | = ≥1 | Whom y & |
| P3 - | G8 | 5, 6, 8 - 7, 8 - | İ | - G |
| G ₃ | Z9 | 9 - | - 0 | John St. |
| | | 763 | Т | L/F/9939-1 |

Connection Diagrams





Pin Assignment for LCC



TL/F/9939-3

| Pin Names | Description |
|----------------------------------|-------------------------------------|
| C _n | Carry Input |
| $\overline{G}_0, \overline{G}_2$ | Carry Generate Inputs (Active LOW) |
| G ₁ | Carry Generate Input (Active LOW) |
| G ₃ | Carry Generate Input (Active LOW) |
| $\overline{P0}, \overline{P}_1$ | Carry Propagate Inputs (Active LOW) |
| \overline{P}_2 | Carry Propagate Input (Active LOW) |
| P ₃ | Carry Propagate Input (Active LOW) |
| $C_{n+x}-C_{n+z}$ | Carry Outputs |
| G | Carry Generate Output (Active LOW) |
| P | Carry Propagate Output (Active LOW) |



54AC/74AC191 Up/Down Counters with Preset and Ripple Clock

General Description

The 'AC191 is a reversible modulo 16 binary counter. It features synchronous counting and asynchronous presetting. The preset feature allows the 'AC191 to be used in programmable dividers. The Count Enable input, the Terminal Count output and the Ripple Clock output make possible a variety of methods of implementing multistage counters. In the counting modes, state changes are initiated by the rising edge of the clock.

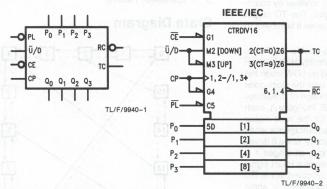
Features

- High speed—133 MHz typical count frequency
- Synchronous counting
- Asynchronous parallel load
- Cascadable
- Outputs source/sink 24 mA

Ordering Code: See Section 5

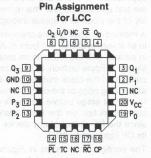
Logic Symbols

Connection Diagrams



| P ₁ —1 | 16 - V _{CC} |
|--------------------|----------------------|
| Q ₁ 2 | 15 -P ₀ |
| $Q_0 - 3$ | 14 — CP |
| CE - 4 | 13 — RC |
| /D = 5 | 12 — TC |
| Q ₂ — 6 | 11 - PL |
| Q ₃ — 7 | 10 -P ₂ |
| 8 — DN | 9 -Pz |

| Pin Names | Description |
|--------------------------------|----------------------------------|
| CE | Count Enable Input |
| CP | Clock Pulse Input |
| P ₀ -P ₃ | Parallel Data Inputs |
| PL | Asynchronous Parallel Load Input |
| Ū/D | Up/Down Count Control Input |
| Q ₀ -Q ₃ | Flip-Flop Outputs |
| RC | Ripple Clock Output |
| TC | Terminal Count Output |



TL/F/9940-4

Functional Description

The 'AC191 is a synchronous up/down counter. The 'AC191 is organized as a 4-bit binary counter. It contains four edge-triggered flip-flops with internal gating and steering logic to provide individual preset, count-up and count-down operations.

Each circuit has an asynchronous parallel load capability permitting the counter to be preset to any desired number. When the Parallel Load (\overline{PL}) input is LOW, information present on the Parallel Load inputs (P_0-P_3) is loaded into the counter and appears on the Q outputs. This operation overides the counting functions, as indicated in the Mode Select Table.

A HIGH signal on the $\overline{\text{CE}}$ input inhibits counting. When $\overline{\text{CE}}$ is LOW, internal state changes are initiated synchronously by the LOW-to-HIGH transition of the clock input. The direction of counting is determined by the $\overline{\text{U}}/\text{D}$ input signal, as indicated in the Mode Select Table. $\overline{\text{CE}}$ and $\overline{\text{U}}/\text{D}$ can be changed with the clock in either state, provided only that the recommended setup and hold times are observed.

Two types of outputs are provided as overflow/underflow indicators. The terminal count (TC) output is normally LOW. It goes HIGH when the circuits reach zero in the count down mode or 15 in the count up mode. The TC output will then remain HIGH until a state change occurs, whether by counting or presetting or until $\overline{\rm U}/{\rm D}$ is changed. The TC output should not be used as a clock signal because it is subject to decoding spikes.

The TC signal is also used internally to enable the Ripple Clock (RC) output. The RC output is normally HIGH. When CE is LOW and TC is HIGH, RC output wil go LOW when the clock next goes LOW and will stay LOW until the clock goes HIGH again. This feature simplifies the design of multistage counters, as indicated in Figures A and B. In Figure A, each RC output is used as the clock input for the next higher stage. This configuration is particularly advantageous when the clock source has a limited drive capability, since it drives only the first stage. To prevent counting in all stages it is only necessary to inhibit the first stage, since a HIGH signal on CE inhibits the RC output pulse, as indicated in the RC Truth Table. A disadvantage of this configuration, in some applications, is the timing skew between state changes in the first and last stages. This represents the cumulative delay of the clock as it ripples through the preceding stages.

A method of causing state changes to occur simultaneously in all stages is shown in Figure B. All clock inputs are driven in parallel and the $\overline{\rm RC}$ outputs propagate the carry/borrow signals in ripple fashion. In this configuration the LOW state duration of the clock must be long enough to allow the negative-going edge of the carry/borrow signal to ripple through to the last stage before the clock goes HIGH. There is no such restriction on the HIGH state duration of the clock, since the $\overline{\rm RC}$ output of any device goes HIGH shortly after its CP input goes HIGH.

The configuration shown in Figure C avoids ripple delays and their associated restrictions. The \overline{CE} input for a given stage is formed by combining the TC signals from all the preceding stages. Note that in order to inhibit counting an enable signal must be included in each carry gate. The simple inhibit scheme of Figures A and B doesn't apply, because the TC output of a given stage is not affected by its own \overline{CE} .

Mode Select Table

| | In | puts | V-14-2833 | Mode |
|----|-----------|------|-----------|----------------------|
| PL | PL CE U/D | | СР | 1 100 1 100 11 11 11 |
| Н | L | L | 5 | Count Up |
| Н | L | н | 5 | Count Down |
| L | X | X | X | Preset (Asyn.) |
| Н | Н | X | X | No Change (Hold) |

RC Truth Table

| | Inputs | | | | | | |
|----|--------------|------------|-----|----|--|--|--|
| PL | CE | TC* | СР | RC | | | |
| Н | essen Fue bu | tren Higmi | o T | | | | |
| Н | Н | X | X | Н | | | |
| Н | X | L | X | Н | | | |
| L | X | X | X | Н | | | |

*TC is generated internally

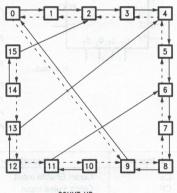
H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

__ = LOW-to-HIGH Transition

State Diagram



COUNT UP

TL/F/9940-5

TL/F/9940-7

Functional Description (Continued)

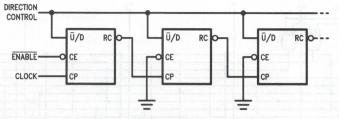


FIGURE A. N-Stage Counter Using Ripple Clock

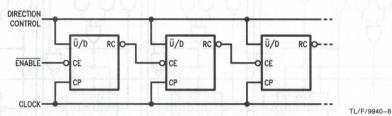


FIGURE B. Synchronous N-Stage Counter Using Ripple Carry/Borrow

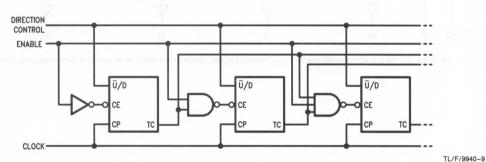
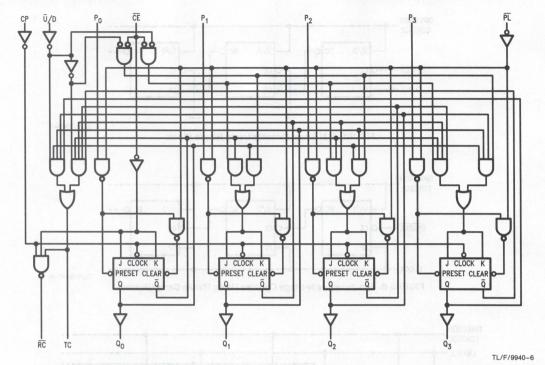


FIGURE C. Synchronous N-Stage Counter with Parallel Gated Carry/Borrow

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

10 ns/V

8 ns/V

Absolute Maximum Rating (Note 1) Recommended Operating

If Military/Aerospace specified devices are required. please contact the National Semiconductor Sales Office/Distributors for availability and specifications

| Office, Distributors for availab | mey and spe | cilications. |
|--|-----------------------------|--------------------------------|
| Supply Voltage (V _{CC}) | 18 + 61 0 19 4 (| 0.5V to + 7.0V |
| DC Input Diode Current (I_{IK}) $V_I = -0.5V$ $V_I = V_{CC} + 0.5V$ | | -20 mA +20 mA |
| DC Input Voltage (V _I) | -0.5V t | 0.5V |
| DC Output Diode Current (I_{OK}) $V_O = -0.5V$ $V_O = V_{CC} + 0.5V$ | | −20 mA +20 mA |
| DC Output Voltage (V _O) | -0.5V to t | 0.5V to V _{CC} + 0.5V |
| DC Output Source or Sink Current (I _O) | | ±50 mA |
| DC V _{CC} or Ground Current per Output Pin (I _{CC} or I _{GND}) | | ± 50 mA |
| Storage Temperature (T _{STG}) | -65 | °C to +150°C |
| Note 1: Absolute maximum ratings are th | ose values bevo | nd which damage |

to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Conditions

| Conditions | | |
|--|------------|-----------------------|
| Supply Voltage (V _{CC}) | | 2.0V to 6.0V |
| Input Voltage (V _I) | | 0V to V _{CC} |
| Output Voltage (V _O) | | 0V to V _{CC} |
| Operating Temperature (T _A) 74AC/ACT 54AC/ACT | -40° | °C to +85°C |
| Junction Temperature (T _{.I}) | Houthous a | GHO |
| CDIP PDIP | | 1100 |
| Input Rise and Fall Time (t _r , t (Note 2) (Typical) (Except Schmitt Inputs) 'AC V _{IN} from 30% to 70% of V | C Devices | |
| V _{CC} @ 3.0V | | 150 ns/V |
| V _{CC} @ 4.5V | | 40 ns/V |
| V _{CC} @ 5.5V | | 25 ns/V |
| Input Rise and Fall Time (t _r , t (Note 2) (Typical) (Except Schmitt Inputs) 'AC V _{IN} from 0.8V to 2.0V, V _{me} from 0.8V to 2.0V | T Devices | |

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

V_{CC} @ 4.5V

V_{CC} @ 5.5V

DC Characteristics for 'AC Family Devices

| | en 0.31 0.1 | | 74 | AC | 54AC | 74AC | e a noise | legg Propag | |
|-----------------|---|---------------------|-------------------------|----------------------|----------------------------------|---------------------------------|------------------|--|--|
| Symbol | Parameter | V _{CC} (V) | T _A = | + 25°C | T _A = -55°C to +125°C | T _A = -40°C to +85°C | Units | Conditions | |
| | 0.00 | | Тур | 0.1 | Guaranteed Lir | nits | | | |
| V _{IH} | Minimum High Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | Volta | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{IL} | Maximum Low Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{OH} | Minimum High Level Output Voltage | 3.0 4.5 5.5 | 2.99 4.49 5.49 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | V | $I_{OUT} = -50 \mu\text{A}$ | |
| | an 8.6 0.5 an 8.6 an 8.6 an 8.6 an | 3.0 4.5 5.5 | | 2.56 3.86 4.86 | 2.4 3.7 4.7 | 2.46 3.76 4.76 | og molla V | $^{*}V_{IN} = V_{IL} \text{ or } V_{IH}$ -12 mA $I_{OH} -24 \text{ mA}$ -24 mA | |
| V _{OL} | Maximum Low Level Output Voltage | 3.0 4.5 5.5 | 0.002 0.001 0.001 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | v _o r | $I_{OUT} = 50 \mu A$ | |
| | 2.5 1.2.5 1.5 1.5 1.5 1.5 1.5 1.5 1.5 1.5 1.5 1 | 3.0 4.5 | 0.01 0.01 a.ar | 0.36 0.36 | 0.50 0.50 | 0.44 0.44 | | $*V_{IN} = V_{IL} \text{ or } V_{IH}$ 12 mA I_{OL} 24 mA | |
| I _{IN} | Maximum Input Leakage Current | 5.5 5.5 | 0 [] | 0.36 ±0.1 | 0.50 ±1.0 | 0.44 ±1.0 | μΑ | $V_{I} = V_{CC}$, GND | |

DC Characteristics for 'AC Family Devices (Continued)

| | | | 74AC T _A = +25°C | | 54AC | 74AC | 1874 Sf1 | Conditions | |
|--------|-------------------------------------|---------------------|--------------------------------|--------|----------------------------------|---------------------------------|-----------|------------------------------|--|
| Symbol | Parameter | V _{CC} (V) | | | T _A = -55°C to +125°C | T _A = -40°C to +85°C | Units | | |
| | | | Тур | | Guaranteed Li | mits | Sept (Ng) | gO shoid tean Ob | |
| IOLD | †Minimum Dynamic | 5.5 | | FOATOA | 50 | 75 | mA | V _{OLD} = 1.65V Max | |
| IOHD | Output Current | 5.5 | | OA UNE | -50 | -75 | mA | V _{OHD} = 3.85V Min | |
| Icc | Maximum Quiescent Supply Current | 5.5 | | 8.0 | 160.0 | 80.0 | μА | $V_{IN} = V_{CC}$ or GND | |

^{*}All outputs loaded; thresholds on input associated with output under test.

AC Electrical Characteristics

| | Parameter | r al) end | | 74AC | | 54 | AC | 74 | AC | a shirtanci Armi | ston |
|------------------|---|------------|-----------------------|--|--------------|------------|---|------------|--|------------------|-------|
| Symbol | | Parameter | V _{CC} * (V) | $T_A = +25^{\circ}C$ $C_L = 50 \text{ pF}$ | | | $T_A = -55^{\circ}C$ to $+125^{\circ}C$ $C_L = 50 pF$ | | $T_A = -40^{\circ}C$ to $+85^{\circ}C$ $C_L = 50 \text{ pF}$ | | Units |
| Vilen Da | | | Min | Тур | Max | Min | Max | Min | Max | | |
| f _{max} | Maximum Count Frequency | 3.3 5.0 | 70 90 | 105 133 | | 55 80 | | 65 85 | | MHz | 2-3 |
| t _{PLH} | Propagation Delay CP to Q _n | 3.3 5.0 | 2.0 1.5 | 8.5 6.0 | 15.0 11.0 | 1.0 1.0 | 16.5 12.0 | 1.5 1.5 | 16.0 12.0 | ns | 2-6 |
| t _{PHL} | Propagation Delay CP to Q _n | 3.3 5.0 | 2.5 1.5 | 8.5 6.0 | 14.5 10.5 | 1.0 1.0 | 16.0 12.0 | 2.0 1.5 | 16.0 11.5 | ns | 2-6 |
| t _{PLH} | Propagation Delay CP to TC | 3.3 5.0 | 3.5 2.5 | 10.5 7.5 | 18.0 12.0 | 1.0 1.0 | 19.5 14.0 | 2.5 1.5 | 20.0 14.0 | ns | 2-6 |
| t _{PHL} | Propagation Delay CP to TC | 3.3 5.0 | 4.0 2.5 | 10.5 7.5 | 17.5 12.5 | 1.0 1.0 | 19.0 14.5 | 3.0 2.0 | 19.0 13.5 | ns | 2-6 |
| t _{PLH} | Propagation Delay CP to RC | 3.3 5.0 | 2.5 2.0 | 7.5 5.5 | 12.0 9.5 | 1.0 1.0 | 14.0 10.5 | 2.0 1.0 | 13.5 10.5 | ns | 2-6 |
| t _{PHL} | Propagation Delay CP to RC | 3.3 5.0 | 2.5 1.5 | 7.0 5.0 | 11.5 8.5 | 1.0 1.0 | 12.5 9.5 | 2.0 1.0 | 12.5 9.5 | ns | 2-6 |
| t _{PLH} | Propagation Delay CE to RC | 3.3 5.0 | 2.5 1.5 | 7.0 5.0 | 12.0 8.5 | 1.0 1.0 | 14.0 10.0 | 1.5 1.0 | 13.5 9.5 | ns | 2-6 |
| t _{PHL} | Propagation Delay CE to RC | 3.3 5.0 | 2.0 1.5 | 6.5 5.0 | 11.0 8.0 | 1.0 1.0 | 12.5 9.5 | 1.5 1.0 | 12.5 9.0 | ns | 2-6 |
| t _{PLH} | Propagation Delay U/D to RC | 3.3 5.0 | 2.5 1.5 | 6.5 5.0 | 12.5 9.0 | 1.0 1.0 | 14.5 11.0 | 2.0 1.0 | 14.5 10.0 | ns | 2-6 |
| t _{PHL} | Propagation Delay \overline{U}/D to \overline{RC} | 3.3 5.0 | 2.5 1.5 | 7.0 5.0 | 12.0 8.5 | 1.0 1.0 | 15.0 11.0 | 2.0 1.0 | 13.5 10.0 | ns | 2-6 |
| t _{PLH} | Propagation Delay U/D to TC | 3.3 5.0 | 2.0 1.5 | 7.0 5.0 | 11.5 8.5 | 1.0 1.0 | 14.0 13.5 | 1.5 1.0 | 13.5 9.5 | ns | 2-6 |
| t _{PHL} | Propagation Delay U/D to TC | 3.3 5.0 | 2.0 1.5 | 6.5 5.0 | 11.0 8.5 | 1.0 1.0 | 13.5 10.0 | 1.5 1.0 | 12.5 9.5 | ns | 2-6 |
| t _{PLH} | Propagation Delay | 3.3 5.0 | 2.5 2.0 | 8.0 5.5 | 13.5 9.5 | 1.0 1.0 | 16.5 11.5 | 2.0 1.0 | 15.5 10.5 | ns | 2-6 |

[†]Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}. I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

AC Electrical Characteristics (Continued)

| Symbol Param | | | | | | | | | | 74AC | | 54 | AC | 74 | AC | 200 | |
|------------------|---|--------------------------|--|------------|--------------|--|--------------|--|--------------|-------|-------------|----------|-----|----|----|-----|--|
| | Parameter | V _{CC} * (V) | T _A = +25°C C _L = 50 pF | | | T _A = -55°C to + 125°C C _L = 50 pF | | T _A = -40°C to +85°C C _L = 50 pF | | Units | Fig. No. | | | | | | |
| | | Sim | a first | 4256 | Min | Тур | Max | Min | Max | Min | Max | \$3 10 h | 1-0 | | | | |
| t _{PHL} | Propagation Delay P _n to Q _n | 3.3 5.0 | 2.5 1.5 | 7.5 5.5 | 13.0 9.5 | 1.0 1.0 | 15.5 10.5 | 1.5 1.0 | 14.5 10.5 | ns | 2-6 | | | | | | |
| t _{PLH} | Propagation Delay | 3.3 5.0 | 3.5 2.0 | 9.5 5.5 | 14.5 9.5 | 1.0 1.0 | 18.0 12.5 | 2.5 1.0 | 17.5 10.5 | ns | 2-6 | | | | | | |
| t _{PHL} | Propagation Delay | 3.3 5.0 | 3.0 2.0 | 8.0 6.0 | 13.5 10.0 | 1.0 1.0 | 15.5 11.5 | 2.0 1.5 | 15.5 11.0 | ns | 2-6 | | | | | | |

^{*}Voltage Range 3.3 is 3.3V ±0.3V Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

| Symbol Paran | emayps | Onoi | 74 | AC | 54AC | 74AC | my 8 d | iloo. |
|------------------|--|-------------------|--------------|------------|--|--|--------|-------------|
| | Parameter | V _{CC} * | | | T _A = -55°C to + 125°C C _L = 50 pF | T _A = -40°C to +85°C C _L = 50 pF | Units | Fig. No. |
| | | | Тур | | Guaranteed Min | imum | - | la jain |
| ts | Setup Time, HIGH or LOW Pn to PL | 3.3 5.0 | 1.0 0.5 | 3.0 2.0 | 4.0 3.0 | 3.0 2.5 | ns | 2-9 |
| t _h | Hold Time, HIGH or LOW P _n to PL | 3.3 5.0 | -1.5 -0.5 | 0.5 1.0 | 1.5 2.0 | 1.0 1.0 | ns | 2-9 |
| ts | Setup Time, LOW CE to CP | 3.3 5.0 | 3.0 1.5 | 6.0 4.0 | 9.0 6.0 | 7.0 4.5 | ns | 2-9 |
| t _h | Hold Time, LOW CE to CP | 3.3 5.0 | -4.0 -2.5 | -0.5 0 | 0 0.5 | -0.5 0 | ns | 2-9 |
| ts | Setup Time, HIGH or LOW U/D to CP | 3.3 5.0 | 4.0 2.5 | 8.0 5.5 | 10.5 7.5 | 9.0 6.5 | ns | 2-9 |
| t _h | Hold Time, HIGH or LOW U/D to CP | 3.3 5.0 | -5.0 -3.0 | 0 0.5 | 0 1.0 | 0 0.5 | ns | 2-9 |
| t _w | PL Pulse Width, LOW | 3.3 5.0 | 2.0 1.0 | 3.5 1.0 | 5.0 5.0 | 4.0 1.0 | ns | 2-6 |
| t _w | CP Pulse Width, LOW | 3.3 5.0 | 2.0 2.0 | 3.5 3.0 | 6.0 6.0 | 4.0 4.0 | ns | 2-6 |
| t _{rec} | Recovery Time PL to CP | 3.3 5.0 | -0.5 -1.0 | 0 | 1.5 1.0 | 0 | ns | 2-9 |

^{*}Voltage Range 3.3 is 3.3V \pm 0.3V Voltage Range 5.0 is 5.0V \pm 0.5V

Capacitance

| Symbol | Parameter | AC/ACT | Units | Conditions | |
|-----------------|----------------------------------|--------|--------|------------------------|--|
| | rai ameter | Тур | Office | | |
| C _{IN} | Input Capacitance | 4.5 | pF | V _{CC} = 5.0\ | |
| C _{PD} | Power Dissipation Capacitance | 75.0 | pF | $V_{CC} = 5.0V$ | |



54AC/74AC240 • 54ACT/74ACT240 Octal Buffer/Line Driver with TRI-STATE® Outputs

General Description

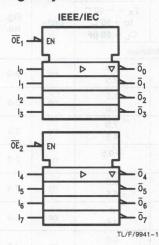
The 'AC/'ACT240 is an octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver which provides improved PC board density.

Features

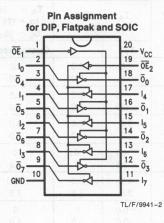
- Inverting TRI-STATE outputs drive bus lines or buffer memory address registers
- Outputs source/sink 24 mA
- 'ACT240 has TTL-compatible inputs

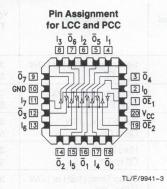
Ordering Code: See Section 5

Logic Symbol



Connection Diagrams





| Pin Names | Description |
|-----------------------------------|--------------------------------|
| ŌĒ₁, ŌĒ₂ | TRI-STATE Output Enable Inputs |
| 10-17 | Inputs |
| $\overline{O}_0 - \overline{O}_7$ | Outputs |

Truth Tables

| Inpu | ıts | Outputs |
|------|------|---------------------------|
| ŌĒ1 | D | (Pins 12, 14, 16, 18) |
| (L) | 0.8L | H 0 a 39 |
| L | Н | VED : L'EL a de enned a |
| Н | X | Value Z0.5 a dic aprofile |

| Inpu | ts | Outputs |
|------|----|------------------------------|
| OE2 | D | Outputs (Pins 3, 5, 7, 9) |
| L | L | Н |
| L | Н | BOSCI BUCHI |
| Н | X | z Z |

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Z = High Impedance

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Supply Voltage (V _{CC}) | ○ 85 + 01 0 0 -0.5V to +7.0V |
|--|---------------------------------|
| DC Input Diode Current (I _{II} $V_I = -0.5V$ $V_I = V_{CC} + 0.5V$ | -20 mA +20 mA |
| DC Input Voltage (V _I) | $-0.5V$ to $V_{CC} + 0.5V$ |
| DC Output Diode Current ($V_O = -0.5V$ $V_O = V_{CC} + 0.5V$ | -20 mA +20 mA |
| DC Output Voltage (V _O) | -0.5 V to to $V_{CC} + 0.5$ V |
| DC Output Source or Sink Current (I _O) | ±50 mA |
| DC V _{CC} or Ground Current per Output Pin (I _{CC} or I _{GI} | |

Storage Temperature (T_{STG}) -65° C to $+150^{\circ}$ C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

Recommended Operating Conditions

| Supply Voltage (V _{CC}) | |
|--|------------------------------|
| 'AC 'ACT | 2.0V to 6.0V 4.5V to 5.5V |
| Input Voltage (V _I) | 0V to V _{CC} |
| | |
| Output Voltage (V _O) | 0V to V _{CC} |
| Operating Temperature (T _A) | |
| 74AC/ACT | -40°C to +85°C |
| 54AC/ACT | -55°C to +125°C |
| Junction Temperature (T,I) | DED Mainten Dynamic |
| CDIP | inemiO tuditiO 175°C |
| PDIP | 1/5 C |
| | Ineodelic Dirigracile |
| Input Rise and Fall Time (t _r , t _f) (Note 2) (Typical) | |
| (Except Schmitt Inputs) 'AC V _{IN} from 30% to 70% of V _{CI} | |
| | 150 ns/V |
| | 40 ns/V |
| V _{CC} @ 5.5V | 25 ns/V |
| | |
| Input Rise and Fall Time (tr, tf) | |
| (Note 2) (Typical) | |
| (Except Schmitt Inputs) 'ACT | |
| V _{IN} from 0.8V to 2.0V, V _{meas} | 3 |
| from 0.8V to 2.0V | |
| V _{CC} @ 4.5V | 10 ns/V |
| V _{CC} @ 5.5V | 8 ns/V |
| to the first of the contract of the first of the contract of t | |

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

| Symbol | 1 30V 40 | 6.0 | 74 | AC | 54AC | 74AC | 200 | 103-30001 |
|--------------------------|--------------------------------------|---------------------|-------------------------|----------------------|----------------------------------|---------------------------------|-----------|--|
| | Parameter | V _{CC} (V) | T _A = +25°C | | T _A = -55°C to +125°C | T _A = -40°C to +85°C | Units | Conditions |
| | $V = N(X_a)$ | 55.0 | Тур | | Guaranteed L | imits | | |
| V _{IH} ks – | Minimum High Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | V | V _{OUT} = 0.1V or V _{CC} - 0.1V |
| V _{IL} Am AS | Maximum Low Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ |
| VOH | Minimum High Level Output Voltage | 3.0 4.5 5.5 | 2.99 4.49 5.49 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | V | $I_{OUT} = -50 \mu\text{A}$ |
| | 0V = 0V Au | 3.0 | | 2.56 | 2.4 | 2.46 | Inemul. | $V_{IN} = V_{IL} \text{ or } V_{IH} - 12 \text{ mA}$ |
| VES - | SOV = IV Am | 4.5 5.5 | | 3.86 4.86 | 3.7 4.7 | 3.76 4.76 | V | I _{OH} -24 mA -24 mA |
| V _{OL} Vaa. | Maximum Low Level Output Voltage | 3.0 4.5 5.5 | 0.002 0.001 0.001 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | Variation | I _{OUT} = 50 μA |
| | OV = MV AU | 3.0 4.5 5.5 | | 0.36 0.36 0.36 | 0.50 0.50 0.50 | 0.44 0.44 0.44 | Ineria | $V_{IN} = V_{IL} \text{ or } V_{IH}$ 12 mA V_{IOL} 10 4 mA 24 mA |
| I _{IN} | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | ±1.0 | μА | $V_{I} = V_{CC}$, GND |

DC Characteristics for 'AC Family Devices (Continued)

| Symbol | | | 74 | AC | 54AC | 74AC | ge gon | georga (engilleri ili elesa e control | |
|--------|--------------------------------------|---------------------|------------------------|-----------|-----------------------------------|---------------------------------|----------|--|--|
| | Parameter | V _{CC} (V) | T _A = +25°C | | T _A = -55°C to + 125°C | T _A = -40°C to +85°C | Units | Conditions | |
| onV of | V0 | | Тур | hadoV luc | Guaranteed Lin | mits | mil Inor | | |
| loz | Maximum TRI-STATE Leakage Current | 5.5 | aredur | ±0.5 | ±10.0 | ±5.0 | μА | V_{I} (OE) = V_{IL} , V_{IH} $V_{I} = V_{CC}$, GND $V_{O} = V_{CC}$, GND | |
| IOLD | †Minimum Dynamic | 5.5 | suusaas | | 50 | 75 | mA | V _{OLD} = 1.65V Max | |
| IOHD | Output Current | 5.5 | | Rice | -50 | -75 | mA | V _{OHD} = 3.85V Min | |
| Icc | Maximum Quiescent Supply Current | 5.5 | | 8.0 | 160.0 | 80.0 | μА | $V_{IN} = V_{CC}$ or GND | |

^{*}All outputs loaded; thresholds on input associated with output under test.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

| | iCT Davices | | 74 | ACT | 54ACT | 74ACT | eliagrio (4) | TOAR to notarago bham. | |
|-----------------|--------------------------------------|------------------------|------------------------|--------------|----------------------------------|---------------------------------|----------------|---|--|
| Symbol | Parameter | V _{CC} (V) | T _A = +25°C | | T _A = -55°C to +125°C | T _A = -40°C to +85°C | Units | Conditions | |
| | | | Тур | tie Deliv | Guaranteed Li | mits | | | |
| V _{IH} | Minimum High Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 2.0 2.0 | 2.0 2.0 | 2.0 2.0 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{IL} | Maximum Low Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 0.8 | 0.8 0.8 | 0.8 0.8 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{OH} | Minimum High Level Output Voltage | 4.5 5.5 | 4.49 5.49 | 4.4 5.4 | 4.4 5.4 | 4.4 5.4 | ٧ | $I_{OUT} = -50 \mu\text{A}$ | |
| | = T.10V | 4.5 5.5 | ellen | 3.86 4.86 | 3.70 4.70 | 3.76 4.76 | V _Q | $V_{IN} = V_{IL} \text{ or } V_{IH}$ -24 mA -24 mA | |
| V _{OL} | Maximum Low Level Output Voltage | 4.5 5.5 | 0.001 0.001 | 0.1 0.1 | 0.1 0.1 | 0.1 0.1 | ٧ | I _{OUT} = 50 μA | |
| | - 00 / 10 · 4 | 4.5 5.5 | | 0.36 0.36 | 0.50 0.50 | 0.44 0.44 | ٧ | $\label{eq:VIN} \begin{array}{ll} *V_{\text{IN}} = V_{\text{IL}} \text{or} V_{\text{IH}} \\ & 24 \text{mA} \\ & 24 \text{mA} \end{array}$ | |
| I _{IN} | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | ±1.0 | μА | $V_{I} = V_{CC}$, GND | |
| loz | Maximum TRI-STATE Leakage Current | 5.5 | | ±0.5 | ±10.0 | ±5.0 | μА | $V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}, GND$ | |
| ICCT | Maximum I _{CC} /Input | 5.5 | 0.6 | | 1.6 | 1.5 | mA | $V_I = V_{CC} - 2.1V$ | |
| lold | †Minimum Dynamic | 5.5 | | | 50 | 75 | mA | V _{OLD} = 1.65V Max | |
| IOHD | Output Current | 5.5 | | | -50 | -75 | mA | V _{OHD} = 3.85V Min | |
| lcc | Maximum Quiescent Supply Current | 5.5 | | 8.0 | 160.0 | 80.0 | μΑ | V _{IN} = V _{CC} or GND | |

^{*}All outputs loaded; thresholds on input associated with output under test.

Note: ICC for 54ACT @ 25°C is identical to 74ACT @ 25°C.

[†]Maximum test duration 2.0 ms, one output loaded at a time.

[†]Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics

| | $V_{CC}^* \qquad \begin{array}{c ccccccccccccccccccccccccccccccccccc$ | AC | 10 8 | | | | | | | | |
|---------------------|---|--|------------|------------|--|-----|--------------|------------------|-------------|-------|-----|
| Symbol | Parameter | $ \begin{array}{c ccccccccccccccccccccccccccccccccccc$ | 85°C | Units | Fig. No. | | | | | | |
| | atuol | uO 1 | Min | Тур | Max | Min | Max | Min | Max | G fed | 00 |
| t _{PLH} | Propagation Delay Data to Output | | | | | | | | 9.0 7.0 | ns | 2-5 |
| t _{PHL} 10 | Propagation Delay Data to Output | 100000000000000000000000000000000000000 | | | THE PARTY OF THE P | | | THE RELEASE HOST | 8.5 6.5 | ns | 2-5 |
| t _{PZH} | Output Enable Time | | | | | | | | 11.0 8.0 | ns | 2-7 |
| t _{PZL} | Output Enable Time | | | | | | | | 11.0 8.5 | ns | 2-8 |
| t _{PHZ} | Output Disable Time | State of the state | | | | | | | 10.5 9.5 | ns | 2-7 |
| t _{PLZ} | Output Disable Time | 3.3 5.0 | 1.5 1.5 | 7.5 6.5 | 10.5 9.0 | 1.0 | 13.5 11.0 | 1.0 1.0 | 11.5 9.5 | ns | 2-8 |

^{*}Voltage Range 3.3 is 3.3V ±0.3V *Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics

| | 10回海一门门一 | 图 图 数 | | 74ACT | | 54 | ACT | 74/ | ACT | - | |
|------------------|-------------------------------------|-------------------|-----|-----------------------|------|------|-------------------------|------|------------------------|----------------|------|
| Symbol | Parameter | V _{CC} * | | C _L = +25° | | to + | -55°C 125°C 50 pF | to + | -40°C 85°C 50 pF | Units | Fig. |
| | | 10 20 8 | Min | Тур | Max | Min | Max | Min | Max | and the second | |
| t _{PLH} | Propagation Delay Data to Output | 5.0 | 1.5 | 6.0 | 8.5 | 1.0 | 9.5 | 1.5 | 9.5 | ns | 2-5 |
| t _{PHL} | Propagation Delay Data to Output | 5.0 | 1.5 | 5.5 | 7.5 | 1.0 | 9.0 | 1.5 | 8.5 | ns | 2-5 |
| t _{PZH} | Output Enable Time | 5.0 | 1.5 | 7.0 | 8.5 | 1.0 | 10.0 | 1.0 | 9.5 | ns | 2-7 |
| t _{PZL} | Output Enable Time | 5.0 | 2.0 | 7.0 | 9.5 | 1.0 | 11.5 | 1.5 | 10.5 | ns | 2-8 |
| t _{PHZ} | Output Disable Time | 5.0 | 2.0 | 8.0 | 9.5 | 1.0 | 11.0 | 2.0 | 10.5 | ns | 2-7 |
| t _{PLZ} | Output Disable Time | 5.0 | 2.5 | 6.5 | 10.0 | 1.0 | 11.5 | 2.0 | 10.5 | ns | 2-8 |

^{*}Voltage Range 5.0 is 5.0V ±0.5V

Capacitance State

| Symbol | Parameter | AC/ACT | Units | Conditions | |
|-----------------|----------------------------------|------------|--------|------------------------|--|
| Symbol | Parameter | Тур | Office | Conditions | |
| C _{IN} | Input Capacitance | 4.5 | pF | $V_{CC} = 5.0V$ | |
| C _{PD} | Power Dissipation Capacitance | ALORE 45.0 | pF | V _{CC} = 5.0\ | |



54AC/74AC241 • 54ACT/74ACT241 Octal Buffer/Line Driver with TRI-STATE® Outputs

General Description

The 'AC/'ACT241 is an octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus-oriented transmitter or receiver which provides improved PC board density.

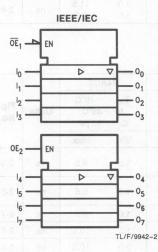
Features

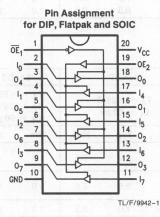
- Non-inverting TRI-STATE outputs drive bus lines or buffer memory address registers
- Outputs source/sink 24 mA
- 'ACT241 has TTL-compatible inputs

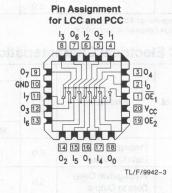
Ordering Code: See Section 5

Logic Symbol

Connection Diagrams







| Pin Names | Description |
|--|--|
| OE ₁ , OE ₂ I ₀ -I ₇ O ₀ -O ₇ | TRI-STATE Output Enable Input TRI-STATE Output Enable Input (Active HIGH) Inputs Outputs |

Truth Tables

| Input | is | Outputs | |
|-----------------|----|-----------------|--------|
| OE ₁ | D | (Pins 12, 14, 1 | 6, 18) |
| TILANDA | L | L | |
| L | Н | Н | lodmy |
| Н | X | Z | |

| O & Inpu | ts | Outputs |
|-----------------|----|-------------------|
| OE ₂ | D | (Pins 3, 5, 7, 9) |
| Н | L | L |
| Н | Н | Н |
| L | X | Z |

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Z = High Impedance

Absolute Maximum Rating (Note 1) Recommended Operating

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Supply Voltage (V _{CC}) | -0.5V to $+7.0V$ |
|--|---------------------------------|
| DC Input Diode Current (I_{IK}) $V_I = -0.5V$ $V_I = V_{CC} + 0.5V$ | - 20 mA + 20 mA |
| DC Input Voltage (V _I) | -0.5 V to $V_{CC} + 0.5$ V |
| DC Output Diode Current (I_{OK}) $V_O = -0.5V$ $V_O = V_{CC} + 0.5V$ | −20 mA +20 mA |
| DC Output Voltage (V _O) | -0.5 V to to $V_{CC} + 0.5$ V |
| DC Output Source or Sink Current (I _O) | ±50 mA |
| DC V _{CC} or Ground Current | |

Storage Temperature (T_{STG}) — 65°C to +150°C **Note 1:** Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

per Output Pin (I_{CC} or I_{GND})

Recommended Operating Conditions

| Odificitions | |
|--|--------------------------------------|
| Supply Voltage (V _{CC}) | |
| 'AC | 2.0V to 6.0V |
| 'ACT | 4.5V to 5.5V |
| Input Voltage (V _I) | 0V to V _{CC} |
| Output Voltage (V _O) | 0V to V _{CC} |
| Operating Temperature (T.) | -40°C to +85°C -55°C to +125°C |
| Junction Temperature (T _J) | |
| CDIP | 175°C |
| PDIP | 140°C |
| (Note 2) (Typical) | icc Maximum Quie Supply Darrent |
| (Except Schmitt Inputs) 'AC Devi | Ces and patrict shipping IIA |
| V _{IN} from 30% to 70% of V _{CC} | Maximum test duration 2.0 m |
| V _{CC} @ 3.0V V _{CC} @ 4.5V | 150 IIS/ V |
| V _{CC} @ 4.5V V _{CC} @ 5.5V | 25 ns/V |
| Input Rise and Fall Time (t _r , t _f) | |
| (Note 2) (Typical) (Except Schmitt Inputs) 'ACT Dev V _{IN} from 0.8V to 2.0V, V _{meas} | vices |
| from 0.8V to 2.0V | |
| V _{CC} @ 4.5V | 10 ns/V |
| V _{CC} @ 5.5V | 8 ns/V |
| Note 2: See individual datasheets for those | davious which differ from the |

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

| | 20 A 10 | 0.0 | 74 | AC | 54AC | 74AC | Span | SA India |
|-----------------------------------|--------------------------------------|---------------------|-------------------------|----------------------|---|---------------------------------|-----------|--|
| Symbol | Parameter | V _{CC} (V) | T _A = +25°C | | T _A = -55°C to +125°C | T _A = -40°C to +85°C | Units | Conditions |
| | $\chi = \nu_0 \lambda_s$ | 25 | Тур | | Guaranteed L | imits | | |
| V _{IH} | Minimum High Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | v l vol n | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ |
| V _{IL} V _{3O 3} | Maximum Low Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ |
| Voh | Minimum High Level Output Voltage | 3.0 4.5 5.5 | 2.99 4.49 5.49 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | tre VLO | $I_{OUT} = -50 \mu\text{A}$ |
| | $V_0 = V_{ab}$ $V_0 = V_0$ | 3.0 | | 2.56 | 0.0 ± | 2.46 | Curent | $*V_{IN} = V_{IL} \text{ or } V_{IH}$ -12 mA |
| | poV = (V Am | 4.5 5.5 | | 3.86 4.86 | 3.7 4.7 | 3.76 4.76 | ٧ | I _{OH} -24 mA -24 mA |
| V _{OL} | Maximum Low Level Output Voltage | 3.0 4.5 5.5 | 0.002 0.001 0.001 | 0.1 0.1 0.1 | 03 0.1 03 0.1 0.1 | 0.1 0.1 0.1 | m Dynair | $I_{OUT} = 50 \mu\text{A}$ |
| 2 | OND TO AH | 3.0 4.5 5.5 | | 0.36 0.36 0.36 | 0.50 0.50 0.50 | 0.44 0.44 0.44 | V | $\label{eq:VIN} \begin{split} *V_{IN} &= V_{IL} or V_{IH} \\ &= 12 mA \\ I_{OL} &= 24 mA \\ &= 24 mA \end{split}$ |
| I _{IN} | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | ±1.0 | μА | $V_I = V_{CC}$, GND |

 \pm 50 mA

DC Characteristics for 'AC Family Devices (Continued)

| | | | 74 | AC | 54AC | 74AC | ak ent | Dieses contests | |
|---------|--------------------------------------|------------------------|-----------------------|----------|-----------------------------------|---------------------------------|----------------------|--|--|
| Symbol | Parameter | V _{CC} (V) | T _A = | + 25°C | T _A = -55°C to + 125°C | T _A = -40°C to +85°C | Units | Conditions | |
| opV at1 | 10 | | Тур | ahaV t | Guaranteed L | imits | _M li Insi | DO Input Blods Co | |
| loz | Maximum TRI-STATE Leakage Current | 5.5 | arecome | ±0.5 | ±10.0 | / O. VB. ±5.0 | μА | V_{I} (OE) = V_{IL} , V_{IH} V_{I} = V_{CC} , GND V_{O} = V_{CC} , GND | |
| IOLD | †Minimum Dynamic | 5.5 | ulerië gan | a) noite | 50 | 75 | mA | V _{OLD} = 1.65V Max | |
| IOHD | Output Current | 5.5 | | SHO | -50 | -75 | mA | V _{OHD} = 3.85V Min | |
| Icc | Maximum Quiescent Supply Current | 5.5 | ind Fall. Tyolcall | 8.0 | 160.0 | 80.0 | μА | V _{IN} = V _{CC} or GND | |

^{*}All outputs loaded; thresholds on input associated with output under test.

DC Characteristics for 'ACT Family Devices

| | asotve@ TOA | | 744 | CT | 54ACT | 74ACT | ehuano Mi | TQA'1 to notherworknern | |
|-----------------|--------------------------------------|------------------------|------------------|--------------|----------------------------------|---------------------------------|--------------------|--|--|
| Symbol | Parameter | V _{CC} (V) | T _A = | + 25°C | T _A = -55°C to +125°C | T _A = -40°C to +85°C | Units | Conditions | |
| V\an 8 | | | Тур | \$ 9 gg | Guaranteed L | imits | | | |
| VIH | Minimum High Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 2.0 2.0 | 2.0 2.0 | 2.0 2.0 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{IL} | Maximum Low Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 0.8 | 0.8 | 0.8 0.8 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| VoH | Minimum High Level Output Voltage | 4.5 5.5 | 4.49 5.49 | 4.4 5.4 | 4.4 5.4 | 4.4 5.4 | ٧ | $I_{OUT} = -50 \mu\text{A}$ | |
| | F-TUOY | 4.5 5.5 | etirai | 3.86 4.86 | 3.70 4.70 | 3.76 4.76 | yea Y gaha | $V_{IN} = V_{IL} \text{ or } V_{IH}$ -24 mA -24 mA | |
| V _{OL} | Maximum Low Level Output Voltage | 4.5 5.5 | 0.001 0.001 | 0.1 0.1 | 0.1 0.1 | 0.1 0.1 | ٧ | $I_{OUT} = 50 \mu A$ | |
| | = TUOV 100 V 10 V | 4.5 5.5 | | 0.36 0.36 | 0.50 0.50 | 0.44 0.44 | A 888 81 MOT | $*V_{IN} = V_{IL} \text{ or } V_{IH}$ I_{OL} 24 mA 24 mA | |
| IIN | Maximum Input Leakage Current | 5.5 | | ±0.1 | 8.5 4.5 ±1.0 5 5 | ±1.0 | μА | $V_{I} = V_{CC}$, GND | |
| loz | Maximum TRI-STATE Leakage Current | 5.5 | | ±0.5 | ±10.0 | ±5.0 | μА | $V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}, GND$ | |
| Ісст | Maximum I _{CC} /Input | 5.5 | 0.6 | | 1.6 38.8 7.5 1.6 38.8 | 1.5 | mA | $V_{\rm I} = V_{\rm CC} - 2.1V$ | |
| lold of | †Minimum Dynamic | 5.5 | | | 50 | 500.0 75 8 16 | mA | V _{OLD} = 1.65V Max | |
| IOHD | Output Current | 5.5 | | | -50 | 1000 -75 | mA | V _{OHD} = 3.85V Min | |
| lcc | Maximum Quiescent Supply Current | 5.5 | | 8.0 | 160.0 | 80.0 | μА | V _{IN} = V _{CC} or GND | |

^{*}All outputs loaded; thresholds on input associated with output under test.

[†]Maximum test duration 2.0 ms, one output loaded at a time.

Note: $I_{\rm IN}$ and $I_{\rm CC}$ @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}. $I_{\rm CC}$ for 54AC @ 25°C is identical to 74AC @ 25°C.

[†]Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

| | | | | 74AC | | 54 | AC | 74 | IAC | | |
|------------------|-------------------------------------|--------------------------|------------|-----------------------|--------------|------------|-------------------------|------------|-------------------------|-------|------|
| Symbol | Parameter | V _{CC} * (V) | | C _L = +25° | | to + | −55°C 125°C 50 pF | to + | -40°C -85°C 50 pF | Units | Fig. |
| | e frant | 1180 | Min | Тур | Max | Min | Max | Min | Max | | 100 |
| t _{PLH} | Propagation Delay Data to Output | 3.3 5.0 | 1.5 1.5 | 6.0 5.0 | 9.0 7.0 | 1.0 1.0 | 12.0 9.5 | 1.5 1.0 | 10.0 7.5 | ns | 2-5 |
| t _{PHL} | Propagation Delay Data to Output | 3.3 5.0 | 1.5 1.5 | 6.0 4.5 | 9.0 7.0 | 1.0 1.0 | 11.5 9.0 | 1.0 1.0 | 10.5 7.5 | ns | 2-5 |
| t _{PZH} | Output Enable Time | 3.3 5.0 | 1.5 1.5 | 6.5 5.5 | 12.5 9.0 | 1.0 | 13.0 10.0 | 1.0 1.0 | 13.0 9.5 | ns | 2-7 |
| t _{PZL} | Output Enable Time | 3.3 5.0 | 1.5 1.5 | 7.0 5.5 | 12.0 9.0 | 1.0 1.0 | 13.0 10.0 | 1.5 1.0 | 13.0 9.5 | ns | 2-8 |
| t _{PHZ} | Output Disable Time | 3.3 5.0 | 2.0 1.5 | 8.0 6.5 | 12.0 10.0 | 1.0 1.0 | 13.0 11.5 | 2.0 1.0 | 12.5 10.5 | ns | 2-7 |
| t _{PLZ} | Output Disable Time | 3.3 5.0 | 1.5 1.5 | 7.0 6.0 | 12.5 10.0 | 1.0 1.0 | 13.0 11.5 | 1.0 1.0 | 13.5 10.5 | ns | 2-8 |

^{*}Voltage Range 3.3 is 3.3V ±3.3V Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics

| | DOMESTICE. | | | 74ACT | - | 54 | ACT | 74/ | ACT | la . | Nº 1 |
|------------------|-------------------------------------|-------------------|-----|-----------------------|------|------|-------------------------|------|------------------------|-------|------|
| Symbol | Parameter | V _{CC} * | | A = +25° CL = 50 p | | to + | -55°C 125°C 50 pF | to + | -40°C 85°C 50 pF | Units | Fig. |
| | | 10 | Min | Тур | Max | Min | Max | Min | Max | la la | 36 |
| t _{PLH} | Propagation Delay Data to Output | 5.0 | 1.5 | 6.5 | 9.0 | 1.0 | 10.0 | 1.5 | 10.0 | ns | 2-5 |
| t _{PHL} | Propagation Delay Data to Output | 5.0 | 1.5 | 7.0 | 9.0 | 1.0 | 10.0 | 1.5 | 10.0 | ns | 2-5 |
| t _{PZH} | Output Enable Time | 5.0 | 1.5 | 6.0 | 9.0 | 1.0 | 11.5 | 1.0 | 10.0 | ns | 2-7 |
| t _{PZL} | Output Enable Time | 5.0 | 1.5 | 7.0 | 10.0 | 1.0 | 12.5 | 1.5 | 11.0 | ns | 2-8 |
| t _{PHZ} | Output Disable Time | 5.0 | 1.5 | 8.0 | 10.5 | 1.0 | 12.5 | 1.5 | 11.5 | ns | 2-7 |
| t _{PLZ} | Output Disable Time | 5.0 | 2.0 | 7.0 | 10.5 | 1.0 | 12.5 | 1.5 | 11.5 | ns | 2-8 |

^{*}Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

| Symbol | Parameter | AC/ACT | Units | Conditions | |
|-----------------|----------------------------------|--------|--------|------------------------|--|
| Symbol | Parameter | Тур | Office | Condition | |
| CIN | Input Capacitance | 4.5 | pF | $V_{CC} = 5.0V$ | |
| C _{PD} | Power Dissipation Capacitance | 45.0 | pF | V _{CC} = 5.0\ | |



54AC/74AC244 • 54ACT/74ACT244 Octal Buffer/Line Driver with TRI-STATE® Outputs

General Description

The 'AC/'ACT244 is an octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus-oriented transmitter/receiver which provides improved PC board density.

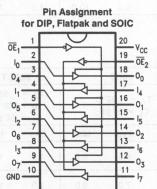
Features

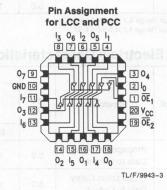
- TRI-STATE outputs drive bus lines or buffer memory address registers
- Outputs source/sink 24 mA
- 'ACT244 has TTL-compatible inputs

Connection Diagrams

Ordering Code: See Section 5

Logic Symbol





Truth Tables

TL/F/9943-2

| Pin Names | Description |
|------------------------------------|--------------------------------|
| $\overline{OE}_1, \overline{OE}_2$ | TRI-STATE Output Enable Inputs |
| 10-17 | Inputs |
| 00-07 | Outputs |

TL/F/9943-1

| Inputs | | Outputs | | | |
|-------------------|---|-----------------------|--|--|--|
| OE ₁ D | | (Pins 12, 14, 16, 18) | | | |
| L | L | retemeted L in | | | |
| Livi | Н | Н | | | |
| Н | X | m monosci man Z | | | |

| lnpu | its | Outputs |
|-----------------|-----|-------------------|
| OE ₂ | D | (Pins 3, 5, 7, 9) |
| L | L | L |
| L | Н | Н |
| Н | X | Z |

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Z = High Impedance

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Supply Voltage (V _{CC}) | -0.5V to $+7.0$ V | ! |
|---|------------------------------------|---|
| DC Input Diode Current (IIK |) alimi i basinma | |
| $V_{I} = -0.5V$ | -20 mA | |
| $V_I = V_{CC} + 0.5V$ | + 20 mA | 1 |
| DC Input Voltage (V _I) | $-0.5V$ to $V_{CC} + 0.5V$ | , |
| DC Output Diode Current (I | OK) | |
| $V_0 = -0.5V$ | -20 mA | 1 |
| $V_O = V_{CC} + 0.5V$ | + 20 mA | 1 |
| DC Output Voltage (V _O) | -0.5V to to V _{CC} + 0.5V | , |
| DC Output Source or Sink Current (I _O) | ±50 mA | 1 |
| DC V _{CC} or Ground Current | | |
| per Output Pin (I _{CC} or I _{GN} | D) ±50 mA | |

Storage Temperature (T_{STG}) Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

Recommended Operating Conditions

| Supply Voltage (V _{CC}) | |
|--|------------------------------------|
| 'AC | 2.0V to 6.0V 4.5V to 5.5V |
| Input Voltage (V _I) | 0V to V _{CC} |
| | |
| Output Voltage (V _O) | OV to VCC |
| Operating Temperature (T _A) 74AC/ACT 54AC/ACT | -40°C to +85°C -55°C to +125°C |
| Junction Temperature (T _{.I}) | |
| CDIP | 175°C |
| PDIP | 140°C |
| Input Rise and Fall Time (t _r , t _f) (Note 2) (Typical) | lgg Maximum Quies Supply Curent |
| (Except Schmitt Inputs) 'AC Dev | |
| V _{IN} from 30% to 70% of V _{CC} | |
| V _{CC} @ 3.0V | |
| | 40 ns/V |
| V _{CC} @ 5.5V | 25 ns/V |
| Input Rise and Fall Time (t _r , t _f) (Note 2) (Typical) | |
| (Except Schmitt Inputs) 'ACT De | evices |
| V _{IN} from 0.8V to 2.0V, V _{meas} | |
| from 0.8V to 2.0V | |
| V _{CC} @ 4.5V | 10 ns/V |
| Vcc @ 5.5V | 8 ns/V |

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

-65°C to +150°C

| | 00//10 | 8.9 | 74AC | | 54AC | 74AC | | BYON IN JUL | |
|---------------------------------|--------------------------------------|------------------------|-------------------------|----------------------|----------------------------------|---------------------------------|----------------------|---|--|
| Symbol Parameter | | V _{CC} (V) | T _A = +25°C | | T _A = -55°C to +125°C | T _A = -40°C to +85°C | Units | Conditions | |
| HIV to IV | $= ^{8l} N_{a}$ | 25.0 | Тур | nec | Guaranteed Li | mits | | | |
| V _{IH} | Minimum High Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | eve I wo. | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| VIL POV TO M Anti AS | Maximum Low Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{OH} | Minimum High Level Output Voltage | 3.0 4.5 5.5 | 2.99 4.49 5.49 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | sə liyan AT&JAT | $I_{OUT} = -50 \mu\text{A}$ | |
| 6, GND 5 = 2.1V 3.65V Max | V = QV $ QV = V $ Am | 3.0 4.5 5.5 | | 2.56 3.86 4.86 | 2.4 3.7 4.7 | 2.46 3.76 4.76 | V Dynamic | $\begin{tabular}{ll} *V_{\text{IN}} &= V_{\text{IL}} \text{ or } V_{\text{IH}} \\ &- 12 \text{ mA} \\ &- 12 \text{ mA} \\ &- 24 \text{ mA} \\ $ | |
| VoL | Maximum Low Level Output Voltage | 3.0 4.5 5.5 | 0.002 0.001 0.001 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | Inor V roceauc | I _{OUT} = 50 μA | |
| | Vivio in | 3.0 4.5 5.5 | | 0.36 0.36 0.36 | 0.50 0.50 0.50 | 0.44 0.44 0.44 | am 05 A | $\begin{tabular}{ll} *V_{\text{IN}} &= V_{\text{IL}} \text{ or } V_{\text{IH}} \\ &= 12 \text{ mA} \\ &= 10 \text{L} \\ &= 24 \text{ mA} \\ &= 24 \text{ mA} \\ \end{tabular}$ | |
| I _{IN} | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | ±1.0 | μΑ | $V_{I} = V_{CC}$, GND | |

DC Characteristics for 'AC Family Devices (Continued)

| | | | 74 | AC | 54AC | 74AC | ga eura sid sida | ti Milliary (Karoag Disase comaci |
|------------------|-------------------------------------|------------------------|--------------------|-----------------------------------|---------------------------------|-------|---------------------|---|
| Symbol Parameter | V _{CC} (V) | T _A = +25°C | | T _A = -55°C to + 125°C | T _A = -40°C to +85°C | Units | Conditions | |
| ∞V of V0 | | | Тур | Typ Guaranteed Limits | | | | DO Input Diode Co |
| loz | Maximum TRI-STATE® Current | 5.5 | oV) stad naomeT | ±0.5 | ±10.0 | ±5.0 | μА | $\begin{aligned} & V_{I} \text{ (OE)} = V_{IL}, V_{IH} \\ & V_{I} = V_{CC}, V_{GND} \\ & V_{O} = V_{CC}, GND \end{aligned}$ |
| IOLD | †Minimum Dynamic | 5.5 | tereviny | | 50 | 75 | mA | V _{OLD} = 1.65V Max |
| IOHD | Output Current | 5.5 | | 9160 | -50 | -75 | mA | V _{OHD} = 3.85V Min |
| Icc | Maximum Quiescent Supply Current | 5.5 | taR bns | 8.0 | 160.0 | 80.0 | μА | $V_{IN} = V_{CC}$ or GND |

^{*}All outputs loaded; thresholds on input associated with output under test.

Note: $I_{|N}$ and $I_{|CC}$ @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V $V_{|CC}$. $I_{|CC}$ for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

| | asolvad TQA (aluga | | 74/ | ACT | 54ACT | 74ACT | balo MITT | AS to note ado briefs | |
|------------------|-------------------------------------|------------------------|-----------------------|--------------|-----------------------------------|---------------------------------|------------|---|--|
| Symbol | Parameter | V _{CC} (V) | T _A = +25° | | T _A = -55°C to + 125°C | T _A = -40°C to +85°C | Units | Conditions | |
| V\en 8 | | | Тур | NO V | Guaranteed Li | mits | | | |
| V _{IH} | Minimum High Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 2.0 2.0 | 2.0 2.0 | 2.0 2.0 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{IL} | Maximum Low Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 0.8 | 0.8 0.8 | 0.8 0.8 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{OH} | Minimum High Level Output Voltage | 4.5 5.5 | 4.49 5.49 | 4.4 5.4 | 4.4 5.4 | 4.4 5.4 | ٧ | $I_{OUT} = -50 \mu\text{A}$ | |
| VIA = 100V - 1.3 | | 4.5 5.5 | niu pas | 3.86 4.86 | 3.70 4.70 | 3.76 4.76 | V | $^*V_{IN} = V_{IL} \text{ or } V_{IH}$ -24 mA -24 mA | |
| V _{OL} | Maximum Low Level Output Voltage | 4.5 5.5 | 0.001 0.001 | 0.1 0.1 | 0.1 0.1 | 0.1 0.1 | V | $I_{OUT} = 50 \mu A$ | |
| V1.0 | - 7d6V | 4.5 5.5 | | 0.36 0.36 | 0.50 0.50 | 0.44 0.44 | spall V | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IN} = V_{IL} \text{ or } V_{IH}$ | |
| I _{IN} | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | ±1.0 | μА | $V_I = V_{CC}$, GND | |
| loz | Maximum TRI-STATE® Current | 5.5 | | ±0.5 | ± 10.0 | ±5.0 | μΑ | $V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}, GND$ | |
| ICCT | Maximum I _{CC} /Input | 5.5 | 0.6 | | 1.6 | 1.5 | mA | $V_I = V_{CC} - 2.1V$ | |
| IOLD | †Minimum Dynamic | 5.5 | | 17.2 | 50 | 75 | mA | V _{OLD} = 1.65V Max | |
| I _{OHD} | Output Current | 5.5 | | 1.0 | -50 | -75 | mA | V _{OHD} = 3.85V Min | |
| Icc | Maximum Quiescent Supply Current | 5.5 | | 8.0 | 160.0 | 80.0 | μА | V _{IN} = V _{CC} or GND | |

^{*}All outputs loaded; thresholds on input associated with output under test.

[†]Maximum test duration 2.0 ms, one output loaded at a time.

[†]Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

| | | | 74AC | | 54 | AC | 74 | AC | | | |
|------------------|-------------------------------------|-------------------|------------|------------|-------------|---|--------------|--|-------------|-------|-------------|
| Symbol Parameter | | V _{CC} * | | | | $T_A = -55^{\circ}C$ to + 125°C $C_L = 50 \text{ pF}$ | | T _A = -40°C to +85°C C _L = 50 pF | | Units | Fig. No. |
| | | | Min | Тур | Max | Min | Max | Min | Max | E le | 50 |
| t _{PLH} | Propagation Delay Data to Output | 3.3 5.0 | 2.0 1.5 | 6.5 5.0 | 9.0 7.0 | 1.0 | 12.5 9.5 | 1.5 1.0 | 10.0 7.5 | ns | 2-5 |
| t _{PHL} | Propagation Delay Data to Output | 3.3 5.0 | 2.0 1.5 | 6.5 5.0 | 9.0 7.0 | 1.0 1.0 | 12.0 9.0 | 2.0 | 10.0 7.5 | ns | 2-5 |
| t _{PZH} | Output Enable Time | 3.3 5.0 | 2.0 1.5 | 6.0 5.0 | 10.5 7.0 | 1.0 1.0 | 11.5 9.0 | 1.5 1.5 | 11.0 8.0 | ns w | 2-7 |
| t _{PZL} | Output Enable Time | 3.3 5.0 | 2.5 1.5 | 7.5 5.5 | 10.0 8.0 | 1.0 1.0 | 13.0 10.5 | 2.0 1.5 | 11.0 8.5 | ns | 2-8 |
| t _{PHZ} | Output Disable Time | 3.3 5.0 | 3.0 2.5 | 7.0 6.5 | 10.0 9.0 | 1.0 1.0 | 12.5 10.5 | 1.5 1.0 | 10.5 9.5 | ns | 2-7 |
| t _{PLZ} | Output Disable Time | 3.3 5.0 | 2.5 2.0 | 7.5 6.5 | 10.5 9.0 | 1.0 1.0 | 13.0 11.0 | 2.5 2.0 | 11.5 9.5 | ns | 2-8 |

^{*}Voltage Range 3.3 is 3.3V ± 0.3 V Voltage Range 5.0 is 5.0V ± 0.5 V

AC Electrical Characteristics

| | purpigna mun | # T# 2 88 8 W | | 74ACT 54ACT 74ACT | | 54ACT | | ACT | M. Carrie | 1000 | |
|------------------|-------------------------------------|---------------|-----|-----------------------|------------------------|-------|--------------------------|------|------------------------|-------|------|
| Symbol | mbol Parameter V _C (V | | | A = +25° CL = 50 p | Charles of Contract of | to + | - 55°C 125°C 50 pF | to + | −40°C 85°C 50 pF | Units | Fig. |
| 00 7 32 7 12 1 | PART PART | Min | Тур | Max | Min | Max | Min | Max | 9 | - | |
| t _{PLH} | Propagation Delay Data to Output | 5.0 | 2.0 | 6.5 | 9.0 | 1.0 | 10.0 | 1.5 | 10.0 | ns | 2-5 |
| t _{PHL} | Propagation Delay Data to Output | 5.0 | 2.0 | 7.0 | 9.0 | 1.0 | 10.0 | 1.5 | 10.0 | ns | 2-5 |
| t _{PZH} | Output Enable Time | 5.0 | 1.5 | 6.0 | 8.5 | 1.0 | 9.5 | 1.0 | 9.5 | ns | 2-7 |
| t _{PZL} | Output Enable Time | 5.0 | 2.0 | 7.0 | 9.5 | 1.0 | 11.0 | 1.5 | 10.5 | ns | 2-8 |
| t _{PHZ} | Output Disable Time | 5.0 | 2.0 | 7.0 | 9.5 | 1.0 | 11.0 | 1.5 | 10.5 | ns | 2-7 |
| t _{PLZ} | Output Disable Time | 5.0 | 2.5 | 7.5 | 10.0 | 1.0 | 11.5 | 2.0 | 10.5 | ns | 2-8 |

^{*}Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

| Parameter | | Units | | |
|---|----------------------------------|---|---|--|
| MOUR CONTRACT | Тур | | Conditions | |
| Input Capacitance | 4.5 | pF | $V_{CC} = 5.0V$ | |
| Power Dissipation Capacitance | 45.0 | pF | $V_{CC} = 5.0V$ | |
| AND | | | a sua c | |
| | Power Dissipation Capacitance | Input Capacitance 4.5 Power Dissipation Capacitance 45.0 | Input Capacitance 4.5 pF Power Dissipation Capacitance 45.0 pF | |



54AC/74AC245 • 54ACT/74ACT245 **Octal Bidirectional Transceiver** with TRI-STATE® Inputs/Outputs

General Description

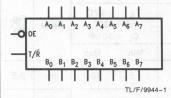
The 'AC/'ACT245 contains eight non-inverting bidirectional buffers with TRI-STATE outputs and is intended for bus-oriented applications. Current sinking capability is 24 mA at both the A and B ports. The Transmit/Receive (T/R) input determines the direction of data flow through the bidirectional transceiver. Transmit (active-HIGH) enables data from A ports to B ports; Receive (active-LOW) enables data from B ports to A ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in a HIGH Z condition.

Features

- Noninverting buffers
- Bidirectional data path
- A and B outputs source/sink 24 mA
- 'ACT245 has TTL-compatible inputs

Ordering Code: See Section 5

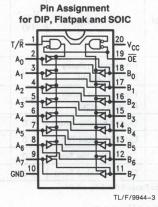
Logic Symbols



| Pin Names | Description |
|--------------------------------|--|
| ŌĒ T/R | Output Enable Input Transmit/Receive Input |
| A ₀ -A ₇ | Side A TRI-STATE |
| 8-9 8 | Inputs or TRI-STATE Outputs |
| B ₀ -B ₇ | Side B TRI-STATE Inputs or TRI-STATE Outputs |

IEEE/IEC G3 3 EN1 (BA) 3 EN2 (AB) 4 TL/F/9944-2

Connection Diagrams

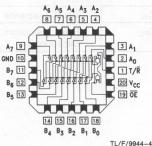


Truth Table

| Inp | outs | Outputs |
|-----|------|---------------------|
| ŌĒ | T/R | Outputs 0.8 = |
| L | L | Bus B Data to Bus A |
| L | Н | Bus A Data to Bus B |
| Н | X | HIGH-Z State |

- H = HIGH Voltage Level
- L = LOW Voltage Level
- X = Immaterial

Pin Assignment for LCC and PCC



Absolute Maximum Rating (Note 1) Recommended Operating

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Cilico, Biotifibatoro for available | mry and opcomoduono. | |
|--|---|--|
| Supply Voltage (V _{CC}) | -0.5V to $+7.0$ V | |
| DC Input Diode Current (I_{IK}) $V_I = -0.5V$ $V_I = V_{CC} + 0.5V$ | -20 mA +20 mA | |
| DC Input Voltage (V _I) | -0.5 V to $V_{CC} + 0.5$ V | |
| DC Output Diode Current (I_{OK}) $V_O = -0.5V$ $V_O = V_{CC} + 0.5V$ | −20 mA +20 mA | |
| DC Output Voltage (V _O) DC Output Source or Sink Current (I _O) | -0.5 V to to V _{CC} + 0.5V ± 50 mA | |
| DC V _{CC} or Ground Current per Output Pin (I _{CC} or I _{GND}) Storage Temperature (T _{STG}) | ±50 mA -65°C to +150°C | |
| -10.29 (1.21.0) | 55 5 10 1 100 0 | |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

Conditions

| Conditions | | |
|--|---------------------------------|-----------------------------------|
| Supply Voltage (V _{CC}) 'AC 'ACT | | 2.0V to 6.0V 4.5V to 5.5V |
| Input Voltage (V _I) | | 0V to V _{CC} |
| Output Voltage (V _O) | | 0V to V _{CC} |
| Operating Temperatur 74AC/ACT 54AC/ACT | e (T _A) | -40°C to +85°C -55°C to +125°C |
| Junction Temperature | (T _J) | |
| CDIP PDIP | | 175°C 140°C |
| V _{IN} from 30% to 70 V _{CC} @ 3.0V V _{CC} @ 4.5V V _{CC} @ 5.5V | uts) 'AC % of V ₀ | Devices CC |
| Input Rise and Fall Tir (Note 2) (Typical) (Except Schmitt Input VIN from 0.8V to 2.0V VCC @ 4.5V VCC @ 5.5V | uts) 'AC | |
| | | |

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

| | 200 x 101 | 0,0 | 74 | AC | 54AC | 74AC | | Britary and the second |
|------------------|--------------------------------------|---------------------|-------------------------|--|----------------------|---------------------------------|--------------|--|
| Symbol | Symbol Parameter | V _{CC} (V) | T _A = | + 25°C T _A = -55°C to + 125°C | | T _A = -40°C to +85°C | Units | Conditions |
| COF VIH | $A = NI_{A*}$ | 3.78 | Тур | 3.70 | Guaranteed Lir | nits | | |
| VIH | Minimum High Level | 3.0 | 1.5 | 2.1 | 2.1 | 2.1 | | $V_{OUT} = 0.1V$ |
| Ац (| Input Voltage | 4.5 5.5 | 2.25 2.75 | 3.15 3.85 | 3.15 3.85 | 3.15 3.85 | ovVLave | or V _{CC} - 0.1V |
| Lorving 24 mA | Maximum Low Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | 0.9 1.35 3.8 1.65 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ |
| V _{OH} | Minimum High Level Output Voltage | 3.0 4.5 5.5 | 2.99 4.49 5.49 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | se Liven | $I_{OUT} = -50 \mu\text{A}$ |
| | = groV Am | 3.0 4.5 | | 2.56 3.86 | 2.4 3.7 | 2.46 3.76 | Oynamic v | $\label{eq:VIN} \begin{split} *V_{\text{IN}} &= V_{\text{IL}} \text{or} V_{\text{IH}} \\ &- 12 \text{mA} \\ I_{\text{OH}} &- 24 \text{mA} \end{split}$ |
| | SV-94V | 5.5 | | 4.86 | 4.7 | 4.76 | nansoiC | -24 mA |
| NOT NO | Maximum Low Level Output Voltage | 3.0 4.5 5.5 | 0.002 0.001 0.001 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | V | $I_{OUT} = 50 \mu\text{A}$ |
| | DV = 0V | 3.0 4.5 5.5 | | 0.36 0.36 0.36 | 0.50 0.50 0.50 | 0.44 0.44 0.44 | V | $V_{IN} = V_{IL} \text{ or } V_{IH}$ 12 mA V_{IOL} 24 mA 24 mA |
| I _{IN} | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | ± 1.0 | μА | $V_I = V_{CC}$, GND |

DC Characteristics for 'AC Family Devices (Continued) and the state of
| Symbol Parameter | | 74 | AC | 54AC | 74AC | qa oos | eth sectors seems | |
|------------------|-------------------------------------|------------------------|-----------------|----------------------|---------------------------------|--------------------|-------------------|--|
| | V _{CC} (V) | T _A = +25°C | | T _A = | T _A = -40°C to +85°C | Units | Conditions | |
| 33 V of VC | | | Тур | gatioV luc | Guaranteed Lin | | uO ebalO lugal DO | |
| IOLD | †Minimum Dynamic | 5.5 | (5V) e g | Nov rous | 50 | 75 | mA | V _{OLD} = 1.65V Max |
| IOHD | Output Current | 5.5 | TUETOCTE | A DINIGRAL Oranga | -50 | of V3.0 -75 | mA | V _{OHD} = 3.85V Min |
| lcc | Maximum Quiescent Supply Current | 5.5 | enuterace | 8.0 | 160.0 | 80.0 | μА | $V_{IN} = V_{CC}$ or GND |
| lozt | Maximum I/O Leakage Current | 5.5 | niT (le For | ±0.6 | va 0 + 50V ±11.0 | of of V8.0 ±6.0 | μА | $V_{I}(OE) = V_{IL}, V_{IH}$ $V_{I} = V_{CC}, GND$ $V_{O} = V_{CC}, GND$ |

^{*}All outputs loaded; thresholds on input associated with output under test.

DC Characteristics for 'ACT Family Devices

| | seaweG TÖA! (atawa | Piedil) | $\begin{array}{c c} & 74ACT \\ \hline V_{CC} \\ (V) & T_A = +25^{\circ}C \end{array}$ | | 54ACT | 74ACT | Units | Conditions | |
|------------------|-------------------------------------|------------|---|--------------|----------------------------------|---------------------------------|-------|---|--|
| Symbol | Parameter | | | | T _A = -55°C to +125°C | T _A = -40°C to +85°C | | | |
| V Ven | | | Тур | 5V | Guaranteed L | imits | | | |
| V _{IH} | Minimum High Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 2.0 2.0 | 2.0 2.0 | 2.0 2.0 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{IL} | Maximum Low Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 0.8 | 0.8 | 0.8 0.8 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{OH} | Minimum High Level Output Voltage | 4.5 5.5 | 4.49 5.49 | 4.4 5.4 | 4.4 5.4 | 4.4 5.4 | V | $I_{OUT} = -50 \mu\text{A}$ | |
| | FE-THOV 5.2 | 4.5 5.5 | k l bee | 3.86 4.86 | 3.70 4.70 | 3.76 4.76 | V | * V _{IN} = V _{IL} or V _{IH} -24 mA -24 mA | |
| V _{OL} | Maximum Low Level Output Voltage | 4.5 5.5 | 0.001 0.001 | 0.1 0.1 | 0.1 0.1 | 0.1 0.1 | V | $I_{OUT} = 50 \mu A$ | |
| | 7 TUOV 9.0 - 30 V 50 t 50 t 68 t | 4.5 5.5 | | 0.36 0.36 | 0.50 0.50 | 0.44 0.44 | vol. | $^*V_{IN} = V_{IL} \text{ or } V_{IH}$ $^{1}V_{IN} = V_{IL} \text{ or } V_{IH}$ $^{24} \text{ mA}$ $^{24} \text{ mA}$ | |
| IIN | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | ±1.0 | μΑ | $V_I = V_{CC}$, GND | |
| ГССТ | Maximum I _{CC} /Input | 5.5 | 0.6 | 3.3 | 1.6 | 1.5 | mA | $V_I = V_{CC} - 2.1V$ | |
| lold | †Minimum Dynamic | 5.5 | | A.S. | 50 | 75 | mA | V _{OLD} = 1.65V Max | |
| IOHD | Output Current | 5.5 | | 15 | -50 | -75 | mA | V _{OHD} = 3.85V Min | |
| Icc | Maximum Quiescent Supply Current | 5.5 | | 8.0 | 160.0 | 80.0 seve | μА | V _{IN} = V _{CC} or GND | |
| lozt HIV 30.3 | Maximum I/O Leakage Current | 5.5 | | ±0.6 | ±11.0 | ±6.0 | μΑ | V_{I} (OE) = V_{IL} , V_{IH} V_{I} = V_{CC} , GND V_{O} = V_{CC} , GND | |

^{*}All outputs loaded; thresholds on input associated with output under test.

[†]Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

[†]Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

| | | | | 74AC | | 54 | AC | 74 | AC | | |
|------------------|--|-----------------------|--|------------|-------------|---|--------------|--|--------------|--------|-------------|
| Symbol Paramet | Parameter | V _{CC} * (V) | T _A = +25°C C _L = 50 pF | | | $T_A = -55^{\circ}C$ to + 125°C $C_L = 50 pF$ | | $T_A = -40^{\circ}C$ to $+85^{\circ}C$ $C_L = 50 pF$ | | Units | Fig. No. |
| | | 2:10 | Min | Тур | Max | Min | Max | Min | Max | essess | Lin |
| t _{PLH} | Propagation Delay An to Bn or Bn to An | 3.3 5.0 | 1.5 1.5 | 5.0 3.5 | 8.5 6.5 | 1.0 1.0 | 11.5 8.5 | 1.0 1.0 | 9.0 7.0 | ns | 2-5 |
| t _{PHL} | Propagation Delay An to Bn or Bn to An | 3.3 5.0 | 1.5 1.5 | 5.0 3.5 | 8.5 6.0 | 1.0 1.0 | 10.0 7.5 | 1.0 1.0 | 9.0 7.0 | ns | 2-5 |
| t _{PZH} | Output Enable Time | 3.3 5.0 | 2.5 | 7.0 5.0 | 11.5 8.5 | 1.0 1.0 | 13.5 10.0 | 2.0 1.0 | 12.5 9.0 | ns | 2-7 |
| t _{PZL} | Output Enable Time | 3.3 5.0 | 2.5 1.5 | 7.5 5.5 | 12.0 9.0 | 1.0 1.0 | 14.5 10.5 | 2.0 1.0 | 13.5 9.5 | ns | 2-8 |
| t _{PHZ} | Output Disable Time | 3.3 5.0 | 2.0 1.5 | 6.5 5.5 | 12.0 9.0 | 1.0 1.0 | 13.5 10.5 | 1.0 1.0 | 12.5 10.0 | ns | 2-7 |
| t _{PLZ} | Output Disable Time | 3.3 5.0 | 2.0 1.5 | 7.0 5.5 | 11.5 9.0 | 1.0 1.0 | 14.0 10.5 | 1.5 1.0 | 13.0 10.0 | ns | 2-8 |

^{*}Voltage Range 3.3 is 3.3V \pm 0.3V Voltage Range 5.0 is 5.0V \pm 0.5V

AC Electrical Characteristics

| | 20,100 | | | 74ACT | | 54ACT | | 74ACT | | | in the same |
|------------------|--|-------------------|--|-------|------|---|------|--|------|-------|-------------|
| Symbol Paramete | Parameter | V _{CC} * | T _A = +25°C C _L = 50 pF | | | T _A = -55°C to +125°C C _L = 50 pF | | $T_A = -40^{\circ}C$ $to +85^{\circ}C$ $C_L = 50 pF$ | | Units | Fig. |
| | Grad S) | C M | Min | Тур | Max | Min | Max | Min | Max | 1 | |
| t _{PLH} | Propagation Delay An to Bn or Bn to An | 5.0 | 1.5 | 4.0 | 7.5 | 1.0 | 9.0 | 1.5 | 8.0 | ns | 2-5 |
| t _{PHL} | Propagation Delay An to Bn or Bn to An | 5.0 | 1.5 | 4.0 | 8.0 | 1.0 | 10.0 | 1.0 | 9.0 | ns | 2-5 |
| t _{PZH} | Output Enable Time | 5.0 | 1.5 | 5.0 | 10.0 | 1.0 | 12.0 | 1.5 | 11.0 | ns | 2-7 |
| t _{PZL} | Output Enable Time | 5.0 | 1.5 | 5.5 | 10.0 | 1.0 | 13.0 | 1.5 | 12.0 | ns | 2-8 |
| t _{PHZ} | Output Disable Time | 5.0 | 1.5 | 5.5 | 10.0 | 1.0 | 12.0 | 1.0 | 11.0 | ns | 2-7 |
| t _{PLZ} | Output Disable Time | 5.0 | 2.0 | 5.0 | 10.0 | 1.0 | 12.0 | 1.5 | 11.0 | ns | 2-8 |

^{*}Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

| Symbol | Parameter | AC/ACT | Units | Conditions |
|------------------|----------------------------------|--------|--------|------------------------|
| | rarameter | Тур | Office | Conditions |
| CIN | Input Capacitance | 4.5 | pF | $V_{CC} = 5.0V$ |
| C _{I/O} | Input/Output Capacitance | 15.0 | pF | V _{CC} = 5.0V |
| C _{PD} | Power Dissipation Capacitance | 45.0 | pF | V _{CC} = 5.0V |



54AC/74AC251 • 54ACT/74ACT251 8-Input Multiplexer with TRI-STATE® Output

General Description

The 'AC/'ACT251 is a high-speed 8-input digital multiplexer. It provides, in one package, the ability to select one bit of data from up to eight sources. It can be used as universal function generator to generate any logic function of four variables. Both true and complementary outputs are provid-

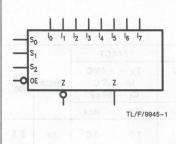
Features

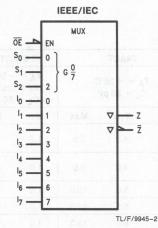
- Multifunctional capability
- On-chip select logic decoding
- Inverting and noninverting TRI-STATE outputs
- Outputs source/sink 24 mA
- 'ACT251 has TTL-compatible inputs

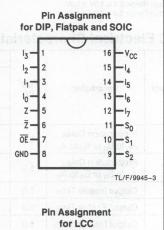
Ordering Code: See Section 5

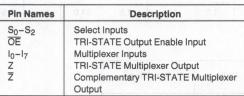
Logic Symbols

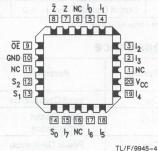
Connection Diagrams











Functional Description

This device is a logical implementation of a single-pole, 8-position switch with the switch position controlled by the state of three Select inputs, S_0 , S_1 , S_2 . Both true and complementary outputs are provided. The Output Enable input (\overline{OE}) is active LOW. When it is activated, the logic function provided at the output is:

$$Z = \overline{OE} \bullet (I_0 \bullet \overline{S}_0 \bullet \overline{S}_1 \bullet \overline{S}_2 + I_1 \bullet S_0 \bullet \overline{S}_1 \bullet \overline{S}_2 + I_2 \bullet \overline{S}_0 \bullet S_1 \bullet \overline{S}_2 + I_3 \bullet S_0 \bullet S_1 \bullet \overline{S}_2 + I_4 \bullet \overline{S}_0 \bullet \overline{S}_1 \bullet S_2 + I_5 \bullet S_0 \bullet \overline{S}_1 \bullet S_2 + I_6 \bullet \overline{S}_0 \bullet S_1 \bullet S_2 + I_7 \bullet S_0 \bullet S_1 \bullet S_2)$$

When the Output Enable is HIGH, both outputs are in the high impedance (High Z) state. This feature allows multiplexer expansion by tying the outputs of up to 128 devices together. When the outputs of the TRI-STATE devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. The Output Enable signals should be designed to ensure there is no overlap in the active-LOW portion of the enable voltages.

Truth Table

| dag ta | Inputs | | | | | | | | |
|--------|----------------|----------------|----------------|----------------|----|--|--|--|--|
| ŌĒ | S ₂ | S ₁ | S ₀ | Z | Z | | | | |
| H | X | X | X | Z | Z | | | | |
| L | L | L | (Sil) Filozo | Īo | lo | | | | |
| L | L | L | H | Ī ₁ | 14 | | | | |
| L | L | Н | L | Ī ₂ | 12 | | | | |
| _ L 33 | A OLF G'A' | Н | н | Ī ₃ | la | | | | |
| L | Н | L | (20) pleaning | Ī ₄ | 14 | | | | |
| L | Н | L | Н | Ī ₅ | 15 | | | | |
| L | Н | Н | L | Ī ₆ | 16 | | | | |
| L | Н | Н | H | Ī ₇ | 17 | | | | |

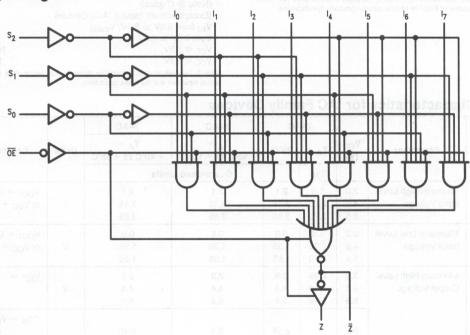
H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Z = High Impedance

Logic Diagram



TL/F/9945-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Supply Voltage (V _{CC}) | -0.5V to $+7.0V$ |
|---|---------------------------------|
| DC Input Diode Current (I _{IK}) | |
| $V_1 = -0.5V$ | -20 mA |
| $V_I = V_{CC} + 0.5V$ | + 20 mA |
| DC Input Voltage (V _I) | $-0.5V$ to $V_{CC} + 0.5V$ |
| DC Output Diode Current (IOK) | |
| $V_0 = -0.5V$ | -20 mA |
| $V_O = V_{CC} + 0.5V$ | + 20 mA |
| DC Output Voltage (V _O) | -0.5 V to to $V_{CC} + 0.5$ V |
| DC Output Source | |
| or Sink Current (IO) | ±50 mA |
| DC V _{CC} or Ground Current | |
| per Output Pin (I _{CC} or I _{GND}) | ±50 mA |
| Storage Temperature (T _{STG}) | -65°C to +150°C |
| Mate de Abantuta manimum rationa ara th | and values howard which damage |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

Recommended Operating Conditions

typical input rise and fall times noted here.

| Supply Voltage (V _{CC}) | |
|---|--------------------------|
| 'AC | 2.0V to 6.0V |
| 'ACT | 4.5V to 5.5V |
| Input Voltage (V _I) | 0V to V _{CC} |
| Output Voltage (V _O) | 01/101/ |
| Operating Temperature (T _A) | |
| 74AC/ACT | -40°C to +85°C |
| 54AC/ACT | -55°C to +125°C |
| lunction Temperature (T.) | |
| CDIP | 175°C |
| PDIP STATE OF THE | 140%; |
| Input Rise and Fall Time (t _r , t _f) | |
| (Except Schmitt Inputs) 'AC Devices V _{IN} from 30% to 70% of V _{CC} | |
| V _{CC} @ 3.0V | 150 ns/V |
| V _{CC} @ 4.5V | 40 ns/V |
| V _{CC} @ 5.5V | 25 ns/V |
| Input Rise and Fall Time (t _r , t _f) (Note 2) (Typical) | |
| (Except Schmitt Inputs) 'ACT Devices | |
| V _{IN} from 0.8V to 2.0V, V _{meas} | |
| from 0.8V to 2.0V | |
| V _{CC} @ 4.5V | 10 ns/V |
| V _{CC} @ 5.5V | 8 ns/V |
| Note 2: See individual datasheets for those device | es which differ from the |

DC Characteristics for 'AC Family Devices

| | | | 74 | AC | 54AC | 74AC | | |
|-----------------|--|------------------------|------------------------|------|----------------------------------|---------------------------------|-------------|---|
| Symbol | Symbol Parameter | V _{CC} (V) | T _A = +25°C | | T _A = -55°C to +125°C | T _A = -40°C to +85°C | Units | Conditions |
| | | | Тур | | Guaranteed Li | imits | | |
| V _{IH} | Minimum High Level | 3.0 | 1.5 | 2.1 | 2.1 | 2.1 | | $V_{OUT} = 0.1V$ |
| | Input Voltage | 4.5 | 2.25 | 3.15 | 3.15 | 3.15 | V | or V _{CC} - 0.1V |
| | and agent and agent of the same and a same a | 5.5 | 2.75 | 3.85 | 3.85 | 3.85 | | |
| VIL | Maximum Low Level | 3.0 | 1.5 | 0.9 | 0.9 | 0.9 | | $V_{OUT} = 0.1V$ |
| | Input Voltage | 4.5 | 2.25 | 1.35 | 1.35 | 1.35 | V | or V _{CC} - 0.1V |
| | | 5.5 | 2.75 | 1.65 | 1.65 | 1.65 | | |
| V _{OH} | Minimum High Level | 3.0 | 2.99 | 2.9 | 2.9 | 2.9 | | $I_{OUT} = -50 \mu$ A |
| | Output Voltage | 4.5 | 4.49 | 4.4 | 4.4 | 4.4 | V | |
| | | 5.5 | 5.49 | 5.4 | 5.4 | 5.4 | | |
| | | | | | | | | $*V_{IN} = V_{IL} \text{ or } V_{I}$ |
| | | 3.0 | 7 | 2.56 | 2.4 | 2.46 | | -12 m |
| | | 4.5 | | 3.86 | 3.7 | 3.76 | V | I _{OH} -24 m |
| | Laidt nodepugato efamiliae d | 5.5 | lea muoda i | 4.86 | 4.7 | 4.76 | the the dat | −24 m |
| VOL | Maximum Low Level | 3.0 | 0.002 | 0.1 | 0.1 | 0.1 | | $I_{OUT} = 50 \mu A$ |
| | Output Voltage | 4.5 | 0.001 | 0.1 | 0.1 | 0.1 | V | |
| | | 5.5 | 0.001 | 0.1 | 0.1 | 0.1 | | |
| | | | | | | | | *V _{IN} = V _{IL} or V |
| | | 3.0 | | 0.36 | 0.50 | 0.44 | | 12 m |
| | | 4.5 | | 0.36 | 0.50 | 0.44 | V | I _{OL} 24 m |
| | | 5.5 | | 0.36 | 0.50 | 0.44 | | 24 m |
| I _{IN} | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | ±1.0 | μА | $V_{I} = V_{CC}$, GND |

DC Characteristics for 'AC Family Devices (Continued) (Seite Desired Report of Continued)

| | 7 SAC | | 74 | IAC | 54AC | 74AC | | | |
|--------|-------------------------------------|------------------------|------------------------|------|-----------------------------------|---------------------------------|-------|---|--|
| Symbol | Parameter | V _{CC} (V) | T _A = +25°C | | T _A = -55°C to + 125°C | T _A = -40°C to +85°C | Units | Conditions | |
| | O ₂ = 80 pF | 40 | Тур | pul | Guaranteed L | imits | | | |
| loz | Maximum TRI-STATE® Current | 5.5 | | ±0.5 | ±10.0 | ±5.0 | μΑ | $\begin{aligned} & V_{I}\left(\text{OE}\right) = V_{IL}, V_{IH} \\ & V_{I} = V_{CC}, V_{GND} \\ & V_{O} = V_{CC}, \text{GND} \end{aligned}$ | |
| IOLD | †Minimum Dynamic | 5.5 | | 0.7 | 50 | 75 | mA | V _{OLD} = 1.65V Max | |
| IOHD | Output Current | 5.5 | | 2 | -50 | -75 | mA | V _{OHD} = 3.85V Min | |
| Icc | Maximum Quiescent Supply Current | 5.5 | | 8.0 | 160.0 | 80.0 | μА | V _{IN} = V _{CC} or GND | |

^{*}All outputs loaded; thresholds on input associated with output under test.

ICC for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

| | en 0.87 c.f | 0.1 | | | 54ACT | 74ACT | Units | Conditions | |
|-----------------|--------------------------------------|------------------------|--------------|--------------|----------------------------------|---------------------------------|------------------|--|--|
| Symbol | Parameter | V _{CC} (V) | | | T _A = -55°C to +125°C | T _A = -40°C to +85°C | | | |
| | | | Тур | | Guaranteed L | imits | V6.0± V8 | c at the synothercation | |
| V _{IH} | Minimum High Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 2.0 2.0 | 2.0 2.0 | 2.0 2.0 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{IL} | Maximum Low Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 0.8 0.8 | 0.8 0.8 | 0.8 0.8 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{OH} | Minimum High Level Output Voltage | 4.5 5.5 | 4.49 5.49 | 4.4 5.4 | 5.4 | 4.4 5.4 | V | $I_{OUT} = -50 \mu\text{A}$ | |
| | xay nist | 4.5 5.5 | | 3.86 4.86 | 3.70 4.70 | 3.76 4.76 | ale V no | * V _{IN} = V _{IL} or V _{IH} -24 mA -24 mA | |
| V _{OL} | Maximum Low Level Output Voltage | 4.5 5.5 | 0.001 | 0.1 | 0.1 a.ar 0.1 | 0.1 0.1a | rsie V no | I _{OUT} = 50 μA | |
| | 2.0 13.0 ns | 4.5 5.5 | | 0.36 0.36 | 0.50 | 0.44 0.44 | on Doler Z V | $*V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IN} = V_{IL} \text{ or } V_{IH}$ | |
| IIN | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | ± 1.0 | μА | V _I = V _{CC} , GND | |
| loz | Maximum TRI-STATE® Current | 5.5 | | ±0.5 | 8.8 0.8 ±10.0 | ±5.0 | μА | $V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}, GND$ | |
| Ісст | Maximum I _{CC} /Input | 5.5 | 0.6 | | 1.6 | 1,5 | mA | $V_I = V_{CC} - 2.1V$ | |
| IOLD | †Minimum Dynamic | 5.5 | | | 50 | 75 | mA | V _{OLD} = 1.65V Max | |
| IOHD | Output Current | 5.5 | | | -50 | -75 | mA | V _{OHD} = 3.85V Min | |
| Icc | Maximum Quiescent Supply Current | 5.5 | | 8.0 | 160.0 | 80.0 | μΑ | V _{IN} = V _{CC} or GND | |

^{*}All outputs loaded; thresholds on input associated with output under test.

[†]Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC} .

[†]Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics and applied yilling 3 OA not applied as a second 20

| | | DAM | 74AC | | | 54AC | | 74AC | | | |
|------------------|--|-------------------|------------|-----------------------|--------------|------------|-------------------------|------------|------------------------|-------|------|
| Symbol | Parameter | V _{CC} * | | C _L = +25° | | to + | -55°C 125°C 50 pF | to + | -40°C 85°C 50 pF | Units | Fig. |
| | | | Min | Тур | Max | Min | Max | Min | Max | -54 | |
| t _{PLH} | Propagation Delay S_n to Z or \overline{Z} | 3.3 5.0 | 1.5 1.5 | 11.5 8.5 | 17.5 12.5 | 1.0 1.0 | 21.0 15.5 | 1.5 1.5 | 19.0 13.5 | ns | 2-6 |
| t _{PHL} | Propagation Delay S_n to Z or \overline{Z} | 3.3 5.0 | 1.5 1.5 | 11.0 8.0 | 17.5 12.5 | 1.0 1.0 | 21.0 15.5 | 1.5 1.5 | 19.0 13.5 | ns | 2-6 |
| t _{PLH} | Propagation Delay I_n to Z or \overline{Z} | 3.3 5.0 | 1.5 1.5 | 10.0 7.0 | 14.0 10.0 | 1.0 1.0 | 17.0 12.0 | 1.5 1.5 | 15.5 11.0 | ns | 2-5 |
| t _{PHL} | Propagation Delay I_n to Z or \overline{Z} | 3.3 5.0 | 1.5 1.5 | 9.0 6.5 | 14.0 10.0 | 1.0 | 16.5 12.0 | 1.5 | 15.5 11.0 | ns | 2-5 |
| t _{PZH} | Output Enable Time | 3.3 5.0 | 1.5 1.5 | 7.5 5.5 | 11.0 8.0 | 1.0 | 13.0 10.0 | 1.5 1.5 | 12.0 9.0 | ns | 2-7 |
| t _{PZL} | Output Enable Time | 3.3 5.0 | 1.5 1.5 | 7.5 5.5 | 11.0 8.0 | 1.0 1.0 | 13.0 10.0 | 1.5 1.5 | 12.0 9.0 | ns | 2-8 |
| t _{PHZ} | Output Disable Time OE to Z or Z | 3.3 5.0 | 1.5 1.5 | 8.5 7.0 | 11.5 9.5 | 3.5 2.5 | 14.0 11.0 | 1.5 1.5 | 13.0 10.0 | ns | 2-7 |
| tpLZ | Output Disable Time | 3.3 5.0 | 1.5 1.5 | 7.0 5.5 | 11.0 8.0 | 4.0 3.0 | 13.0 10.0 | 1.5 1.5 | 12.0 8.5 | ns | 2-8 |

^{*}Voltage Range 3.3 is 3.3V ± 0.3 V Voltage Range 5.0 is 5.0V ± 0.5 V

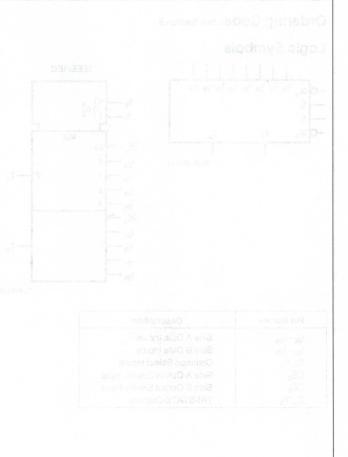
AC Electrical Characteristics

| | = 100° V | 8.0 | | 74ACT | | 54/ | ACT | 74 | ACT | leV svent | |
|------------------|--|-------------------|--|-------|------|---|------|--|------|-----------|------|
| Symbol | Parameter | V _{CC} * | $	extstyle{T_A = +25^{\circ}C} \ 	extstyle{C_L = 50 pF}$ | | | $T_A = -55^{\circ}C$ to + 125°C $C_L = 50 \text{ pF}$ | | $T_A = -40^{\circ}C$ to $+85^{\circ}C$ $C_L = 50 \text{ pF}$ | | Units | Fig. |
| HIV 10 J | V - v.V" | 0.7 | Min | Тур | Max | Min | Max | Min | Max | | |
| t _{PLH} | Propagation Delay S_n to Z or \overline{Z} | 5.0 | 2.5 | 7.0 | 15.5 | 1.0 | 18.5 | 2.0 | 17.0 | ns | 2-6 |
| t _{PHL} | Propagation Delay S_n to Z or \overline{Z} | 5.0 | 2.5 | 7.5 | 16.5 | 1.0 | 19.5 | 2.5 | 18.5 | ns | 2-6 |
| t _{PLH} | Propagation Delay I_n to Z or \overline{Z} | 5.0 | 2.5 | 5.5 | 12.0 | 1.0 | 14.0 | 2.0 | 13.0 | ns | 2-5 |
| t _{PHL} | Propagation Delay I_n to Z or \overline{Z} | 5.0 | 2.5 | 6.5 | 12.5 | 1.0 | 15.0 | 2.5 | 14.0 | ns | 2-5 |
| tpzH | Output Enable Time OE to Z or Z | 5.0 | 1.5 | 5.0 | 8.5 | 1.0 | 10.0 | 1.5 | 9.0 | ns | 2-7 |
| t _{PZL} | Output Enable Time | 5.0 | 1.5 | 4.5 | 8.5 | 1.0 | 10.0 | 1.5 | 9.5 | ns | 2-8 |
| t _{PHZ} | Output Disable Time | 5.0 | 2.0 | 6.0 | 12.0 | 1.0 | 13.5 | 2.0 | 13.0 | ns | 2-7 |
| t _{PLZ} | Output Disable Time | 5.0 | 3.0 | 4.5 | 8.5 | 1.0 | 9.5 | 3.0 | 9.0 | ns | 2-8 |

^{*}Voltage Range 5.0 is 5.0V $\pm 0.5 \text{V}$

| Capacitance |
|-------------|
|-------------|

| pacitano | e | | | | |
|-----------------|----------------------------------|---------------|-------|-----------------|------------|
| Symbol | Parameter | AC/ACT Typ | Units | Conditions | oinse h |
| C _{IN} | Input Capacitance | 4.5 | pF | $V_{CC} = 5.0V$ | ACCOUNT OF |
| C _{PD} | Power Dissipation Capacitance | 70.0 | pF | $V_{CC} = 5.0V$ | luoni a is |





54AC/74AC253 • 54ACT/74ACT253 Dual 4-Input Multiplexer with TRI-STATE® Outputs

General Description

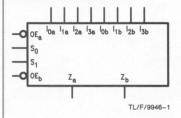
The 'AC/'ACT253 is a dual 4-input multiplexer with TRI-STATE outputs. It can select two bits of data from four sources using common select inputs. The outputs may be individually switched to a high impedance state with a HIGH on the respective Output Enable (OE) inputs, allowing the outputs to interface directly with bus oriented systems.

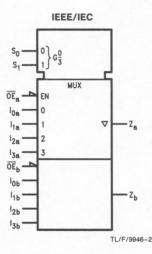
Features

- Multifunction capability
- Noninverting TRI-STATE outputs
- Outputs source/sink 24 mA
- 'ACT253 has TTL-compatible inputs

Ordering Code: See Section 5

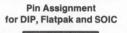
Logic Symbols

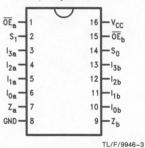




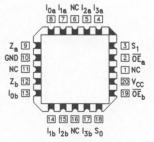
| Pin Names | Description |
|----------------------------------|----------------------------|
| I _{0a} -I _{3a} | Side A Data Inputs |
| I _{0b} -I _{3b} | Side B Data Inputs |
| S ₀ , S ₁ | Common Select Inputs |
| ŌĒa | Side A Output Enable Input |
| ŌĒb | Side B Output Enable Input |
| Z_a, Z_b | TRI-STATE Outputs |

Connection Diagrams





Pin Assignment for LCC



TL/F/9946-4

Functional Description

The 'AC/'ACT253 contains two identical 4-input multiplexers with TRI-STATE outputs. They select two bits from four sources selected by common Select inputs (S₀, S₁). The 4-input multiplexers have individual Output Enable ($\overline{\text{OE}}_a$, $\overline{\text{OE}}_b$) inputs which, when HIGH, force the outputs to a high impedance (High Z) state. This device is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two select inputs. The logic equations for the outputs are shown:

$$\begin{split} Z_{a} &= \overline{OE}_{a} \bullet (I_{0a} \bullet \overline{S}_{1} \bullet \overline{S}_{0} + I_{1a} \bullet \overline{S}_{1} \bullet S_{0} + \\ &I_{2a} \bullet S_{1} \bullet \overline{S}_{0} + I_{3a} \bullet S_{1} \bullet S_{0}) \\ Z_{b} &= \overline{OE}_{b} \bullet (I_{0b} \bullet \overline{S}_{1} \bullet \overline{S}_{0} + I_{1b} \bullet \overline{S}_{1} \bullet S_{0} + \\ &I_{2b} \bullet S_{1} \bullet \overline{S}_{0} + I_{3b} \bullet S_{1} \bullet S_{0}) \end{split}$$

If the outputs of TRI-STATE devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to TRI-STATE devices whose outputs are tied together are designed so that there is no overlap.

Truth Table

| | ect | | Data | Inputs | | Output Enable | Outputs |
|----------------|----------------|----------------|----------------|----------------|----------------|------------------|---------|
| S ₀ | S ₁ | I ₀ | l ₁ | l ₂ | l ₃ | ŌĒ | Z |
| X | Х | Х | Х | X | X | H | Z |
| L | L | L | Х | X | X | L | L |
| L | L | Н | X | X | X | L | Н |
| Н | L | X | L | X | X | s asu Lindui | L |
| Н | L | X | Н | X | X | L | Н |
| L | Н | X | X | L | X | L | L |
| L | Н | X | X | H | X | V8.0 Lon | Н |
| a Hot | Н | X | X | X | L | L _O V | L |
| Н | Н | X | X | X | н | id ® LoV | Н |

Address Inputs S₀ and S₁ are common to both sections.

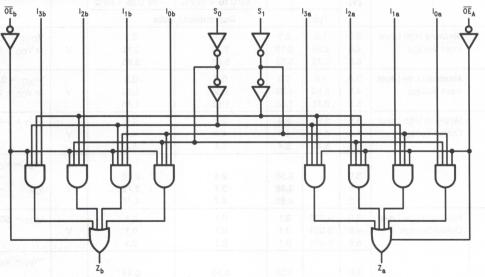
H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Z = High Impedance

Logic Diagram



TL/F/9946-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Supply Voltage (V _{CC}) | -0.5V to $+7.0V$ |
|---|--|
| DC Input Diode Current (I_{IK}) $V_I = -0.5V$ $V_I = V_{CC} + 0.5V$ | −20 mA +20 mA |
| DC Input Voltage (V _I) | -0.5 V to $V_{CC} + 0.5$ V |
| DC Output Diode Current (I_{OK}) $V_O = -0.5V$ $V_O = V_{CC} + 0.5V$ DC Output Voltage (V_O) | -20 mA +20 mA -0.5V to to V _{CC} + 0.5V |
| DC Output Source or Sink Current (I _O) | ±50 mA |
| DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND}) | ±50 mA |
| Storage Temperature (T _{STG}) | -65°C to +150°C |
| | |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

Recommended Operating Conditions

| Supply Voltage (V _{CC}) | |
|--|-----------------------------------|
| 'AC | 20V to 60V |
| 'ACT | 4 20 10 2 20 |
| Input Voltage (V _I) | 0V to V _{CC} |
| Output Voltage (VO) | |
| Operating Temperature (T _A) 74AC/ACT 54AC/ACT | -40°C to +85°C -55°C to +125°C |
| Junction Temperature (T _J) CDIP PDIP | 175°C 140°C |
| Input Rise and Fall Time (t _r , t _f) (Note 2) (Typical) (Except Schmitt Inputs) 'AC Devices V _{IN} from 30% to 70% of V _{CC} V _{CC} @ 3.0V V _{CC} @ 4.5V V _{CC} @ 5.5V | 150 ns/V 40 ns/V 25 ns/V |
| Input Rise and Fall Time (t _r , t _f) (Note 2) (Typical) (Except Schmitt Inputs) 'ACT Device V _{IN} from 0.8V to 2.0V, V _{meas} from 0.8V to 2.0V V _{CC} @ 4.5V V _{CC} @ 5.5V | 10 ns/V 8 ns/V |

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

| | | | 74 | AC | 54AC | 74AC | | ontonserior (Sec 7 |
|-----------------|--------------------------------------|---------------------|-------------------------|----------------------|----------------------------------|---------------------------------|------------------|--|
| Symbol | Parameter | V _{CC} (V) | T _A = +25°C | | T _A = -55°C to +125°C | T _A = -40°C to +85°C | Units | Conditions |
| | 0 a0 a1 | | Тур | | Guaranteed L | imits | KS ¹ | da a 450 |
| V _{IH} | Minimum High Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ |
| V _{IL} | Maximum Low Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ |
| V _{OH} | Minimum High Level Output Voltage | 3.0 4.5 5.5 | 2.99 4.49 5.49 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | ٧ | $I_{OUT} = -50 \mu\text{A}$ |
| | | 3.0 4.5 5.5 | Y | 2.56 3.86 4.86 | 2.4 3.7 4.7 | 2.46 3.76 4.76 | V | $\label{eq:VIN} \begin{split} *V_{\text{IN}} &= V_{\text{IL}} \text{or} V_{\text{IH}} \\ &- 12 \text{mA} \\ I_{\text{OH}} &- 24 \text{mA} \\ &- 24 \text{mA} \end{split}$ |
| V _{OL} | Maximum Low Level Output Voltage | 3.0 4.5 5.5 | 0.002 0.001 0.001 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | V | Ι _{ΟΟΤ} = 50 μΑ |
| | rr Tya na sourceas na stambas e | 3.0 4.5 5.5 | jon oludila | 0.36 0.36 0.36 | 0.50 0.50 0.50 | 0.44 0.44 0.44 | V so a di tan | $*V_{IN} = V_{IL} \text{ or } V_{IH}$ 12 mA I_{OL} 24 mA 24 mA |
| I _{IN} | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | ±1.0 | μА | $V_{I} = V_{CC}$, GND |

DC Characteristics for 'AC Family Devices (Continued)

| | 2440 | | 74 | AC | 54AC | 74AC | | | |
|------------------|-------------------------------------|------------------------|-----|------|----------------------------------|---------------------------------|-------|--|--|
| Symbol | Parameter | V _{CC} (V) | | | T _A = -55°C to +125°C | T _A = -40°C to +85°C | Units | Conditions | |
| .olf | Fig 96 = 20 | 36 | Тур | 0 | Guaranteed L | | | | |
| loz | Maximum TRI-STATE® | Kel | n | 68 | ralf gyT fal | | | V_{I} (OE) = V_{IL} , V_{IH} | |
| 0.0 | Current | 5.5 | | ±0.5 | ±10.0 | ±5.0 | μΑ | $V_I = V_{CC}$, GND $V_O = V_{CC}$, GND | |
| I _{OLD} | †Minimum Dynamic | 5.5 | | | 50 | 75 | mA | V _{OLD} = 1.65V Max | |
| I _{OHD} | Output Current | 5.5 | 0 | T | -50 0. | -75 | mA | V _{OHD} = 3.85V Min | |
| loc | Maximum Quiescent Supply Current | 5.5 | | 8.0 | 160.0 | 80.0 | μΑ | $V_{IN} = V_{CC}$ or GND | |

^{*}All outputs loaded; thresholds on input associated with output under test.

DC Characteristics for 'ACT Family Devices

| | | | 74 | ACT | 54ACT | 74ACT | | | |
|------------------|-------------------------------------|------------------------|------------------------------------|--------------|----------------------------------|---------------------------------|----------|---|--|
| Symbol | Parameter | V _{CC} (V) | T _A = +25°C | | T _A = -55°C to +125°C | T _A = -40°C to +85°C | Units | Conditions | |
| 8-8 | su 2 01 | | Тур | | Guaranteed Li | mits | aichaste | andano Zida | |
| V _{IH} | Minimum High Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 2.0 2.0 | 2.0 2.0 | 2.0 2.0 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{IL} | Maximum Low Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 0.8 | 0.8 | 0.8 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{OH} | Minimum High Level Output Voltage | 4.5 5.5 | 4.49 5.49 | 4.4 5.4 | 4.4 5.4 | 4.4 5.4 | ٧ | $I_{OUT} = -50 \mu\text{A}$ | |
| ,oW | 0 - 80 pF Units CL - 80 pF Wax | 4.5 5.5 | 1207 - 1 15 U2 - 1 14 U2 - 1 | 3.86 4.86 | 3.70 4.70 | 3.76 4.76 | ٧ | $^{*}V_{IN} = V_{IL} \text{ or } V_{IH}$ -24 mA -24 mA | |
| V _{OL} | Maximum Low Level Output Voltage | 4.5 5.5 | 0.001 0.001 | 0.1 0.1 | 0.1 0.1 | 0.1 0.1 | V V | $I_{OUT} = 50 \mu A$ | |
| | an dat da | 4.5 5.5 | | 0.36 0.36 | 0.50 0.50 | 0.44 0.44 | ٧ | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IN} = V_{IL} \text{ or } V_{IH}$ | |
| I _{IN} | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | ±1.0 | μА | $V_{I} = V_{CC}$, GND | |
| loz | Maximum TRI-STATE® Current | 5.5 | | ±0.5 | ±10.0 | ±5.0 | μА | $V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}, GND$ | |
| ГССТ | Maximum I _{CC} /Input | 5.5 | 0.6 | | 1.6 | 1.5 | mA | $V_{\rm I} = V_{\rm CC} - 2.1V$ | |
| I _{OLD} | †Minimum Dynamic | 5.5 | | | 50 | 75 | mA | V _{OLD} = 1.65V Max | |
| IOHD | Output Current | 5.5 | | | -50 | -75 | mA | V _{OHD} = 3.85V Min | |
| Icc | Maximum Quiescent Supply Current | 5.5 | | 8.0 | 160.0 | 80.0 | μА | V _{IN} = V _{CC} or GND | |

^{*}All outputs loaded; thresholds on input associated with output under test.

[†]Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC} . I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

[†]Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

| | | TAAC | | 74AC | | 54 | AC | 74 | AC | | | |
|------------------|---|------------|-------------------|------------|--------------|------------|--------------|--|--------------|-------|-------|-------------|
| Symbol | Parameter | Parameter | V _{CC} * | | | | to + | T _A = -55°C T _A = -40°C to +125°C to +85°C C _L = 50 pF C _L = 50 pF | | 85°C | Units | Fig. No. |
| MV No. | CONTRACTOR | | Min | Тур | Max | Min | Max | Min | Max | nixeM | 50 | |
| t _{PLH} | Propagation Delay S _n to Z _n | 3.3 5.0 | 2.0 2.0 | 8.5 6.5 | 15.5 11.0 | 1.0 1.0 | 19.5 13.5 | 2.0 1.5 | 17.5 12.5 | ns | 2-6 | |
| t _{PHL} | Propagation Delay S _n to Z _n | 3.3 5.0 | 2.5 2.0 | 9.5 7.0 | 16.0 11.5 | 1.0 1.0 | 20.0 15.0 | 2.0 1.5 | 18.0 13.0 | ns | 2-6 | |
| t _{PLH} | Propagation Delay | 3.3 5.0 | 1.5 1.5 | 7.0 5.5 | 14.5 10.0 | 1.0 1.0 | 19.0 13.0 | 1.5 1.5 | 17.0 11.5 | ns | 2-5 | |
| t _{PHL} | Propagation Delay I _n to Z _n | 3.3 5.0 | 2.0 1.5 | 7.5 5.5 | 13.0 9.5 | 1.0 1.0 | 16.0 12.0 | 1.5 1.5 | 15.0 11.0 | ns | 2-5 | |
| t _{PZH} | Output Enable Time | 3.3 5.0 | 1.5 1.5 | 4.5 3.5 | 8.0 6.0 | 1.0 1.0 | 9.5 7.0 | 1.0 1.0 | 8.5 6.5 | ns | 2-7 | |
| t _{PZL} | Output Enable Time | 3.3 5.0 | 1.5 1.5 | 5.0 3.5 | 8.0 6.0 | 1.0 | 10.0 7.5 | 1.0 1.0 | 9.0 7.0 | ns | 2-8 | |
| t _{PHZ} | Output Disable Time | 3.3 5.0 | 2.0 2.0 | 5.5 5.0 | 9.5 8.0 | 1.0 1.0 | 11.0 9.5 | 1.5 1.5 | 10.0 8.5 | ns | 2-7 | |
| t _{PLZ} | Output Disable Time | 3.3 5.0 | 1.5 1.5 | 5.0 4.0 | 8.0 7.0 | 1.0 1.0 | 9.5 8.0 | 1.0 1.0 | 9.0 7.5 | ns | 2-8 | |

^{*}Voltage Range 3.3 is 3.3V ± 0.3 V Voltage Range 5.0 is 5.0V ± 0.5 V

AC Electrical Characteristics

| | | 74ACT 54 | | 54/ | ACT | CT 74ACT | | enion's | | | |
|------------------|--|-------------------|-----|--|------|----------|---|---------|--|----|-------------|
| Symbol Parameter | | V _{CC} * | | T _A = +25°C C _L = 50 pF | | | $T_A = -55^{\circ}C$ to $+125^{\circ}C$ $C_L = 50 pF$ | | $T_A = -40^{\circ}C$ $to +85^{\circ}C$ $C_L = 50 pF$ | | Fig. No. |
| Am AS | Holl V | 87.4. | Min | Тур | Max | Min | Max | Min | Max | | |
| t _{PLH} | Propagation Delay S_n to Z_n | 5.0 | 2.0 | 7.0 | 11.5 | 1.0 | 14.5 | 2.0 | 13.0 | ns | 2-6 |
| t _{PHL} | Propagation Delay S_n to Z_n | 5.0 | 3.0 | 7.5 | 13.0 | 1.0 | 16.0 | 2.5 | 14.5 | ns | 2-6 |
| t _{PLH} | Propagation Delay | 5.0 | 2.5 | 5.5 | 10.0 | 1.0 | 12.0 | 2.0 | 11.0 | ns | 2-5 |
| t _{PHL} | Propagation Delay I _n to Z _n | 5.0 | 3.5 | 6.5 | 11.0 | 1.0 | 13.5 | 3.0 | 12.5 | ns | 2-5 |
| t _{PZH} | Output Enable Time | 5.0 | 2.0 | 4.5 | 7.5 | 1.0 | 9.5 | 1.5 | 8.5 | ns | 2-7 |
| t _{PZL} | Output Enable Time | 5.0 | 2.0 | 5.0 | 8.0 | 1.0 | 9.5 | 1.5 | 9.0 | ns | 2-8 |
| t _{PHZ} | Output Disable Time | 5.0 | 3.0 | 6.0 | 9.5 | 1.0 | 11.0 | 2.5 | 10.0 | ns | 2-7 |
| t _{PLZ} | Output Disable Time | 5.0 | 2.5 | 4.5 | 7.5 | 1.0 | 9.0 | 2.0 | 8.5 | ns | 2-8 |

^{*}Voltage Range 5.0 is 5.0V \pm 0.5V

| Capacita | nce |
|----------|-----|
|----------|-----|

| Symbol | Parameter - | AC/ACT Typ | Units | Conditions |
|-----------------|----------------------------------|---------------|-------|------------------------|
| C _{IN} | Input Capacitance | 4.5 | pF | $V_{CC} = 5.0V$ |
| C _{PD} | Power Dissipation Capacitance | 50.0 | pF | V _{CC} = 5.0V |



54AC/74AC257•54ACT/74ACT257 Quad 2-Input Multiplexer with TRI-STATE® Outputs

General Description

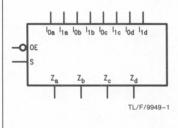
The 'AC/'ACT257 is a quad 2-input multiplexer with TRI-STATE outputs. Four bits of data from two sources can be selected using a Common Data Select input. The four outputs present the selected data in true (noninverted) form. The outputs may be switched to a high impedance state by placing a logic HIGH on the common Output Enable $\overline{(\text{OE})}$ input, allowing the outputs to interface directly with bus-oriented systems.

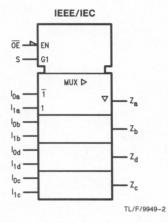
Features

- Multiplexer expansion by tying outputs together
- Noninverting TRI-STATE outputs
- Outputs source/sink 24 mA
- 'ACT257 has TTL-compatible inputs

Ordering Code: See Section 5

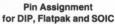
Logic Symbols

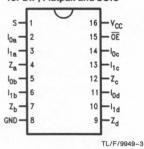




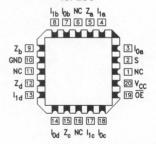
| Pin Names | Description |
|----------------------------------|-------------------------------|
| S | Common Data Select Input |
| ŌĒ | TRI-STATE Output Enable Input |
| $I_{0a}-I_{0d}$ | Data Inputs from Source 0 |
| I _{1a} -I _{1d} | Data Inputs from Source 1 |
| $Z_a - Z_d$ | TRI-STATE Multiplexer Outputs |

Connection Diagrams





Pin Assignment for LCC



TL/F/9949-4

Functional Description

The 'AC/'ACT257 is guad 2-input multiplexer with TRI-STATE outputs. It selects four bits of data from two sources under control of a Common Data Select input. When the Select input is LOW, the I_{0x} inputs are selected and when Select is HIGH, the I_{1x} inputs are selected. The data on the selected inputs appears at the outputs in true (noninverted) form. The device is the logic implementation of a 4-pole, 2position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$$Z_{a} = \overline{OE} \bullet (1_{1a} \bullet S + I_{0a} \bullet \overline{S})$$

$$Z_{b} = \overline{OE} \bullet (1_{1b} \bullet S + I_{0b} \bullet \overline{S})$$

$$Z_{b} = \overline{OE} \bullet (1_{1b} \bullet S + I_{0b} \bullet \overline{S})$$

$$Z_{c} = \overline{OE} \bullet (1_{1c} \bullet S + I_{0c} \bullet \overline{S})$$

$$Z_d = \overline{OE} \cdot (1_{1d} \cdot S + I_{0d} \cdot \overline{S})$$

When the Output Enable (OE) is HIGH, the outputs are forced to a high impedance state. If the outputs are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure the Output Enable signals to TRI-STATE devices whose outputs are tied together are designed so there is no overlap.

Truth Table

| Output Enable | Select Input | | ata outs | Outputs |
|------------------|-----------------|----------------|----------------|----------------------|
| ŌĒ | S | I ₀ | l ₁ | Z |
| Am OSH | X | Х | X | 72.0 - Z OV |
| Am 09L | Н | X | Falo | 1 00 (E oV |
| Vail Loov o | Va.O.H | X | H | 16V 16 H 6 30 |
| Am oak | L (al) 18 | onLO ! | X | 00 0 L u0 00 |
| L | L | Н | X | H V OO |

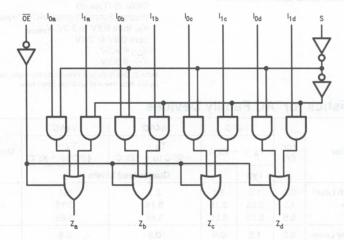
H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Z = High Impedance

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Supply Voltage (V _{CC}) | -0.5V to 7.0V |
|---|------------------------------|
| DC Input Diode Current (I _{IK}) | |
| $V_I = -0.5V$ | -20 mA |
| $V_I = V_{CC} + 0.5V$ | + 20 mA |
| DC Input Voltage (V _I) | -0.5 V to $V_{CC} + 0.5$ V |
| DC Output Diode Current (IOK) | |
| $V_{O} = -0.5V$ | -20 mA |
| $V_O = V_{CC} + 0.5V$ | + 20 mA |
| DC Output Voltage (V _O) | -0.5 V to $V_{CC} + 0.5$ V |
| DC Output Source or Sink Current (IO) | ± 50 mA |
| DC V _{CC} or Ground Current | |
| Per Output Pin (I _{CC} or I _{GND}) | ±50 mA |

Storage Temperature (T_{STG}) —65°C to +150°C Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

| Supply Voltage (V _{CC}) | |
|---|-----------------------|
| 'AC Service on Salest and Office | 0.01/+0.6.01/ |
| 'ACT | |
| Input Voltage (V _I) | |
| Output Voltage (Vo) | 0V to V _{CC} |
| Operating remperature (1A) | |
| 74AC/ACT | -40°C to +85°C |
| 54AC/ACT | -55°C to +125°C |
| Junction Temperature (T _J) | |
| CDIP | 175°C |
| PDIP (9 A 1 A 2 A 1 A | 140°C |

Input Rise and Fall Time (tr, tf)

(Note 2) (Typical)

(Except Schmitt Inputs) 'AC Devices

Input Rise and Fall Time (t_r, t_f)

(Note 2) (Typical)

(Except Schmitt Inputs) 'ACT Devices

 V_{IN} from 0.8V to 2.0V, V_{meas}

from 0.8V to 2.0V

V_{CC} @ 4.5V V_{CC} @ 5.5V 10 ns/V 8 ns/V

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

| | | - Table | 74 | AC | 54AC | 74AC | | | |
|--|--------------------------------------|------------------------|-------------------------|----------------------|----------------------------------|---------------------------------|--------------------|--|--|
| Symbol | Parameter | V _{CC} (V) | T _A = +25°C | | T _A = -55°C to +125°C | T _A = -40°C to +85°C | Units | Conditions | |
| | | 4 | Тур | - ALL | Guaranteed L | imits | | | |
| V _{IH} Minimum High Level Input Voltage | | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{IL} | Maximum Low Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | 50 8 V 1-11 | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{OH} | Minimum High Level Output Voltage | 3.0 4.5 5.5 | 2.99 4.49 5.49 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | V | $I_{OUT} = -50 \mu\text{A}$ | |
| | | 3.0 4.5 5.5 | | 2.56 3.86 4.86 | 2.4 3.7 4.7 | 2.46 3.76 4.76 | V | $\begin{tabular}{ll} *V_{IN} &= V_{IL} \mbox{ or } V_{IH} \\ &- 12 \mbox{ mA} \\ I_{OH} &- 24 \mbox{ mA} \\ &- 24 \mbox{ mA} \\ \end{tabular}$ | |
| V _{OL} | Maximum Low Level Output Voltage | 3.0 4.5 5.5 | 0.002 0.001 0.001 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | V | $I_{OUT} = 50 \mu A$ | |
| | | 3.0 4.5 5.5 | | 0.36 0.36 0.36 | 0.50 0.50 0.50 | 0.44 0.44 0.44 | V | $V_{IN} = V_{IL} \text{ or } V_{IH}$ 12 mA V_{IOL} 24 mA 24 mA | |
| I _{IN} | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | ±1.0 | μΑ | $V_{I} = V_{CC}$, GND | |

| | 74AC | | 74 | AC | 54AC | 74AC | | | |
|------------------|--------------------------------------|------------------------|-------------------------|--------|-----------------------------------|---------------------------------|-------|--|--|
| Symbol | Parameter | V _{CC} (V) | T _A = + 25°C | | T _A = -55°C to + 125°C | T _A = -40°C to +85°C | Units | Conditions | |
| | 70 03 = 10 | | Тур | 6 - 10 | Guaranteed L | imits | | and the state of t | |
| loz | Maximum TRI-STATE Leakage Current | 5.5 | 0.8 | ±0.5 | ±10.0 | ±5.0 | μА | V_{I} (OE) = V_{IL} , V_{IH} $V_{I} = V_{CC}$, GND $V_{O} = V_{CC}$, GND | |
| I _{OLD} | †Minimum Dynamic | 5.5 | | 0. | 50 | 75 | mA | V _{OLD} = 1.65V Max | |
| IOHD | Output Current | 5.5 | 0.11 | 0. | -50 | -75 | mA | V _{OHD} = 3.85V Min | |
| Icc | Maximum Quiescent Supply Current | 5.5 | 0.8 h | 8.0 | 160.0 | 80.0 | μА | V _{IN} = V _{CC} or GND | |

^{*}All outputs loaded; thresholds on input associated with output under test.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}. I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

| | | | 744 | CT | 54ACT | 74ACT | | | |
|------------------|--------------------------------------|-----------------|------------------------|--------------|-----------------------------------|---------------------------------|-----------|---|--|
| Symbol | Parameter | V _{CC} | T _A = +25°C | | T _A = -55°C to + 125°C | T _A = -40°C to +85°C | Units | Conditions | |
| | | | Тур | | Guaranteed Li | mits | 78.0 ± V0 | 8 at 0.8 opnak ogsåd/ | |
| V _{IH} | Minimum High Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 2.0 2.0 | 2.0 2.0 | 2.0 2.0 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{IL} | Maximum Low Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 0.8 | 0.8 0.8 | 0.8 0.8 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{OH} | Minimum High Level Output Voltage | 4.5 5.5 | 4.49 5.49 | 4.4 5.4 | 4.4 5.4 | 4.4 5.4 | ٧ | $I_{OUT} = -50 \mu\text{A}$ | |
| 8-9 | ėn 3,5 (| 4.5 5.5 | 0.8 | 3.86 4.86 | 3.70 4.70 | 3.76 4.76 | v | $\begin{tabular}{ll} *V_{\mbox{IN}} &= V_{\mbox{IL}} \mbox{ or } V_{\mbox{IH}} \\ &-24 \mbox{ mA} \\ &-24 \mbox{ mA} \end{tabular}$ | |
| V _{OL} | Maximum Low Level Output Voltage | 4.5 5.5 | 0.001 0.001 | 0.1 0.1 | 0.1 0.1 | 0.1 0.1 | ٧ | $I_{OUT} = 50 \mu A$ | |
| | an (8.0) an | 4.5 5.5 | 0.1 t | 0.36 0.36 | 0.50 0.50 | 0.44 0.44 | eCV. | $\label{eq:VIN} \begin{array}{l} ^* V_{\text{IN}} = V_{\text{IL}} \text{or} V_{\text{IH}} \\ \text{I}_{\text{OL}} \qquad \qquad 24 \text{mA} \\ \\ \text{24 mA} \end{array}$ | |
| I _{IN} | Maximum Input Leakage Current | 5.5 | 3.6 | ±0.1 | 0.8 ± 1.0 .3 0 | ±1.0 | μА | $V_{I} = V_{CC}$, GND | |
| loz | Maximum TRI-STATE Leakage Current | 5.5 | 3,5 | ±0.5 | ±10.0 | ±5.0 | μА | $V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}, GND$ | |
| ICCT | Maximum I _{CC} /Input | 5.5 | 0.6 | 0,3 | 1.6 | 1.5 | mA | $V_{\rm I} = V_{\rm CC} - 2.1V$ | |
| I _{OLD} | †Minimum Dynamic | 5.5 | | | 50 | 75 | mA | V _{OLD} = 1.65V Max | |
| I _{OHD} | Output Current | 5.5 | | | -50 | -75 | mA | V _{OHD} = 3.85V Min | |
| Icc | Maximum Quiescent Supply Current | 5.5 | 0 | 8.0 | 160.0 | 80.0 | μΑ | V _{IN} = V _{CC} or GND | |

^{*}All outputs loaded; thresholds on input associated with output under test.

[†]Maximum test duration 2.0 ms, one output loaded at a time.

[†]Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

| | | MAG | | 74AC | DAAC | 54 | AC | 74 | AC | | |
|------------------|--|-------------------|------------|-------------------|-------------|------------|-------------------------|------------|------------------------|-------|-------------|
| Symbol | Parameter | V _{CC} * | | \ = +2 \(= 50 | | to + | −55°C 125°C 50 pF | to + | -40°C 85°C 50 pF | Units | Fig. No. |
| t _{PLH} | Propagation Delay | 3.3 5.0 | 1.5 1.5 | 5.0 4.0 | 8.5 6.0 | 1.0 1.0 | 11.0 8.0 | 1.0 1.0 | 9.0 7.0 | ns | 2-6 |
| t _{PHL} | Propagation Delay | 3.3 5.0 | 1.5 1.5 | 6.0 4.5 | 8.5 6.0 | 1.0 1.0 | 11.0 8.5 | 1.0 1.0 | 9.0 7.0 | ns | 2-6 |
| t _{PLH} | Propagation Delay S to Z _n | 3.3 5.0 | 1.5 1.5 | 7.0 5.0 | 10.5 7.5 | 1.0 1.0 | 14.5 11.0 | 1.5 1.0 | 11.5 8.5 | ns | 2-6 |
| t _{PHL} | Propagation Delay S to Z _n | 3.3 5.0 | 1.5 1.5 | 7.5 5.5 | 10.5 7.5 | 1.0 1.0 | 14.5 11.0 | 1.5 1.0 | 11.5 8.5 | ns | 2-6 |
| t _{PZH} | Output Enable Time | 3.3 5.0 | 1.5 1.5 | 6.5 5.0 | 9.5 7.5 | 1.0 1.0 | 13.0 | 1.0 | 10.5 8.5 | ns | 2-7 |
| t _{PZL} | Output Enable Time | 3.3 5.0 | 1.5 1.5 | 5.5 5.0 | 9.0 8.5 | 1.0 1.0 | 11.0 9.5 | 1.0 1.0 | 10.0 9.5 | ns | 2-8 |
| t _{PHZ} | Output Disable Time | 3.3 5.0 | 1.5 1.5 | 5.5 5.0 | 10.0 | 1.0 1.0 | 13.0 11.0 | 1.0 1.0 | 11.0 10.0 | ns | 2-7 |
| t _{PLZ} | Output Disable Time | 3.3 5.0 | 1.5 1.5 | 5.5 5.0 | 9.0 8.0 | 1.0 1.0 | 10.5 9.5 | 1.0 | 10.0 9.0 | ns | 2-8 |

^{*}Voltage Range 3.3 is 3.0V ± 0.3 V Voltage Range 5.0 is 5.0V ± 0.5 V

AC Electrical Characteristics

| | Vite = moV / V | | | 74AC1 | 0 | 54/ | ACT | 74 | ACT | mixeld | ال | |
|------------------|--|-----|--------------------------|-------|--------------------|-----|------|-------------------------|------|------------------------|-------|-------------|
| Symbol | Parameter | | V _{CC} * (V) | | \ = +2 \ \ = 50 | | to + | -55°C 125°C 50 pF | to + | -40°C 85°C 50 pF | Units | Fig. No. |
| t _{PLH} | Propagation Delay | 5.0 | 1.5 | 5.0 | 7.0 | 1.0 | 8.0 | 1.0 | 7.5 | ns | 2-6 | |
| t _{PHL} | Propagation Delay | 5.0 | 2.0 | 6.0 | 7.5 | 1.0 | 9.5 | 1.5 | 8.5 | ns | 2-6 | |
| t _{PLH} | Propagation Delay S to Z _n | 5.0 | 2.0 | 7.0 | 9.5 | 1.0 | 11.0 | 1.5 | 10.5 | ns | 2-6 | |
| tPHL | Propagation Delay S to Z _n | 5.0 | 2.5 | 7.0 | 10.5 | 1.0 | 11.5 | 2.0 | 11.5 | ns | 2-6 | |
| t _{PZH} | Output Enable Time | 5.0 | 2.0 | 6.0 | 8.0 | 1.0 | 9.5 | 1.5 | 9.0 | ns | 2-7 | |
| t _{PZL} | Output Enable Time | 5.0 | 2.0 | 6.0 | 8.0 | 1.0 | 9.5 | 1.5 | 9.0 | ns | 2-8 | |
| t _{PHZ} | Output Disable Time | 5.0 | 2.5 | 6.5 | 9.0 | 1.0 | 10.5 | 1.5 | 10.0 | ns | 2-7 | |
| t _{PLZ} | Output Disable Time | 5.0 | 2.0 | 6.0 | 7.5 | 1.0 | 9.0 | 1.5 | 8.5 | ns | 2-8 | |

^{*}Voltage Range 5.0 is 5.0V ± 0.5 V

Capacitance

| Symbol | Parameter | AC/ACT | Units | Conditions | | |
|-----------------|----------------------------------|--------|-------|------------------------|--|--|
| GADAO | Au diameter | Тур | Onits | Oditations | | |
| C _{IN} | Input Capacitance | 4.5 | pF | $V_{CC} = 5.0V$ | | |
| C _{PD} | Power Dissipation Capacitance | 50.0 | pF | V _{CC} = 5.0V | | |



54AC/74AC258 • 54ACT/74ACT258 Quad 2-Input Multiplexer with TRI-STATE® Outputs

General Description

The 'AC/'ACT258 is a quad 2-input multiplexer with TRI-STATE outputs. Four bits of data from two sources can be selected using a common data select input. The four outputs present the selected data in the complement (inverted) form. The outputs may be switched to a high impedance state with a HIGH on the common Output Enable (OE) input, allowing the outputs to interface directly with bus-oriented systems.

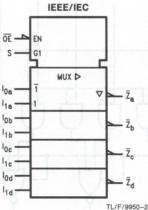
Features

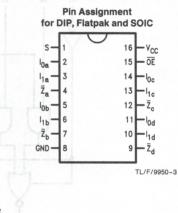
- Multiplexer expansion by tying outputs together
- Inverting TRI-STATE outputs
- Outputs source/sink 24 mA
- 'ACT258 has TTL-compatible inputs

Ordering Code: See Section 5

Logic Symbols

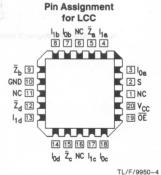
OE S TL/F/9950-1 OB TL/F/9950-1





Connection Diagrams

| 2038 | Pin Names | Description | |
|------|-----------------------------------|----------------------------------|--|
| Sey. | S | Common Data Select Input | |
| | OE | TRI-STATE Output Enable Input | |
| | $I_{0a} - I_{0d}$ | Data Inputs from Source 0 | |
| | I _{1a} -I _{1d} | Data Inputs from Source 1 | |
| | $\overline{Z}_a - \overline{Z}_d$ | TRI-STATE Inverting Data Outputs | |



TL/F/9950-

Functional Description

The 'AC/'ACT258 is a quad 2-input multiplexer with TRI-STATE outputs. It selects four bits of data from two sources under control of a common Select input (S). When the Select input is LOW, the $\rm l_{0x}$ inputs are selected and when Select is HIGH, the $\rm l_{1x}$ inputs are selected. The data on the selected inputs appears at the outputs in inverted form. The 'AC/'ACT258 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$$\begin{split} \overline{Z}_{a} &= \overline{OE} \bullet (I_{1a} \bullet S + I_{0a} \bullet \overline{S}) \\ \overline{Z}_{b} &= \overline{OE} \bullet (I_{1b} \bullet S + I_{0b} \bullet \overline{S}) \\ \overline{Z}_{c} &= \overline{OE} \bullet (I_{1c} \bullet S + I_{0c} \bullet \overline{S}) \\ \overline{Z}_{d} &= \overline{OE} \bullet (I_{1d} \bullet S + I_{0d} \bullet \overline{S}) \end{split}$$

When the Output Enable input (\overline{OE}) is HIGH, the outputs are forced to a high impedance state. If the outputs of the TRI-STATE devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should

ensure that Output Enable signals to TRI-STATE devices whose outputs are tied together are designed so there is no overlap.

Truth Table

| Output Enable | Select Input | ALC: NOT THE | ata outs | Outputs |
|------------------|-----------------|----------------|-------------|----------|
| ŌĒ | S | I ₀ | 11 | Z |
| H of Calle | X | X | X | Z |
| secfics on | Н | X | L | Н |
| L | Н | X | Н | belon Le |
| L | L | L | X | Н |
| L | L | Н | X | L |

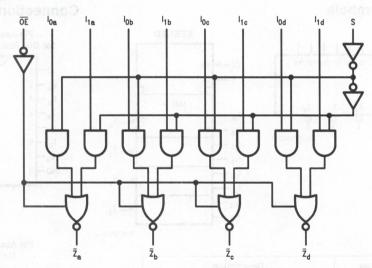
H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Z = High Impedance

Logic Diagram



TL/F/9950-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1) Recommended Operating

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Office, Pictipatore for availab | mity and specimoutions. |
|---|---------------------------------|
| Supply Voltage (V _{CC}) | -0.5V to $+7.0$ V |
| DC Input Diode Current (IIK) | |
| $V_1 = -0.5V$ | -20 mA |
| $V_I = V_{CC} + 0.5V$ | + 20 mA |
| DC Input Voltage (V _I) | -0.5 V to $V_{CC} + 0.5$ V |
| DC Output Diode Current (IOK) | |
| $V_0 = -0.5V$ | -20 mA |
| $V_O = V_{CC} + 0.5V$ | + 20 mA |
| DC Output Voltage (V _O) | -0.5 V to to $V_{CC} + 0.5$ V |
| DC Output Source | |
| or Sink Current (IO) | ±50 mA |
| DC V _{CC} or Ground Current | |
| per Output Pin (I _{CC} or I _{GND}) | \pm 50 mA |
| Storage Temperature (T _{STG}) | -65°C to +150°C |
| | |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

Recommended Operating Conditions

| Supply Voltage (VCC | 2) |
|---------------------------------|---|
| 'AC | 2.0V to 6.0V |
| 'ACT | 4.5V to 5.5V |
| Input Voltage (V _I) | 0V to V _{CC} |
| Output Voltage (VO) | OV to VCC |
| Operating Temperat | |
| 74AC/ACT | -40°C to +85°C |
| 54AC/ACT | -55°C to +125°C |
| Junction Temperatu | re (Tu) platsayC munifold (1) |
| CDIP | 2.3 175°C |
| PDIP | 140°C |
| Input Rise and Fall | Co Maximum Quiescept (t. t) emiT |
| (Note 2) (Typical) | Time (4, 4) Identify Current |
| | nputs) 'AC Devices |
| | 70% of V _{CC} |
| | 150 ns/V |
| | 40 ns/V |
| V _{CC} @ 5.5V | 25 ns/V |
| Input Rise and Fall | Time (t _r , t _f) |
| (Note 2) (Typical) | Timo (q, q) |
| | nputs) 'ACT Devices |
| V _{IN} from 0.8V to 2 | |
| from 0.8V to 2.0V | |
| V _{CC} @ 4.5V | 10 ns/V |
| V _{CC} @ 5.5V | 8 ns/V |
| | |

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

| | Parameter | 8.4 | | | 54AC | 74AC | Units | SERON FROM | |
|----------------------------|--------------------------------------|------------------------|-------------------------|----------------------|----------------------------------|---------------------------------|-----------------------|--|--|
| Symbol | | V _{CC} (V) | | | T _A = -55°C to +125°C | T _A = -40°C to +85°C | | Conditions | |
| 141V TO 1 | V = valv*) | 207 12 | Тур | acc | Guaranteed L | imits | | | |
| V _{IH} S = | Minimum High Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| VIL HIV 70 31 Am 1/3 | Maximum Low Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | V | V _{OUT} = 0.1V or V _{CC} - 0.1V | |
| Voh | Minimum High Level Output Voltage | 3.0 4.5 5.5 | 2.99 4.49 5.49 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | V | $I_{OUT} = -50 \mu A$ | |
| CMO VI.S | oV = oV oV = v Am | 3.0 4.5 5.5 | | 2.56 3.86 4.86 | 2.4 3.7 4.7 | 2.46 3.76 4.76 | V | $*V_{IN} = V_{IL} \text{ or } V_{IH} - 12 \text{ m/s}$ $I_{OH} - 24 \text{ m/s}$ -24 m/s | |
| V _{OL} | Maximum Low Level Output Voltage | 3.0 4.5 5.5 | 0.002 0.001 0.001 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | Jnen V neoseinO | I _{OUT} = 50 μA | |
| | (610) (6) | 3.0 4.5 5.5 | | 0.36 0.36 0.36 | 0.50 0.50 0.50 | 0.44 0.44 0.44 | ٧ | $*V_{IN} = V_{IL} \text{ or } V_{IH}$ 12 mA I_{OL} 24 mA 24 mA | |
| I _{IN} | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | ±1.0 | μΑ | $V_{I} = V_{CC}$, GND | |

DC Characteristics for 'AC Family Devices (Continued) and all and an applicable and a second and

| Symbol | | | 74 | AC | 54AC | 74AC | etje 90s Gu on | Conditions $V_{I} (OE) = V_{IL}, V_{IH}$ $V_{I} = V_{CC}, GND$ $V_{A} = V_{AB}, GND$ | |
|------------------|-------------------------------------|---------------------|----------------------|--------------------|----------------------------------|---------------------------------|-------------------|--|--|
| | Parameter | V _{CC} (V) | | 4 = 25°C | T _A = -55°C to +125°C | T _A = -40°C to +85°C | Units | | |
| | (0 | | Тур | of Voltag | Guaranteed L | imits | (Jul) Iner | DO Inper Diode Cur | |
| loz | Maximum TRI-STATE® Current | 5.5 | ye (Vo negme T | ±0.5 | ±10.0 | ±5.0 | μА | | |
| I _{OLD} | †Minimum Dynamic | 5.5 | constitu | DROUNE Silenius | 50 60 | 75 | mA | V _{OLD} = 1.65V Max | |
| IOHD | Output Current | 5.5 | | 910 | -50 | -75 | mA | V _{OHD} = 3.85V Min | |
| Icc | Maximum Quiescent Supply Current | 5.5 | is in on | 8.0 | 160.0 | 80.0 | μΑ | $V_{IN} = V_{CC}$ or GND | |

^{*}All outputs loaded; thresholds on input associated with output under test.

DC Characteristics for 'ACT Family Devices

| | ngule) "ACT Devices | | 74ACT | | 54ACT | 74ACT | LONG WITT | DASI to dosptish busin | |
|------------------|---|---------------|----------------|--------------|--------------|--------------|-----------|---|--|
| Symbol | Parameter | Parameter A A | | | Units | Conditions | | | |
| Viens | | | Тур | aV | Guaranteed L | _imits | | | |
| V _{IH} | Minimum High Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 2.0 | 2.0 2.0 | 2.0 2.0 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{IL} | Maximum Low Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 0.8 | 0.8 0.8 | 0.8 0.8 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{OH} | Minimum High Level Output Voltage | 4.5 5.5 | 4.49 5.49 | 4.4 5.4 | 4.4 5.4 | 4.4 5.4 | ٧ | $I_{OUT} = -50 \mu\text{A}$ | |
| | = 100V f.5 | 4.5 5.5 | ill bee | 3.86 4.86 | 3.70 4.70 | 3.76 4.76 | V | $^*V_{IN} = V_{IL} \text{ or } V_{IH}$ -24 mA -24 mA | |
| V _{OL} | Maximum Low Level Output Voltage | 4.5 5.5 | 0.001 0.001 | 0.1 0.1 | 0.1 0.1 | 0.1 0.1 | ٧ | $I_{OUT} = 50 \mu A$ | |
| V1.0 | 0.0 (A) | 4.5 5.5 | | 0.36 0.36 | 0.50 0.50 | 0.44 0.44 | V | $\begin{tabular}{ll} *V_{IN} = V_{IL} \mbox{ or } V_{IH} \\ I_{OL} & 24 \mbox{ mA} \\ & 24 \mbox{ mA} \\ \end{tabular}$ | |
| I _{IN} | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | ±1.0 | μΑ | $V_I = V_{CC}$, GND | |
| loz | Maximum TRI-STATE® Current | 5.5 | | ±0.5 | ±10.0 | ±5.0 | μΑ | $V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}, GND$ | |
| ICCT | Maximum I _{CC} /Input | 5.5 | 0.6 | 2.4 | 1.6 | 1.5 | mA | $V_{\rm I} = V_{\rm CC} - 2.1V$ | |
| I _{OLD} | †Minimum Dynamic Output Current | | | 1,5 | 50 | 75 | mA | V _{OLD} = 1.65V Max | |
| I _{OHD} | | | | 1.0 | -50 | -75 lave | mA | V _{OHD} = 3.85V Min | |
| Icc | Maximum Quiescent Supply Current | 5.5 | | 8.0 | 160.0 | 80.0 | μΑ | $V_{IN} = V_{CC}$ or GND | |

^{*}All outputs loaded; thresholds on input associated with output under test.

[†]Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC} . I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

[†]Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

| | | | | 74AC | | 54 | AC | 74 | AC | | |
|------------------|---|--------------------------|--|------------|-------------|--|--------------|--|--------------|--------|-------------|
| Symbol | Parameter | V _{CC} * (V) | T _A = +25°C C _L = 50 pF | | | $T_A = -55^{\circ}C$ $to + 125^{\circ}C$ $C_L = 50 pF$ | | $T_A = -40^{\circ}C$ to $+85^{\circ}C$ $C_L = 50 \text{ pF}$ | | Units | Fig. No. |
| | | | Min | Тур | Max | Min | Max | Min | Max | 154 16 | a.a |
| t _{PLH} | Propagation Delay I_n to \overline{Z}_n | 3.3 5.0 | 2.0 1.5 | 6.0 4.5 | 9.5 7.5 | 1.0 1.0 | 12.0 9.5 | 1.5 1.0 | 11.0 8.5 | ns | 2-5 |
| t _{PHL} | Propagation Delay I_n to \overline{Z}_n | 3.3 5.0 | 2.0 1.5 | 5.0 4.0 | 8.5 6.5 | 1.0 1.0 | 10.5 7.5 | 1.5 1.0 | 9.5 7.0 | ns | 2-5 |
| t _{PLH} | Propagation Delay S to \overline{Z}_n | 3.3 5.0 | 3.0 2.0 | 7.5 6.0 | 12.0 9.5 | 1.0 | 15.0 11.5 | 2.5 1.5 | 14.0 10.5 | ns | 2-6 |
| t _{PHL} | Propagation Delay S to \overline{Z}_n | 3.3 5.0 | 2.5 1.5 | 7.5 5.5 | 11.5 9.0 | 1.0 1.0 | 14.0 10.5 | 2.0 1.5 | 13.0 10.0 | ns | 2-6 |
| ^t PZH | Output Enable Time | 3.3 5.0 | 2.5 1.5 | 6.0 4.5 | 9.5 7.5 | 1.0 1.0 | 11.5 9.0 | 2.0 1.5 | 10.5 8.5 | ns | 2-7 |
| t _{PZL} | Output Enable Time | 3.3 5.0 | 2.0 1.5 | 5.5 5.5 | 9.0 7.0 | 1.0 1.0 | 10.5 8.5 | 1.5 1.0 | 10.0 8.0 | ns | 2-8 |
| t _{PHZ} | Output Disable Time | 3.3 5.0 | 2.5 2.0 | 5.5 5.5 | 10.0 8.5 | 1.0 1.0 | 11.5 9.5 | 2.0 1.5 | 11.5 9.0 | ns | 2-7 |
| t _{PLZ} | Output Disable Time | 3.3 5.0 | 2.0 1.5 | 5.5 5.0 | 9.0 7.0 | 1.0 1.0 | 10.5 8.5 | 2.0 1.5 | 10.0 8.0 | ns | 2-8 |

*Voltage Range 3.3 is 3.3V ±0.3V Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics

| Symbol | Parameter | 80 (83) | 74ACT | | 54/ | ACT | 74ACT | | | | |
|------------------|---|-------------------|--|-----|------|---|-------|--|------|--------|------|
| | | V _{CC} * | T _A = +25°C C _L = 50 pF | | | $T_A = -55^{\circ}C$ to $+125^{\circ}C$ $C_L = 50 pF$ | | $T_A = -40^{\circ}C$ to $+85^{\circ}C$ $C_L = 50 \text{ pF}$ | | Units | Fig. |
| | | | Min | Тур | Max | Min | Max | Min | Max | DEL TO | -ā\u |
| t _{PLH} | Propagation Delay I_n to \overline{Z}_n | 5.0 | 2.0 | 6.5 | 8.5 | 1.0 | 10.5 | 1.5 | 9.5 | ns | 2-5 |
| t _{PHL} | Propagation Delay I_n to \overline{Z}_n | 5.0 | 2.0 | 5.5 | 7.5 | 1.0 | 9.0 | 1.5 | 8.0 | ns | 2-5 |
| t _{PLH} | Propagation Delay S to \overline{Z}_n | 5.0 | 3.0 | 7.5 | 10.5 | 1.0 | 13.0 | 2.0 | 11.5 | ns | 2-6 |
| t _{PHL} | Propagation Delay S to \overline{Z}_n | 5.0 | 1.5 | 7.0 | 9.5 | 1.0 | 12.0 | 1.5 | 11.0 | ns | 2-6 |
| t _{PZH} | Output Enable Time | 5.0 | 2.0 | 6.5 | 8.5 | 1.0 | 10.5 | 1.5 | 9.5 | ns | 2-7 |
| t _{PZL} | Output Enable Time | 5.0 | 2.0 | 6.5 | 8.5 | 1.0 | 10.0 | 1.5 | 9.5 | ns | 2-8 |
| t _{PHZ} | Output Disable Time | 5.0 | 1.5 | 7.0 | 9.0 | 1.0 | 10.5 | 1.0 | 10.0 | ns | 2-7 |
| t _{PLZ} | Output Disable Time | 5.0 | 2.0 | 6.0 | 8.0 | 1.0 | 10.0 | 1.5 | 9.0 | ns | 2-8 |

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

| Symbol | Parameter | AC/ACT | Units | Conditions |
|-----------------|----------------------------------|--------|--------|------------------------|
| Symbol | Farameter | Тур | Office | P-8888VAVST |
| C _{IN} | Input Capacitance | 4.5 | pF | $V_{CC} = 5.0V$ |
| C _{PD} | Power Dissipation Capacitance | 55.0 | pF | V _{CC} = 5.0V |



54AC/74AC269 8-Bit Bidirectional Binary Counter

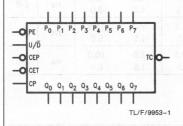
General Description

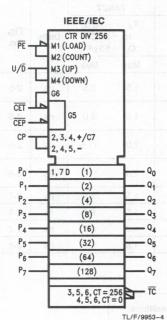
The 'AC269 is a fully synchronous 8-stage up/down counter featuring a preset capability for programmable operation, carry lookahead for easy cascading and a U/D input to control the direction of counting. All state changes, whether in counting or parallel loading, are initiated by the rising edge of the clock.

Features

- Synchronous counting and loading
- Built-in lookahead carry capability
- 300 mil slimline package

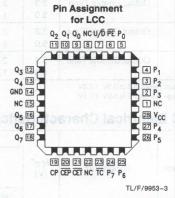
Logic Symbols





Connection Diagrams





Function Table

| | PE CEP | | CET | U/D | CP | Function |
|---|--------|-----|-----|-----|----|---------------------|
| 1 | L | X | X | X | 1 | Parallel Load All |
| | | 0.5 | 0.0 | | 5 | Flip-Flops |
| | Н | Н | X | X | 1 | Hold |
| | Н | X | Н | X | _ | Hold (TC Held HIGH) |
| | Н | L | L | Н | _ | Count Up |
| | Н | L | L | L | 1 | Count Down |

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

= Transition LOW-to-HIGH

54AC/74AC273 • 54ACT/74ACT273 Octal D Flip-Flop

General Description

The 'AC/'ACT273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ($\overline{\text{MR}}$) input load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the $\overline{\text{MR}}$ input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

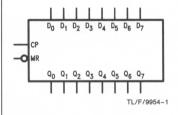
Features

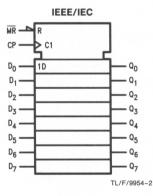
- Ideal buffer for MOS microprocessor or memory
- Eight edge-triggered D flip-flops
- Buffered common clock
- Buffered, asynchronous master reset
- See '377 for clock enable version
- See '373 for transparent latch version
- See '374 for TRI-STATE version
- Outputs source/sink 24 mA
- 'ACT273 has TTL compatible inputs

The information for the ACT273 is Advanced Information only.

Ordering Code: See Section 5

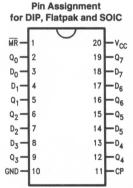
Logic Symbols



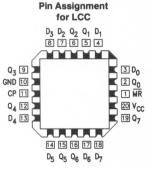


| Pin Names | Description |
|--------------------------------|-------------------|
| D ₀ -D ₇ | Data Inputs |
| MR | Master Reset |
| CP | Clock Pulse Input |
| $Q_0 - Q_7$ | Data Outputs |

Connection Diagrams



TL/F/9954-3



TL/F/9954-4

Mode Select-Function Table

| Operating Mode | | | Outputs | |
|----------------|----|----|---------|--------|
| operating mode | MR | CP | Dn | Qn |
| Reset (Clear) | L | X | X | TO THE |
| Load '1' | Н | 5 | Н | Н |
| Load '0' | Н | _ | L | L |

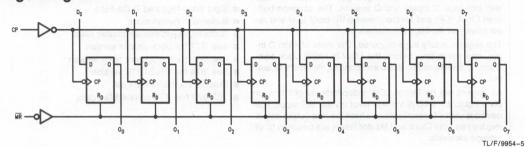
H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

✓ = LOW-to-HIGH Transition

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Supply Voltage (V _{CC}) | -0.5V to $+7.0$ V |
|---|---------------------------------|
| DC Input Diode Current (I _{IK}) | |
| $V_{I} = -0.5V$ | -20 mA |
| $V_I = V_{CC} + 0.5V$ | + 20 mA |
| DC Input Voltage (V _I) | $-0.5V$ to $V_{CC} + 0.5V$ |
| DC Output Diode Current (I_{OK}) $V_O = -0.5V$ | -20 mA |
| | 201117 |
| $V_O = V_{CC} + 0.5V$ | + 20 mA |
| DC Output Voltage (V _O) | -0.5 V to to $V_{CC} + 0.5$ V |
| DO Outrant Courses | |

DC Output Source
or Sink Current (I_O) ±50 mA

DC V_{CC} or Ground Current

Storage Temperature (T_{STG}) -65°C to +150°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recom-

mend operation of FACT™ circuits outside databook specifications.

per Output Pin (I_{CC} or I_{GND})

Recommended Operating Conditions

| Supply Voltage (V _{CC}) 'AC 'ACT | 2.0V to 6.0V 4.5 to 5.5V |
|---|-----------------------------------|
| Input Voltage (V _I) | 0V to V _{CC} |
| Output Voltage (V _O) | 0V to V _{CC} |
| Operating Temperature (T _A) 74AC/ACT 54AC/ACT | -40°C to +85°C -55°C to +125°C |
| PDIP | 175°C 140°C |
| Input Rise and Fall Time (t _r , t _f (Note 2) (Typical) (Except Schmitt Inputs) 'AC V _{IN} from 30% to 70% of V _{CC} @ 3.0V | Devices |
| V _{CC} @ 4.5V | 40 ns/V |
| V _{CC} @ 5.5V | 25 ns/V |
| Input Rise and Fall Time (t _r , t _f (Note 2) (Typical) (Except Schmitt Inputs) 'AC V _{IN} from 0.8V to 2.0V, V _{mea} | T Devices |
| from 0.8V to 2.0V | |
| V _{CC} @ 4.5V V _{CC} @ 5.5V | 10 ns/V 8 ns/V |

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

| a-s : | Parameter | 0. | 74 | AC | 54AC | 74AC | ation Dei | d of FIM | |
|-----------------|--------------------------------------|------------------------|-------------------------|-----------------------|-----------------------------------|---------------------------------|-----------|--|--|
| Symbol | | V _{CC} (V) | T _A = | + 25°C | T _A = -55°C to + 125°C | T _A = -40°C to +85°C | Units | | |
| | | | Тур | Typ Guaranteed Limits | | imits | 44 | 4 mm m m / 10 / 10 / 2 | |
| V _{IH} | Minimum High Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{IL} | Maximum Low Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{OH} | Minimum High Level Output Voltage | 3.0 4.5 5.5 | 2.99 4.49 5.49 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | V o | $I_{OUT} = -50 \mu\text{A}$ | |
| | en 0,1 en 0,8 e.k | 3.0 4.5 5.5 | 6.5 6.5 5.0 | 2.56 3.86 4.86 | 2.4 3.7 4.7 | 2.46 3.76 4.76 | Pulse W | *V _{IN} = V _{IL} or V _{IH} - 12 mA I _{OH} - 24 mA - 24 mA | |
| V _{OL} | Maximum Low Level Output Voltage | 3.0 4.5 5.5 | 0.002 0.001 0.001 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | VOL 10 | I _{OUT} = 50 μA | |
| | | 3.0 4.5 5.5 | | 0.36 0.36 0.36 | 0.50 0.50 0.50 | 0.44 0.44 0.44 | v V | $\begin{tabular}{ll} *V_{IN} &= V_{IL} \mbox{ or } V_{IH} \\ &= 12 \mbox{ mA} \\ I_{OL} &= 24 \mbox{ mA} \\ &= 24 \mbox{ mA} \\ \end{tabular}$ | |
| I _{IN} | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | ± 1.0 | μА | $V_I = V_{CC}$, GND | |

±50 mA

DC Characteristics for 'AC Family Devices (Continued)

| Symbol | Parameter | | 74 | AC | 54AC | 74AC | nge non | Light ten typestee 11 | |
|------------------|-------------------------------------|---------------------|------------------------|------------|-----------------------------------|-------|----------|------------------------------|--|
| | | V _{CC} (V) | T _A = +25°C | | T _A = -55°C to + 125°C | | | Conditions | |
| | | | Тур | gall() / | Guaranteed L | imits | ya) Inet | eO abolO tog if OG | |
| I _{OLD} | †Minimum Dynamic | 5.5 | (CV) eg | Pijo, irc | 50 | 75 | mA | V _{OLD} = 1.65V Max | |
| I _{OHD} | Output Current | 5.5 | managan. | Taling II. | -50 | -75 | mA | V _{OHD} = 3.85V Min | |
| Icc | Maximum Quiescent Supply Current | 5.5 | rusiagn | 8.0 | 160.0 | 80.0 | μА | $V_{IN} = V_{CC}$ or GND | |

^{*}All outputs loaded; thresholds on input associated with output under test.

AC Electrical Characteristics

| | | | Va A | 74AC | | 54 | AC | 74 | AC | | Electric . | |
|------------------|--------------------------------------|--------------------------|------------|---------------------|--------------|--|--------------|------------|--|-----|-------------|--|
| Symbol | Parameter | V _{CC} * (V) | | = +25° L = 50 pl | | $T_A = -55^{\circ}C$ to $+ 125^{\circ}C$ $C_L = 50 pF$ | | to + | $T_A = -40^{\circ}C$ $to +85^{\circ}C$ $C_L = 50 pF$ | | Fig. No. | |
| | and Devices | estivetr i | A (SILIZE | Min | Тур | Max | Min | Max | Min | Max | | |
| f _{max} | Maximum Clock Frequency | 3.3 5.0 | 90 140 | 125 175 | | 75 90 | | 75 125 | | MHz | 2-3 | |
| t _{PLH} | Propagation Delay Clock to Output | 3.3 5.0 | 4.0 3.0 | 7.0 5.5 | 12.5 9.0 | 1.0 1.0 | 15.0 11.0 | 3.0 2.5 | 14.0 10.0 | ns | 2-6 | |
| t _{PHL} | Propagation Delay Clock to Output | 3.3 5.0 | 4.0 3.0 | 7.0 5.0 | 13.0 10.0 | 1.0 1.0 | 16.0 11.5 | 3.5 2.5 | 14.5 11.0 | ns | 2-6 | |
| t _{PHL} | Propagation Delay MR to Output | 3.3 5.0 | 4.0 3.0 | 7.0 5.0 | 13.0 10.0 | 1.0 1.0 | 16.0 11.5 | 3.5 2.5 | 14.0 10.5 | ns | 2-6 | |

^{*}Voltage Range 3.3 is 3.3V ± 0.3 V Voltage Range 5.0 is 5.0V ± 0.5 V

AC Operating Requirements

| | gVac V also | | 74 | AC | 54AC | 74AC | teen | |
|------------------|---------------------------------------|--------------------------|--|------------|--|--|-------|-------------|
| Symbol | Parameter | V _{CC} * (V) | T _A = +25°C C _L = 50 pF | | T _A = -55°C to + 125°C C _L = 50 pF | $T_A = -40^{\circ}C$ $to +85^{\circ}C$ $C_L = 50 pF$ | Units | Fig. No. |
| | 80.7 | | Тур | 8 | Guaranteed Minimum | | | |
| ts | Setup Time, HIGH or LOW Data to CP | 3.3 5.0 | 3.5 2.5 | 5.5 4.0 | 8.0 5.0 | 6.0 4.5 | ns | 2-9 |
| t _h | Hold Time, HIGH or LOW Data to CP | 3.3 5.0 | -2.0 -1.0 | 0 | 0 1.0 | 0 1.0 | ns | 2-9 |
| t _w | Clock Pulse Width HIGH or LOW | 3.3 5.0 | 3.5 2.5 | 5.5 4.0 | 6.5 5.0 | 6.0 4.5 | ns | 2-6 |
| t _w | MR Pulse Width HIGH or LOW | 3.3 5.0 | 2.0 1.5 | 5.5 4.0 | 10.0 6.5 | 6.0 4.5 | ns | 2-6 |
| t _{rec} | Recovery Time MR to CP | 3.3 5.0 | 1.5 1.0 | 3.5 2.0 | 6.0 4.0 | 4.5 3.0 | ns | 2-9 |

^{*}Voltage Range 3.3 is 3.3V ± 0.3 V Voltage Range 5.0 is 5.0V ± 0.5 V

[†]Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC} . I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

Capacitance

| Symbol | Parameter | AC/ACT | Units | Conditions | |
|-----------------|----------------------------------|--------|--------|-----------------|--|
| | rarameter | Тур | Office | | |
| C _{IN} | Input Capacitance | 4.5 | pF | $V_{CC} = 5.0V$ | |
| C _{PD} | Power Dissipation Capacitance | 50.0 | pF | $V_{CC} = 5.0V$ | |



54AC/74AC280 • 54ACT/74ACT280 9-Bit Parity Generator/Checker

General Description

The 'AC/'ACT280 is a high-speed parity generator/checker that accepts nine bits of input data and detects whether an even or an odd number of these inputs is HIGH. If an even number of inputs is HIGH, the Sum Even output is HIGH. If an odd number is HIGH, the Sum Even output is LOW. The Sum Odd output is the complement of the Sum Even output.

Features

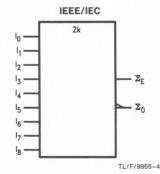
- 9-bit width for memory applications
- 'ACT280 has TTL-compatible inputs

The information for the 'ACT280 is Advanced Information only.

Ordering Code: See Section 5

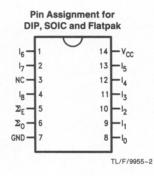
Logic Symbols

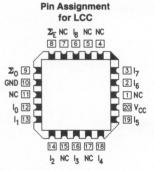
TL/F/9955-1



| Pin Names | Description |
|--------------------------------|--------------------|
| I ₀ -I ₈ | Data Inputs |
| Σ_{O} | Odd Parity Output |
| Σ_{E} | Even Parity Output |

Connection Diagrams





TL/F/9955-3

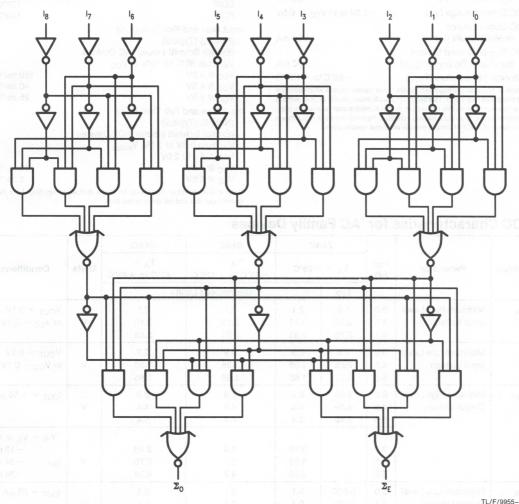
Truth Table its equipment modeli

| Number of | Outputs | | | | |
|---------------|---------|-----------------|--|--|--|
| HIGH Inputs | Σ Even | Σ Odd | | | |
| 0, 2, 4, 6, 8 | Н | (V) epaLoV nign | | | |
| 1, 3, 5, 7, 9 | L | y spailH notic | | | |

H = HIGH Voltage Level

L = LOW Voltage Level

Logic Diagram



TL/F/9955-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Office, Distributors for availabilit | y and specifications. |
|---|---------------------------------|
| Supply Voltage (V _{CC}) | -0.5V to $+7.0V$ |
| DC Input Diode Current (I _{IK}) | |
| $V_I = -0.5V$ | -20 mA |
| $V_I = V_{CC} + 0.5V$ | + 20 mA |
| DC Input Voltage (V _I) | -0.5 V to $V_{CC} + 0.5$ V |
| DC Output Diode Current (IOK) | |
| $V_0 = -0.5V$ | -20 mA |
| $V_O = V_{CC} + 0.5V$ | + 20 mA |
| DC Output Voltage (V _O) | -0.5 V to to $V_{CC} + 0.5$ V |
| DC Output Source | |
| or Sink Current (I _O) | ±50 mA |
| DC V _{CC} or Ground Current | |
| per Output Pin (I _{CC} or I _{GND}) | ±50 mA |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Storage Temperature (TSTG)

-65°C to +150°C

Recommended Operating Conditions

| Supply Voltage (V _{CC}) 'AC 'ACT | 2.0V to 6.0V 4.5V to 5.5V |
|--|-----------------------------------|
| Input Voltage (V _I) | 0V to V _{CC} |
| Output Voltage (V _O) | 0V to V _{CC} |
| | -40°C to +85°C -55°C to +125°C |
| Junction Temperature (T _J) CDIP PDIP | 175°C 140°C |
| Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'AC Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.0V V_{CC} @ 4.5V V_{CC} @ 5.5V | 150 ns/V 40 ns/V 25 ns/V |
| Input Rise and Fall Time (t _r , t _f) (Note 2) (Typical) (Except Schmitt Inputs) 'ACT Devices V _{IN} from 0.8V to 2.0V, V _{meas} from 0.8V to 2.0V | |
| V _{CC} @ 4.5V | 10 ns/V |

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

8 ns/V

V_{CC} @ 5.5V

DC Characteristics for 'AC Family Devices

| | | | 74 | AC | 54AC | 74AC | | | |
|-----------------|--------------------------------------|---------------------|-------------------------|----------------------|--|--|----------------|---|--|
| Symbol | Parameter | V _{CC} (V) | T _A = +25°C | | T _A = T _A = -55°C to + 125°C -40°C to +85°C | | Units | Conditions | |
| | | | Тур | | Guaranteed Lin | nits | committee of | | |
| V _{IH} | Minimum High Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{IL} | Maximum Low Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{OH} | Minimum High Level Output Voltage | 3.0 4.5 5.5 | 2.99 4.49 5.49 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | v | $I_{OUT} = -50 \mu\text{A}$ | |
| | 1 | 3.0 4.5 5.5 | | 2.56 3.86 4.86 | 2.4 3.7 4.7 | 2.46 3.76 4.76 | ٧ | $\label{eq:VIN} \begin{split} * V_{\text{IN}} &= V_{\text{IL}} \text{or} V_{\text{IH}} \\ &- 12 \text{mA} \\ I_{\text{OH}} &- 24 \text{mA} \\ &- 24 \text{mA} \end{split}$ | |
| V _{OL} | Maximum Low Level Output Voltage | 3.0 4.5 5.5 | 0.002 0.001 0.001 | 0.1 0.1 0.1 | 0.1 0.1 0.1 0.1 | 0.1 0.1 10.1 10 be 0.1 1 se crange | V e and had | I _{OUT} = 50 μA | |
| | | 3.0 4.5 5.5 | | 0.36 0.36 0.36 | 0.50 0.50 0.50 | 0.44 0.44 0.44 | v | $V_{IN} = V_{IL} \text{ or } V_{IH}$ 12 mA V_{IOL} 24 mA | |
| I _{IN} | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | ±1.0 | μΑ | $V_{I} = V_{CC}$, GND | |

DC Characteristics for 'AC Family Devices (Continued)

| Symbol | Parameter | | 74AC T _A = +25°C | | 54AC | 74AC | | |
|------------------|-------------------------------------|---------------------|-----------------------------|-----|----------------------------------|---------------------------------|-------|--|
| | | V _{CC} (V) | | | T _A = -55°C to +125°C | T _A = -40°C to +85°C | Units | Conditions |
| | | | Тур | 100 | Guaranteed Li | mits | | |
| I _{OLD} | †Minimum Dynamic | 5.5 | | yms | 50 | 75 | mA | V _{OLD} = 1.65V Max |
| IOHD | Output Current | 5.5 | | | -50 | −75 | mA | V _{OHD} = 3.85V Min |
| Icc | Maximum Quiescent Supply Current | 5.5 | gmod Ji | 8.0 | 160.0 | 80.0 | μА | V _{IN} = V _{CC} or GND |

^{*}All outputs loaded; thresholds on input associated with output under test.

AC Electrical Characteristics

| | | nanol | iG no | 74AC | 30 | 54 | AC | 74 | AC | rva oi | bol |
|------------------|---------------------------------------|-------------------|------------|---|--------------|------------|------|------------|--------------|-------------|-----|
| Symbol | Parameter | V _{CC} * | | $ \begin{array}{cccccccccccccccccccccccccccccccccccc$ | | to + 125°C | | 85°C | Units | Fig. No. | |
| | 30.010 | | Min | Тур | Max | Min | Max | Min | Max | A . 90 5A | |
| t _{PLH} | Propagation Delay I_n to Σ_E | 3.3 5.0 | 5.0 3.0 | 10.5 7.5 | 17.0 13.0 | 1 | 4,50 | 4.0 2.0 | 18.5 14.5 | ns | 2-5 |
| t _{PLH} | Propagation Delay I_n to Σ_O | 3.3 5.0 | 5.0 3.0 | 12.0 8.5 | 17.0 13.0 | 3 | | 4.0 2.0 | 18.5 14.5 | ns | 2-5 |

Capacitance

| Symbol | Parameter | AC/ACT | Units | Conditions | |
|-----------------|----------------------------------|--------|--------|-----------------|--|
| Oymbor | A SE OM A SE | Тур | Office | | |
| CIN | Input Capacitance | 4.5 | pF | $V_{CC} = 5.0V$ | |
| C _{PD} | Power Dissipation Capacitance | 75.0 | pF | $V_{CC} = 5.0V$ | |

[†]Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{1N} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC} - I_{CC} for 54AC @ 25°C is identical to 74 AC @ 25°C.





54AC/74AC283 • 54ACT/74ACT283 4-Bit Binary Full Adder with Fast Carry

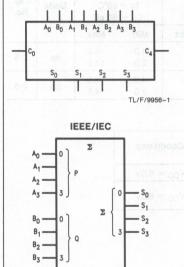
General Description

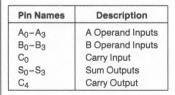
The 'AC/'ACT283 high-speed 4-bit binary full adder with internal carry lookahead accepts two 4-bit binary words (An-A₃, B₀-B₃) and a Carry input (C₀). It generates the binary Sum outputs (S0-S3) and the Carry output (C4) from the most significant bit. The 'AC/'ACT283 will operate with either active HIGH or active LOW operands (positive or negative logic).

Features

■ 'ACT283 has TTL-compatible inputs

Logic Symbols

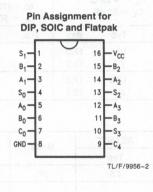


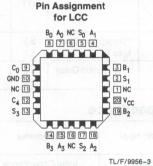


CO

TL/F/9956-4

Connection Diagrams







54AC/74AC299 • 54ACT/74ACT299 8-Input Universal Shift/Storage Register with Common Parallel I/O Pins

General Description

The 'AC/'ACT299 is an 8-bit universal shift/storage register with TRI-STATE® outputs. Four modes of operation are possible: hold (store), shift left, shift right and load data. The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Additional outputs are provided for flip-flops $\mathrm{Q}_0,\,\mathrm{Q}_7$ to allow easy serial cascading. A separate active LOW Master Reset is used to reset the register.

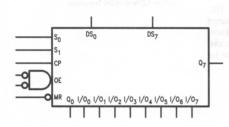
Features

- Common parallel I/O for reduced pin count
- Additional serial inputs and outputs for expansion
- Four operating modes: shift left, shift right, load and store
- TRI-STATE outputs for bus-oriented applications
- Outputs source/sink 24 mA
- 'ACT299 has TTL-compatible inputs

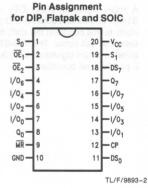
Ordering Code: See Section 5

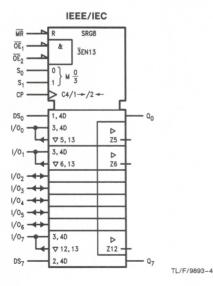
Logic Symbols

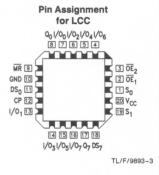
Connection Diagrams



TL/F/9893-1







4

| Pin Names | Description |
|---------------------------------------|-----------------------------------|
| CP | Clock Pulse Input |
| DS ₀ | Serial Data Input for Right Shift |
| DS ₇ | Serial Data Input for Left Shift |
| S ₀ , S ₁ | Mode Select Inputs |
| S ₀ , S ₁ MR | Asynchronous Master Reset |
| \overline{OE}_1 , \overline{OE}_2 | TRI-STATE Output Enable Inputs |
| 1/00-1/07 | Parallel Data Inputs or |
| | TRI-STATE Parallel Outputs |
| Q_0, Q_7 | Serial Outputs |

Functional Description

The 'AC/'ACT299 contains eight edge-triggered D-type flipflops and the interstage logic necessary to perform synchronous shift left, shift right, parallel load and hold operations. The type of operation is determined by S₀ and S₁, as shown in the Truth Table. All flip-flop outputs are brought out through TRI-STATE buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Qo and Q7 are also brought out on other pins for expansion in serial shifting of longer words.

A LOW signal on MR overrides the Select and CP inputs and resets the flip-flops. All other state changes are initiated by the rising edge of the clock. Inputs can change when the clock is in either state provided only that the recommended setup and hold times, relative to the rising edge of CP, are observed.

A HIGH signal on either \overline{OE}_1 or \overline{OE}_2 disables the TRI-STATE buffers and puts the I/O pins in the high impedance state. In this condition the shift, hold, load and reset operations can still occur. The TRI-STATE buffers are also disabled by HIGH signals on both So and S1 in preparation for a parallel load operation.

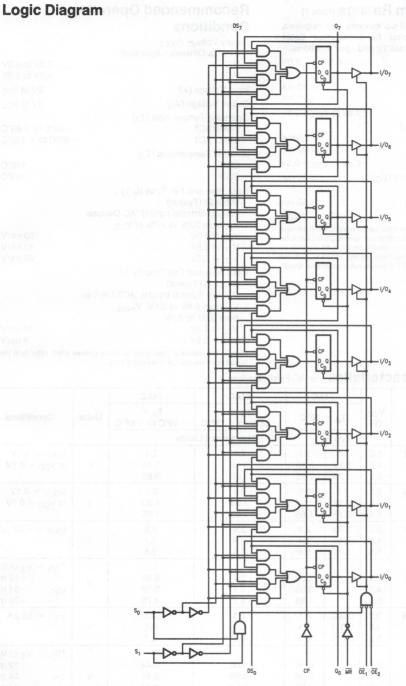
Truth Table

| CONTRACT. | Inp | outs | Sau He | Response | | | | |
|-----------|----------------|----------------|--------|--|--|--|--|--|
| MR | S ₁ | S ₀ | СР | Datus Para Team in the | | | | |
| L | X | × | X | Asynchronous Reset; Q ₀ -Q ₇ = LOW | | | | |
| Н | Н | Н | _ | Parallel Load; I/On → Q | | | | |
| Н | s E | Н | 5 | Shift Right; $DS_0 \rightarrow Q_0$, $Q_0 \rightarrow Q_1$, etc. | | | | |
| Н | н | L | ~ | Shift Left, DS ₇ \rightarrow Q ₇ , | | | | |
| Н | L | L | X | $Q_7 \rightarrow Q_6$, etc. Hold | | | | |

H = HIGH Voltage Level

= LOW Voltage Level = Immaterial

= LOW-to-HIGH Transition



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

TL/F/9893-5

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required. please contact the National Semiconductor Sales Office/Distributors for availability and specifications

| Office/ Distributors for availability a | ind specifications. |
|---|--|
| Supply Voltage (V _{CC}) | -0.5V to $+7.0V$ |
| DC Input Diode Current (I _{IK}) | |
| $V_1 = -0.5V$ | -20 mA |
| $V_I = V_{CC} + 0.5V$ | + 20 mA |
| DC Input Voltage (V _I) | $-0.5 \mbox{V}$ to $\mbox{V}_{\mbox{CC}} + 0.5 \mbox{V}$ |
| DC Output Diode Current (IOK) | |
| $V_0 = -0.5V$ | -20 mA |
| $V_O = V_{CC} + 0.5V$ | + 20 mA |
| DC Output Voltage (V _O) | $-0.5 \mbox{V}$ to $\mbox{V}_{\mbox{CC}} + 0.5 \mbox{V}$ |
| DC Output Source or Sink Current (IO) | ±50 mA |
| DC V _{CC} or Ground Current | |
| Per Output Pin (I _{CC} or I _{GND}) | ± 50 mA |
| Storage Temperature (T _{STG}) | -65°C to +150°C |
| | |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. Obviously the databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifi-

Recommended Operating Conditions

Supply Voltage (V_{CC})

| (Unless Otherwise Specified) | |
|---|-----------------------------------|
| 'AC | 2.0V to 6.0V |
| 'ACT | 4.5V to 5.0V |
| Input Voltage (V _I) | 0V to V _{CC} |
| Output Voltage (V _O) | 0V to V _{CC} |
| Operating Temperature (T _A) 74AC/ACT 54AC/ACT | -40°C to +85°C -55°C to +125°C |
| Junction Temperature (T _J) CDIP PDIP | 175°C 140°C |
| 1 1 D: 1 E 1 E 1 E 1 A 1 | |

Input Rise and Fall Time (tr, tf) (Note 2) (Typical) (Except Schmitt Inputs) 'AC Devices

VIN from 30% to 70% of VCC V_{CC} @ 3.0V

150 ns/V 40 ns/V V_{CC} @ 4.5V V_{CC} @ 5.5V 25 ns/V

Input Rise and Fall Time (tr, tf) (Note 2) (Typical) (Except Schmitt Inputs) 'ACT Devices V_{IN} from 0.8V to 2.0V, V_{meas} from 0.8V to 2.0V V_{CC} @ 4.5V 10 ns/V V_{CC} @ 5.5V 8 ns/V

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Electrical Characteristics For 'AC Family Devices

| | Parameter | | 74 | AC | 54AC | 74AC | | Conditions | |
|-----------------|--------------------------------------|------------------------|-------------------------|----------------------|----------------------------------|---------------------------------|-------|--|--|
| Symbol | | V _{CC} (V) | T _A = | 25°C | T _A = -55°C to +125°C | T _A = -40°C to +85°C | Units | | |
| | | 10/1-2-1 | Тур | | Guaranteed Lin | mits | | | |
| V _{IH} | Minimum High Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{IL} | Maximum Low Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{OH} | Minimum High Level Output Voltage | 3.0 4.5 5.5 | 2.99 4.49 5.49 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | ٧ | $I_{OUT} = -50 \mu\text{A}$ | |
| | | 3.0 4.5 5.5 | | 2.56 3.86 4.86 | 2.4 3.7 4.7 | 2.46 3.76 4.76 | V | $\begin{tabular}{ll} *V_{\text{IN}} &= V_{\text{IL}} \text{ or } V_{\text{IH}} \\ &- 12 \text{ mA} \\ I_{\text{OH}} &- 24 \text{ mA} \\ &- 24 \text{ mA} \\ \end{tabular}$ | |
| VoL | Maximum Low Level Output Voltage | 3.0 4.5 5.5 | 0.002 0.001 0.001 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | ٧ | $I_{OUT} = 50 \mu A$ | |
| | ave there there | 3.0 4.5 5.5 | 99 gs | 0.36 0.36 0.36 | 0.50 0.50 0.50 | 0.44 0.44 0.44 | V | * V _{IN} = V _{IL} or V _{IH} 12 mA $^{\rm IOH}$ 24 mA 24 mA | |
| I _{IN} | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | ±1.0 | μΑ | $V_{I} = V_{CC}$, GND | |
| loz | Maximum TRI-STATE Leakage Current | 5.5 | | ±0.5 | ± 10.0 | ±5.0 | μΑ | $V_{I}(OE) = V_{IL}, V_{IH}$ $V_{I} = V_{CC}, GND$ $V_{O} = V_{CC}, GND$ | |

DC Electrical Characteristics For 'AC Family Devices Application of the State of th

| | Parameter | | 74AC T _A = 25°C | | 54AC | 74AC | 14-14-14-14-14-14-14-14-14-14-14-14-14-1 | Conditions | |
|--------|-------------------------------------|------------------------|-------------------------------|--------|-----------------------------------|---------------------------------|--|--|--|
| Symbol | | V _{CC} (V) | | | T _A = -55°C to + 125°C | T _A = -40°C to +85°C | Units | | |
| .014 | | | Тур | 130 | Guaranteed Li | mits | | | |
| lold | †Minimum Dynamic | 5.5 | 51/3 · · · | Till . | 57 | 86 | mA | V _{OLD} = 1.65V Max | |
| IOHD | Output Current | 5.5 | | 05 | -50 | -75 | mA | V _{OHD} = 3.85V Min | |
| Icc | Maximum Quiescent Supply Current | 5.5 | 10 | 8.0 | 160 | 80 | μΑ | V _{IN} = V _{CC} or GND | |
| lozt | Maximum I/O Leakage Current | 5.5 | VI- | ±0.6 | ±11.0 | ±6.0 | μΑ | $V_{I}(OE) = V_{IL}, V_{IH}$ $V_{I} = V_{CC}, GND$ $V_{O} = V_{CC}, GND$ | |

^{*}All outputs loaded; threshold on input associated with output under test.

DC Electrical Characteristics For 'ACT Family Devices

| | Parameter | | | | 54ACT | 74ACT | 930 | Conditions | |
|------------------|--------------------------------------|------------------------|----------------|--------------|-----------------------------------|---------------------------------|---------|--|--|
| Symbol | | V _{CC} (V) | | | T _A = -55°C to + 125°C | T _A = -40°C to +85°C | Units | | |
| | Tables 18 | 0 | Тур | | Guaranteed L | imits | T HE | Santa Santa | |
| V _{IH} | Minimum High Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 2.0 | 2.0 2.0 | 2.0 2.0 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{IL} | Maximum Low Level Input Voltage | 3.0 4.5 | 1.5 1.5 | 0.8 0.8 | 0.8 0.8 | 0.8 | T picks | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{OH} | Minimum High Level | 4.5 5.5 | 4.49 5.49 | 4.4 5.4 | 4.4 5.4 | 4.4 5.4 | ٧ | $I_{OUT} = -50 \mu\text{A}$ | |
| | 20 19.5 1 | 4.5 5.5 | 0.0001 | 3.86 4.86 | 3.70 4.70 | 3.76 4.76 | ٧ | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IOH} = -24 \text{ mA}$ $V_{IOH} = -24 \text{ mA}$ | |
| V _{OL} | Maximum Low Level Output Voltage | 4.5 5.5 | 0.001 0.001 | 0.1 0.1 | 0.1 0.1 | 0.1 0.1 | V | $I_{OUT} = 50 \mu A$ | |
| | 7450 TA - 48 C | 4.5 5.5 | 0458 88 = A | 0.36 0.36 | 0.50 0.50 | 0.44 0.44 | V | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ | |
| I _{IN} | Maximum Input Leakage Current | 5.5 | 103 - 1 | ±0.1 | ±1.0 | ±1.0 | μΑ | $V_I = V_{CC}$, GND | |
| loz | Maximum TRI-STATE Leakage Current | 5.5 | | ±0.5 | ±10.0 | ±5.0 | μΑ | $V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}, GND$ | |
| Ісст | Maximum I _{CC} /Input | 5.5 | 0.6 | | 1.6 | 1.5 | mA | $V_I = V_{CC} - 2.1V$ | |
| I _{OLD} | †Minimum Dynamic | 5.5 | 13 | | 50 | 75 | mA | V _{OLD} = 1.65V Max | |
| IOHD | Output Current | 5.5 | 0.0 | 1 - 7 | -50 | -75 | mA | V _{OHD} = 3.85V Min | |
| Icc | Maximum Quiescent Supply Current | 5.5 | 4.0 | 8.0 | 160 | 80 | μА | V _{IN} = V _{CC} or GND | |
| lozt | Maximum I/O Leakage Current | 5.5 | 2.5 7.8 | ±0.6 | ±11.0 | ±6.0 | μΑ | $V_{I}(OE) = V_{IL}, V_{IH}$ $V_{I} = V_{CC}, GND$ $V_{O} = V_{CC}, GND$ | |

Note: I_{CC} limit for 54ACT @ 25°C is identical to 74ACT @ 25°C.

Capacitance

| Symbol | Parameter | AC/ACT Typ | Units | Conditions |
|-----------------|----------------------------------|---------------|-------|------------------------|
| C _{IN} | Input Capacitance | 4.5 | pF | V _{CC} = 5.5V |
| C _{PD} | Power Dissipation Capacitance | 170 | pF | $V_{CC} = 5.5V$ |

[†]Maximum test duration 20 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC} .

I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

^{*}All outputs loaded; thresholds on input associated with output under test.

[†]Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

| | | 0.45 | | 74AC | 3 | 54AC | | 74 | AC | | |
|------------------|--|--------------------------|--|--------------|--------------|--|--|--|--------------|----------|-------------|
| Symbol | Parameter | V _{CC} * (V) | T _A = +25°C C _L = 50 pF | | | T _A = -55°C to + 125°C C _L = 50 pF | | T _A = -40°C to +85°C C _L = 50 pF | | Units | Fig. No. |
| relat VBB | t = may Am | | Min | Тур | Max | Min | Max | Min | Max | NA TOTAL | Le sal |
| f _{max} | Maximum Input Frequency | 3.3 5.0 | 90 130 | 124 173 | | 70 80 | la l | 80 105 | inenso ju | MHz | 2-0 |
| t _{PLH} | Propagation Delay CP to Q ₀ or Q ₇ (Shift Left or Right) | 3.3 5.0 | 8.5 5.5 | 14.0 9.5 | 20.5 14.0 | 1.0 1.0 | 25.5 17.5 | 7.0 4.5 | 22.0 15.0 | ns | 2-6 |
| t _{PHL} | Propagation Delay CP to Q ₀ or Q ₇ (Shift Left or Right) | 3.3 5.0 | 8.5 5.5 | 14.5 10.0 | 21.5 14.5 | 1.0 | 26.5 18.0 | 7.0 5.0 | 23.0 | ns | 2-6 |
| t _{PLH} | Propagation Delay CP to I/On | 3.3 5.0 | 9.0 6.0 | 14.5 10.0 | 20.5 14.5 | 1.0 1.0 | 24.5 17.0 | 7.5 5.0 | 22.5 16.0 | ns | 2-6 |
| t _{PHL} | Propagation Delay CP to I/On | 3.3 5.0 | 10.0 6.5 | 16.0 11.0 | 23.0 16.0 | 1.0 1.0 | 26.5 18.5 | 8.5 6.0 | 24.5 17.5 | ns | 2-6 |
| t _{PHL} | Propagation Delay MR to Q ₀ or Q ₇ | 3.3 5.0 | 9.0 5.5 | 15.5 10.5 | 22.5 15.5 | 1.0 1.0 | 27.0 18.5 | 7.5 5.0 | 25.0 17.0 | ns | 2-6 |
| t _{PHL} | Propagation Delay MR to I/On | 3.3 5.0 | 9.0 5.5 | 15.0 10.0 | 21.5 15.0 | 1.0 | 26.5 18.0 | 7.5 5.0 | 24.0 16.5 | ns | 2-6 |
| t _{PZH} | Output Enable Time | 3.3 5.0 | 7.0 4.5 | 12.0 8.5 | 18.0 12.5 | 1.0 | 22.0 15.0 | 6.0 4.0 | 19.5 13.5 | ns | 2-7 |
| t _{PZL} | Output Enable Time | 3.3 5.0 | 7.0 5.0 | 12.5 8.0 | 18.0 12.5 | 1.0 | 23.5 16.0 | 6.0 4.0 | 20.5 14.0 | ns | 2-8 |
| t _{PHZ} | Output Disable Time | 3.3 5.0 | 6.5 3.5 | 13.0 9.5 | 18.5 14.0 | 1.0 1.0 | 22.5 17.0 | 5.5 3.0 | 19.5 15.0 | ns | 2-7 |
| t _{PLZ} | Output Disable Time | 3.3 5.0 | 5.5 3.5 | 11.5 8.0 | 17.0 12.5 | 1.0 1.0 | 21.5 16.0 | 4.5 2.0 | 19.0 13.5 | ns | 2-8 |

^{*}Voltage Range 3.3 is 3.3V \pm 0.3V. Voltage Range 5.0 is 5.0V \pm 0.5V.

AC Operating Requirements: See Section 2 for Waveforms

| V _{II} or V _{II} | = 14 Y 5 F F F F F F F F F F F F F F F F F F | | 74 | AC | 54AC | 74AC | | |
|------------------------------------|---|--------------------------|--------------|------------|--|--|-------|-------------|
| Symbol Paran | Parameter | V _{CC} * (V) | | | $T_{A} = -55^{\circ}C$ $to + 125^{\circ}C$ $C_{L} = 50 \text{ pF}$ | T _A = -40°C to +85°C C _L = 50 pF | Units | Fig. No. |
| | | | Тур | | Guaranteed Min | imum | | |
| ts | Setup Time, HIGH or LOW S ₀ or S ₁ to CP | 3.3 5.0 | 3.0 | 8.0 5.0 | 9.5 7.0 | 8.5 5.5 | ns | 2-9 |
| th | Hold Time, HIGH or LOW S ₀ or S ₁ to CP | 3.3 5.0 | -3.0 -1.5 | 0.5 1.0 | 2.0 2.5 | 0.5 1.0 | ns | 2-9 |
| ts | Setup Time, HIGH or LOW I/On to CP | 3.3 5.0 | 2.0 1.0 | 5.5 3.5 | 6.0 4.0 | 6.0 4.0 | ns | 2-9 |
| t _h | Hold Time, HIGH or LOW I/On to CP | 3.3 5.0 | -2.0 -1.0 | 0 1.0 | 1.5 2.0 | 1.0 | ns | 2-9 |
| ts | Setup Time, HIGH or LOW DS ₀ or DS ₇ to CP | 3.3 5.0 | 2.5 1.5 | 6.5 4.0 | 7.5 5.0 | 7.0 4.5 | ns | 2-9 |
| t _h | Hold Time, HIGH or LOW DS ₀ or DS ₇ to CP | 3.3 5.0 | -2.0 -1.0 | 0 | 1.5 1.5 | 0.5 1.0 | ns | 2-9 |
| t _w | CP Pulse Width, LOW | 3.3 5.0 | 3.5 2.0 | 4.5 3.5 | 5.5 5.0 | 5.0 3.5 | ns | 2-6 |
| t _w | MR Pulse Width, LOW | 3.3 5.0 | 4.0 2.0 | 4.5 3.5 | 5.5 5.0 | 5.0 3.5 | ns | 2-6 |
| t _{rec} | Recovery Time MR to CP | 3.3 5.0 | 0 0.5 | 1.5 1.5 | 2.5 2.5 | 1.5 1.5 | ns | 2-6 |

^{*}Voltage Range 3.3 is 3.3V \pm 0.3V *Voltage Range 5.0 is 5.0V \pm 0.5V

AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

| | Parameter | | 74AC | | | 54/ | ACT | 74 | ACT | | 100 |
|------------------|--|-------------------|--|------|-------|--|-------------|--|------|-------|-------------|
| Symbol | | V _{CC} * | $egin{aligned} \mathbf{T_A} = +25^{\circ}\mathbf{C} \\ \mathbf{C_L} = 50\ \mathbf{pF} \end{aligned}$ | | | T _A = -55°C to + 125°C C _L = 50 pF | | T _A = -40°C to +85°C C _L = 50 pF | | Units | Fig. No. |
| | | | Min | Тур | Max | Min | Max | Min | Max | 3 4 4 | 2 63 |
| f _{max} | Maximum Input Frequency | 5.0 | 120 | 170 | in si | 70 | sam e Ke | 110 | | MHz | 2-0 |
| t _{PLH} | Propagation Delay CP to Q ₀ or Q ₇ (Shift Left or Right) | 5.0 | 4.0 | 8.5 | 12.5 | 1.0 | 15.5 | 3.0 | 14.0 | ns | 2-6 |
| t _{PHL} | Propagation Delay CP to Q ₀ or Q ₇ (Shift Left or Right) | 5.0 | 4.0 | 9.0 | 13.5 | 1.0 | 16.0 | 3.5 | 15.0 | ns | 2-6 |
| t _{PLH} | Propagation Delay CP to I/On | 5.0 | 4.5 | 8.5 | 12.5 | 1.0 | 15.0 | 4.5 | 13.5 | ns | 2-6 |
| t _{PHL} | Propagation Delay CP to I/O _n | 5.0 | 5.0 | 9.5 | 15.0 | 1.0 | 18.0 | 4.5 | 16.5 | ns | 2-6 |
| t _{PHL} | Propagation Delay MR to Q ₀ or Q ₇ | 5.0 | 4.0 | 14.0 | 15.0 | 1.0 | 18.0 | 4.0 | 18.0 | ns | 2-6 |
| t _{PHL} | Propagation Delay MR to I/On | 5.0 | 4.0 | 13.0 | 14.5 | 1.0 | 17.5 | 3.5 | 17.5 | ns | 2-6 |
| t _{PZH} | Output Enable Time OE to I/On | 5.0 | 2.5 | 8.0 | 12.0 | 1.0 | 14.0 | 1.5 | 13.0 | ns | 2-7 |
| t _{PZL} | Output Enable Time OE to I/On | 5.0 | 2.0 | 8.0 | 12.0 | 1.0 | 14.5 | 1.5 | 13.5 | ns | 2-8 |
| t _{PHZ} | Output Disable Time OE to I/On | 2.5 | 2.0 | 8.5 | 12.5 | 1.0 | 14.5 | 2.0 | 13.5 | ns | 2-7 |
| t _{PLZ} | Output Disable Time OE to I/On | 2.0 | 2.5 | 8.0 | 11.5 | 1.0 | 14.0 | 2.0 | 12.5 | ns | 2-8 |

*Voltage Range 5.0 is 5.0V ± 0.5 V

AC Operating Requirements: See Section 2 for Waveforms

| | Parameter | | 74A | CT | 54ACT | 74ACT | | |
|------------------|--|-------------------|------|-----|--|--|-------|-------------|
| Symbol | | V _{CC} * | | | $T_A = -55^{\circ}C$ to $+ 125^{\circ}C$ $C_L = 50 pF$ | $T_A = -40^{\circ}C$ $to +85^{\circ}C$ $C_L = 50 pF$ | Units | Fig. No. |
| | Insmoves A nig | | Тур | | Guaranteed Min | imum | | |
| ts | Setup Time, HIGH or LOW S ₀ or S ₁ to CP | 5.0 | 2.0 | 5.0 | 6.5 | 5.5 | ns | 2-9 |
| t _h | Hold Time, HIGH or LOW S ₀ or S ₁ to CP | 5.0 | -2.0 | 1.0 | 1.5 | 1.0 | ns | 2-9 |
| ts | Setup Time, HIGH or LOW | 5.0 | 1.5 | 4.0 | 4.5 | 4.5 | ns | 2-9 |
| t _h | Hold Time, HIGH or LOW | 5.0 | -1.0 | 1.0 | 1.5 | 1.0 | ns | 2-9 |
| ts | Setup Time, HIGH or LOW DS ₀ or DS ₇ to CP | 5.0 | 1.5 | 4.5 | 5.5 | 5.0 | ns | 2-9 |
| t _h | Hold Time, HIGH or LOW DS ₀ or DS ₇ to CP | 5.0 | -1.0 | 1.0 | 1.5 | 1.0 | ns | 2-9 |
| t _w | CP Pulse Width HIGH or LOW | 5.0 | 2.0 | 4.0 | 5.0 | 4.5 | ns | 2-6 |
| t _w | MR Pulse Width, LOW | 5.0 | 2.0 | 3.5 | 5.0 | 3.5 | ns | 2-6 |
| t _{rec} | Recovery Time MR to CP | 5.0 | 0 | 1.5 | 1.5 | 1.5 | ns | 2-6 |

*Voltage Range 5.0 is 5.0V \pm 0.5V.



54ACT/74ACT323 8-Bit Universal Shift/Storage Register with Synchronous Reset and Common I/O Pins

General Description

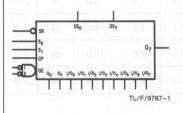
The 'ACT323 is an 8-bit universal shift/storage register with TRI-STATE® outputs. Parallel load inputs and flip-flop outputs are multiplexed to minimize pin count. Separate serial inputs and outputs are provided for Qo and Qo to allow easy cascading. Four operation modes are possible: hold (store), shift left, shift right and parallel load.

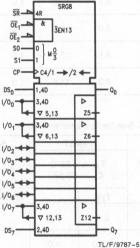
Features

- Common parallel I/O for reduced pin count
- Additional serial inputs and outputs for expansion
- Four operating modes: shift left, shift right, load and
- TRI-STATE outputs for bus-oriented applications
- Outputs source/sink 24 mA
- TTL-compatible inputs

Ordering Code: See Section 5

Logic Symbols





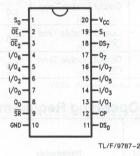
| Pin Name | Description |
|--|--|
| $\begin{array}{c} CP \\ DS_0 \\ DS_7 \\ S_0, S_1 \\ \overline{SR} \\ \overline{OE}_1, \overline{OE}_2 \\ I/O_0 \text{-} I/O_7 \end{array}$ | Clock Pulse Input Serial Data Input for Right Shift Serial Data Input for Left Shift Mode Select Inputs Synchronous Reset Input TRI-STATE Output Enable Inputs Multiplexed Parallel Data Inputs or TRI-STATE Parallel Data Outputs |

Serial Outputs

Q0, Q7

Connection Diagrams

Pin Assignment for DIP. SOIC and Flatpak



for LCC 00 1/00 1/02 1/04 1/06 8 7 6 5 4 SR 9 3 0E2 GND 10 2 0E, DS₀ 11 1 So CP 12 20 V_{CC} 1/0, 13 19 S 14 15 16 17 18 1/03 1/05 1/07 Q7 DS7 TL/F/9787-3

Pin Assignment

Functional Description

The 'ACT323 contains eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous reset, shift left, shift right, parallel load and hold operations. The type of operation is determined by S_0 and S_1 as shown in the Mode Select Table. All flip-flop outputs are brought out through TRI-STATE buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q_0 and Q_7 are also brought out on other pins for expansion in serial shifting of longer words.

A LOW signal on SR overrides the Select inputs and allows the flip-flops to be reset by the next rising edge of CP.

Mode Select Table

| Inputs | | | | Response |
|--------|----------------|----------------|---------------|--|
| SR | S ₁ | S ₀ | CP | 1100porido |
| L | X | X | _ | Synchronous Reset; Q ₀ -Q ₇ = LOW |
| Н | Н | Н | _ | Parallel Load; I/O _n → Q _n |
| Н | L | Н | _ | Shift Right; $DS_0 \rightarrow Q_0$, $Q_0 \rightarrow Q_1$, etc. |
| Н | Н | L | $\overline{}$ | Shift Left; $DS_7 \rightarrow Q_7, Q_7 \rightarrow Q_6$, etc. |
| Н | L | L | X | Hold |

H = HIGH Voltage Level

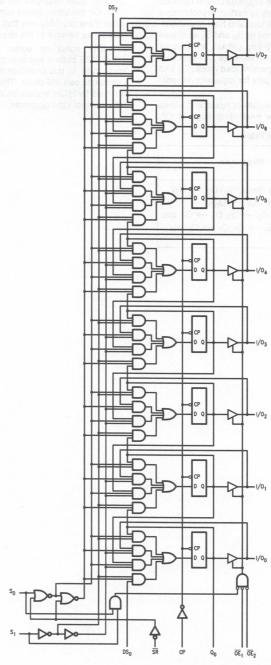
All other state changes are also initiated by the LOW-to-HIGH CP transition. Inputs can change when the clock is in either state provided only that the recommended setup and hold times, relative to the rising edge of CP, are observed. A HIGH signal on either $\overline{\text{OE}}_1$ or $\overline{\text{OE}}_2$ disables the TRI-STATE buffers and puts the I/O pins in the high impedance state. In this condition the shift, load, hold and reset operations can still occur. The TRI-STATE buffers are also disabled by HIGH signals on both S_0 and S_1 in preparation for a parallel load operation.

L = LOW Voltage Level

X = Immaterial

__ = LOW-to-HIGH Clock Transition

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})

Sink Current (IO)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| DC Input Diode Current (I _{IK}) | |
|---|---------------------------------|
| $V_{I} = -0.5V$ | -20 mA |
| $V_I = V_{CC} + 0.5V$ | + 20 mA |
| DC Input Voltage (V _I) | -0.5 V to V_{CC} + 0.5 V |
| DC Output Diode Current (IOK) | |
| $V_0 = -0.5V$ | -20 mA |
| $V_O = V_{CC} + 0.5V$ | +20 mA |
| DC Output Voltage (V _O) | -0.5V to V _{CC} + 0.5V |
| DC Output Source or | |

DC V_{CC} or Ground Current
Per Output Pin (I_{CC} or I_{GND})

\$\delta 50 \text{ mA}\$

Storage Temperature (I_{STG})

-65°C to +150°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

Recommended Operating Conditions

| Supply Voltage (V _{CC}) 'AC | 2.0V to 6.0V |
|---|-----------------------------------|
| ACT | 4.5V to 5.5V |
| Input Voltage (V _I) | 0V to V _{CC} |
| Output Voltage (V _O) | 0V to V _{CC} |
| Operating Temperature (T _A) 74AC/ACT 54AC/ACT | -40°C to +85°C -55°C to +125°C |
| Junction Temperature (T _J) CDIP PDIP | 175°C 140°C |
| Input Rise and Fall Time (t_r, t_f) (Note 2) (Typical) (Except Schmitt Inputs) 'AC Devices | |
| V _{IN} from 30% to 70% of V _{CC} V _{CC} @ 3.0V | 150 ns/V |
| Vcc @ 4.5V | 40 ns/V |
| V _{CC} @ 5.5V | 25 ns/V |
| Input Rise and Fall Time (t _r , t _f) | |
| (Note 2) (Typical) | |
| (Except Schmitt Inputs) 'ACT Devices V _{IN} from 0.8V to 2.0V, V _{meas} | |
| V _{CC} @ 4.5V | 10 ns/V |
| V _{CC} @ 5.5V | 8 ns/V |
| | |

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Electrical Characteristics For 'ACT Family Devices

-0.5V to +7.0V

±50 mA

| | TOART | | 74ACT | | 54ACT | 74ACT | | | |
|------------------|--------------------------------------|------------------------|------------------|--------------|-------------------------------------|---------------------------------|---------------|---|--|
| Symbol | Parameter | V _{CC} (V) | T _A = | + 25°C | T _A = -55°C to +125°C | T _A = -40°C to +85°C | Units | Conditions | |
| | 70 02 - 10 | | Тур | | Guaranteed Li | mits | \$15 ets etc. | lodmys | |
| V _{IH} | Minimum High Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 2.0 | 2.0 2.0 | 2.0 2.0 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| VIL | Maximum Low Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 0.8 0.8 | 0.8 0.8 | 0.8 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{OH} | Minimum High Level Output Voltage | 4.5 5.5 | 4.49 5.49 | 4.4 5.4 | 4.4 5.4 | 4.4 5.4 | V | $I_{OUT} = -50 \mu\text{A}$ | |
| | an 3.4 | 4.5 5.5 | 4.5 | 3.86 4.86 | 3.70 4.70 | 3.76 4.76 | V | $ ^*V_{\text{IN}} = V_{\text{IL}} \text{ or } V_{\text{IH}} $ | |
| V _{OL} | Maximum Low Level Output Voltage | 4.5 5.5 | 0.001 0.001 | 0.1 0.1 | 0.1 0.1 | 0.1 0.1 | ٧ | I _{OUT} = 50 μA | |
| | an 3.7 | 4.5 5.5 | 0.8 | 0.36 0.36 | 0.50 0.50 | 0.44 0.44 | V | $\label{eq:VIN} \begin{split} ^*\text{V}_{\text{IN}} &= \text{V}_{\text{IL}} \text{or} \text{V}_{\text{IH}} \\ \text{I}_{\text{OL}} & -24 \text{mA} \\ & -24 \text{mA} \end{split}$ | |
| I _{IN} | Maximum Input Leakage Current | 5.5 | 0.1 | ±0.1 | ± 1.0 | ±1.0 | μА | V _I = V _{CC} , GND | |
| loz | Maximum TRI-STATE Current | 5.5 | 0.0 | ±0.5 | ±10.0 | ±5.0 | μА | $V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}, GND$ | |
| lozt | Maximum I/O Leakage Current | 5.5 | | ±0.6 | ±11.0 | ±6.0 | μА | $V_{I/O} = V_{CC}$ or GND $V_{IN} = V_{IH}$, V_{IL} | |
| ICCT | Maximum I _{CC} /Input | 5.5 | 0.6 | | 1.6 | 1.5 | mA | $V_I = V_{CC} - 2.1V$ | |
| I _{OLD} | †Minimum Dynamic Output | 5.5 | aneatter | (05) | 50 | 75 | mA | V _{OLD} = 1.65V Max | |
| IOHD | Current | 5.5 | Vir z = | | -50 | -75 | mA | V _{OHD} = 3.85V Min | |
| Icc | Maximum Quiescent Supply Current | 5.5 | V07 = | 8.0 | 160 | 0 80 O no re | μА | V _{IN} = V _{CC} or GND (Note 3) | |

*All outputs loaded; thresholds on input associated with output under test. †Maximum test duration 2.0 ms, one output loaded at a time.

Note 3; I_{CC} for 54ACT is identical to 74ACT @ 25°C.

AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

| | (元) | | 74ACT | | 54ACT | | 74ACT | | E BBOY VI | GUE . | |
|------------------|---|-----------------------|---|------|--------------------------|---|-------|--|---|----------|-------------|
| Symbol | Parameter (AT) | V _{CC} * (V) | $T_A = 25^{\circ}C$ $C_L = 50 \text{ pF}$ | | Ain Os Am OS Valor | $T_A = -55^{\circ}C$ to $+125^{\circ}C$ $C_L = 50 pF$ | | $T_A = -40^{\circ}C$ to $+85^{\circ}C$ $C_L = 50 pF$ | | Units | Fig. No. |
| | 010103 - | | Min | Тур | Max | Min | Max | Min | Max | i neonic | 60 |
| f _{max} | Maximum Input Frequency | 5.0 | 120 | 125 | A 10 00 | 95 | | 110 | VA Section of the section of the sec | MHz | 2-3 |
| t _{PLH} | Propagation Delay CP to Q ₀ or Q ₇ | 5.0 | 5.0 | 9.0 | 12.5 | 1.0 | 16.5 | 4.0 | 14.0 | ns | 2-6 |
| t _{PHL} | Propagation Delay CP to Q ₀ or Q ₇ | 5.0 | 5.0 | 9.0 | 13.5 | 1.0 | 17.0 | 4.5 | 15.0 | ns | 2-6 |
| t _{PLH} | Propagation Delay CP to I/O _n | 5.0 | 5.0 | 8.5 | 12.5 | 1.0 | 16.5 | 4.5 | 14.5 | ns | 2-6 |
| t _{PHL} | Propagation Delay CP to I/On | 5.0 | 6.0 | 10.0 | 14.5 | 1.0 | 18.0 | 5.0 | 16.0 | ns | 2-6 |
| t _{PZH} | Output Enable Time | 5.0 | 3.5 | 7.5 | 11.0 | 1.0 | 15.0 | 3.0 | 12.5 | ns | 2-7 |
| t _{PZL} | Output Enable Time | 5.0 | 3.5 | 7.5 | 11.5 | 1.0 | 15.5 | 3.0 | 13.0 | ns | 2-8 |
| t _{PHZ} | Output Disable Time | 5.0 | 4.0 | 8.5 | 12.5 | 1.0 | 15.5 | 3.0 | 13.5 | ns | 2-7 |
| t _{PLZ} | Output Disable Time | 5.0 | 3.0 | 8.0 | 11.5 | 1.0 | 15.0 | 2.5 | 12.5 | ns | 2-8 |

^{*}Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

| | | | 744 | CT | 54ACT | 74ACT | | |
|----------------|---|-------------------|--|-----|---|---|---------|-------------|
| Symbol | Parameter | V _{CC} * | $\begin{aligned} T_{\text{A}} &= 25^{\circ}\text{C} \\ C_{\text{L}} &= 50\text{pF} \\ V_{\text{CC}} &= +5.0\text{V} \end{aligned}$ | | $\begin{aligned} \mathbf{T_A} &= -55^{\circ}\mathbf{C} \\ & \text{to} + 125^{\circ}\mathbf{C} \\ \mathbf{C_L} &= 50 \text{ pF} \\ \mathbf{V_{CC}} &= +5.0 \mathbf{V} \end{aligned}$ | $T_A = -40^{\circ}C$ $to +85^{\circ}C$ $C_L = 50 \text{ pF}$ $V_{CC} = +5.0V$ | Units | Fig. No. |
| Vita | 33A 22 | | Тур | | Guaranteed Min | imum | Visioni | FILE |
| t _s | Setup Time, HIGH or LOW S ₀ or S ₁ to CP | 5.0 | 2.0 | 5.0 | 6.0 | 5.0 | ns | 2-9 |
| th | Hold Time, HIGH or LOW S ₀ or S ₁ to CP | 5.0 | 0 | 1.5 | 1.5 | 1.5 | ns | 2-9 |
| t _s | Setup Time, HIGH or LOW I/On, DS ₀ , DS ₇ to CP | 5.0 | 1.0 | 4.0 | 4.5 | 4.5 | ns | 2-9 |
| th Ago | Hold Time, HIGH or LOW I/On, DS ₀ , DS ₇ to CP | 5.0 | 0 | 1.0 | 1.0 | 1.0 | ns | 2-9 |
| t _s | Setup Time, HIGH or LOW SR to CP | 5.0 | 1.0 | 2.5 | 3.0 | 2.5 | ns | 2-9 |
| t _h | Hold Time, HIGH or LOW SR to CP | 5.0 | 0 | 1.0 | 1.0 | 1.0 | ns | 2-9 |
| t _w | CP Pulse Width HIGH or LOW | 5.0 | 2.0 | 4.0 | 5.0 | 4.5 | ns | 2-6 |

^{*}Voltage Range 5.0 is 5.0V \pm 0.5V

Capacitance

| Symbol | Parameter | AC/ACT | Units | Conditions |
|-----------------|-------------------------------|--------|-------|-----------------|
| Oymbo. | | Тур | Onno | Contactions |
| C _{IN} | Input Capacitance | 4.5 | pF | $V_{CC} = 5.0V$ |
| C _{PD} | Power Dissipation Capacitance | 170 | pF | $V_{CC} = 5.0V$ |



54AC/74AC350 • 54ACT/74ACT350 4-Bit Shifter with TRI-STATE® Outputs

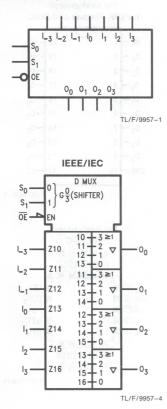
General Description

The 'AC/'ACT350 is a specialized multiplexer that accepts a 4-bit word and shifts it 0, 1, 2 or 3 places, as determined by two Select (S_0 , S_1) inputs. For expansion to longer words, three linking inputs are provided for lower-order bits; thus two packages can shift an 8-bit word, four packages a 16-bit word, etc. Shifting by more than three places is accomplished by paralleling the TRI-STATE outputs of different packages and using the Output Enable (\overline{OE}) inputs as a third Select level. With appropriate interconnections, the 'AC/'ACT350 can perform zero-backfill, sign-extend or endaround (barrel) shift functions.

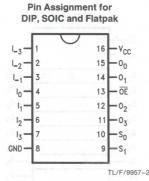
Features

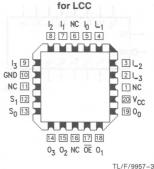
- Linking inputs for word expansion
- TRI-STATE ouputs for extending shift range
- 'ACT350 has TTL-compatible inputs

Logic Symbols



Connection Diagrams





Pin Assignment

TL/F/9957-3

| Pin Names | Description |
|---------------------------------|----------------------------------|
| S ₀ , S ₁ | Select Inputs |
| I_3-I3 | Data Inputs |
| ŌĒ | Output Enable Input (Active LOW) |
| 00-03 | TRI-STATE Outputs |



54AC/74AC373 • 54ACT/74ACT373 Octal Transparent Latch with TRI-STATE® Outputs

General Description

The 'AC/'ACT373 consists of eight latches with TRI-STATE outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup time is latched. Data appears on the bus when the Output Enable $(\overline{\text{OE}})$ is LOW. When $\overline{\text{OE}}$ is HIGH, the bus output is in the high impedance state.

Features

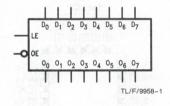
- Eight latches in a single package
- TRI-STATE outputs for bus interfacing
- Outputs source/sink 24 mA
- 'ACT373 has TTL-compatible inputs

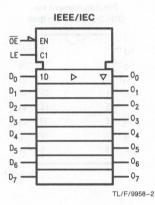
Ordering Code: See Section 5

Logic Symbols

Connection Diagrams

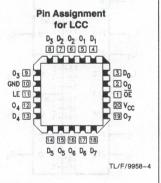
Pin Assignment





| OE 1 | 20 | -v _{cc} |
|--------------------|----|------------------|
| 00-2 | 19 | -07 |
| $D_0 - 3$ | 18 | -D ₇ |
| D ₁ -4 | 17 | -D ₆ |
| 01-5 | 16 | -06 |
| 02-6 | 15 | -05 |
| 02-7 | 14 | -D ₅ |
| D ₃ - 8 | 13 | -D ₄ |
| 03 9 | 12 | -04 |
| ND - 10 | 11 | -LE |

| Pin Names | Description |
|--------------------------------|-------------------------|
| D ₀ -D ₇ | Data Inputs |
| LE | Latch Enable Input |
| ŌĒ | Output Enable Input |
| 00-07 | TRI-STATE Latch Outputs |



Functional Description

The 'AC/'ACT373 contains eight D-type latches with TRI-STATE standard outputs. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE standard outputs are controlled by the Output Enable (\overline{OE}) input. When \overline{OE} is LOW, the standard outputs are in the 2-state mode. When \overline{OE} is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

Truth Table

| A Selection | Inputs | o bumbaga soc A decokuri or | Outputs | |
|-------------|-------------|--------------------------------|-------------------|--|
| LE | ŌĒ | Dn | On | |
| X | 02 Vd 0 - H | X | Z | |
| Н | L | L) The | 100 sport 1000 00 | |
| Н | L | Н | Н | |
| L | L | X | 00 | |

H = HIGH Voltage Level

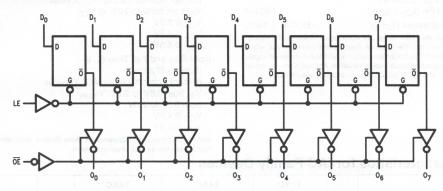
L = LOW Voltage Level

Z = High Impedance

X = Immaterial

O₀ = Previous O₀ before HIGH to Low transition of Latch Enable

Logic Diagram



TL/F/9958-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

-0.5V to +7.0V

±50 mA

±50 mA

| DC Input Diode Current (I _{IK}) | |
|---|-----------------------------------|
| $V_1 = -0.5V$ | -20 mA |
| $V_I = V_{CC} + 0.5V$ | + 20 mA |
| DC Input Voltage (V _I) | $-0.5V$ to $V_{CC} + 0.5V$ |
| DC Output Diode Current (IOK) | |
| $V_0 = -0.5V$ | -20 mA |
| $V_O = V_{CC} + 0.5V$ | + 20 mA |
| DC Output Voltage (V _O) | -0.5 V to to V_{CC} + 0.5 V |
| DC Output Source | |

or Sink Current (IO) DC V_{CC} or Ground Current

Supply Voltage (V_{CC})

per Output Pin (I_{CC} or I_{GND}) Storage Temperature (TSTG)

-65°C to +150°C Note 1: Absolute maximum ratings are those values beyond which damage

to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

Recommended Operating Conditions

| Supply Voltage (V _{CC}) 'AC 'ACT | 4.5V to 5.5V |
|--|----------------|
| Input Voltage (V _I) | 01/+01/ |
| Output Voltage (V _O) | |
| Operating Temperature (T _A) 74AC/ACT | |
| Juliculott rettiperature (11) | 175°C 140°C |

Input Rise and Fall Time (tr, tf)

(Note 2) (Typical)

(Except Schmitt Inputs) 'AC Devices

VIN from 30% to 70% of VCC VCC @ 3.0V

150 ns/V V_{CC} @ 4.5V 40 ns/V V_{CC} @ 5.5V 25 ns/V

Input Rise and Fall Time (tr, tf)

(Note 2) (Typical)

(Except Schmitt Inputs) 'ACT Devices VIN from 0.8V to 2.0V, Vmeas

from 0.8V to 2.0V

typical input rise and fall times noted here.

V_{CC} @ 4.5V

10 ns/V V_{CC} @ 5.5V 8 ns/V Note 2: See individual datasheets for those devices which differ from the

DC Characteristics for 'AC Family Devices

| Symbol | | | | | 54AC | 74AC | | Conditions | |
|-----------------|----------------------------------|------------------------|-------|------|----------------------------------|---------------------------------|-------|---------------------------------------|--|
| | Parameter | V _{CC} (V) | | | T _A = -55°C to +125°C | T _A = -40°C to +85°C | Units | | |
| | | | Тур | | Guaranteed L | imits | | | |
| VIH | Minimum High Level | 3.0 | 1.5 | 2.1 | 2.1 | 2.1 | | V _{OUT} = 0.1V | |
| | Input Voltage | 4.5 | 2.25 | 3.15 | 3.15 | 3.15 | V | or V _{CC} - 0.1V | |
| | | 5.5 | 2.75 | 3.85 | 3.85 | 3.85 | | | |
| V _{IL} | Maximum Low Level | 3.0 | 1.5 | 0.9 | 0.9 | 0.9 | | $V_{OUT} = 0.1V$ | |
| | Input Voltage | 4.5 | 2.25 | 1.35 | 1.35 | 1.35 | V | or V _{CC} - 0.1V | |
| | , | 5.5 | 2.75 | 1.65 | 1.65 | 1.65 | | | |
| V _{OH} | Minimum High Level | 3.0 | 2.99 | 2.9 | 2.9 | 2.9 | | $I_{OUT} = -50 \mu A$ | |
| | Output Voltage | 4.5 | 4.49 | 4.4 | 4.4 | 4.4 | V | | |
| | | 5.5 | 5.49 | 5.4 | 5.4 | 5.4 | | | |
| | | | | | | | | $*V_{IN} = V_{IL} \text{ or } V_{II}$ | |
| | | 3.0 | | 2.56 | 2.4 | 2.46 | | -12 m | |
| | | 4.5 | | 3.86 | 3.7 | 3.76 | V | I _{OH} -24 m. | |
| | | 5.5 | | 4.86 | 4.7 | 4.76 | | −24 m | |
| V _{OL} | Maximum Low Level | 3.0 | 0.002 | 0.1 | 0.1 | 0.1 | | $I_{OUT} = 50 \mu A$ | |
| | Output Voltage | 4.5 | 0.001 | 0.1 | 0.1 | 0.1 | V | | |
| | | 5.5 | 0.001 | 0.1 | 0.1 | 0.1 | | | |
| | | | | | | | | $*V_{IN} = V_{IL} \text{ or } V_{I}$ | |
| | | 3.0 | | 0.36 | 0.50 | 0.44 | | 12 m | |
| | | 4.5 | | 0.36 | 0.50 | 0.44 | V | I _{OL} 24 m | |
| | | 5.5 | | 0.36 | 0.50 | 0.44 | | 24 m | |
| I _{IN} | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | ±1.0 | μΑ | $V_I = V_{CC}$, GND | |

DC Characteristics for 'AC Family Devices (Continued)

| Symbol | Parameter | | 74 | AC | 54AC | 74AC | | | |
|--------|-------------------------------------|---------------------|------------------------|------|----------------------------------|---------------------------------|-------|--|--|
| | | V _{CC} (V) | T _A = +25°C | | T _A = -55°C to +125°C | T _A = -40°C to +85°C | Units | Conditions | |
| | | | Typ Guaranteed Limits | | | | | | |
| loz | Maximum TRI-STATE® Current | 5.5 | | ±0.5 | ±10.0 | ± 5.0 | μА | V_{I} (OE) = V_{IL} , V_{IH} $V_{I} = V_{CC}$, GND $V_{O} = V_{CC}$, GND | |
| IOLD | †Minimum Dynamic | 5.5 | | | 50 | 75 | mA | V _{OLD} = 1.65V Max | |
| IOHD | Output Current | 5.5 | | | -50 | -75 | mA | V _{OHD} = 3.85V Min | |
| Icc | Maximum Quiescent Supply Current | 5.5 | | 8.0 | 160.0 | 80.0 | μА | V _{IN} = V _{CC} or GND | |

^{*}All outputs loaded; thresholds on input associated with output under test.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC} . I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

| | 8.5 1.0 12.5 a | 1 | 74/ | ACT | 54ACT | 74ACT | | | |
|------------------|-------------------------------------|------------------------|------------------------|--------------|----------------------------------|---------------------------------|---------|---|--|
| Symbol | Parameter | V _{CC} (V) | T _A = +25°C | | T _A = -55°C to +125°C | T _A = -40°C to +85°C | Units | Conditions | |
| | | | Тур | | Guaranteed L | imits | 05 Y0.8 | Voltage Rungs Düne Voltage Rungs 5:0 is 5 | |
| V _{IH} | Minimum High Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 2.0 2.0 | 2.0 2.0 | 2.0 2.0 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{IL} | Maximum Low Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 0.8 | 0.8 0.8 | 0.8 0.8 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{OH} | Minimum High Level Output Voltage | 4.5 5.5 | 4.49 5.49 | 4.4 5.4 | 4.4 5.4 | 4.4 5.4 | ٧ | $I_{OUT} = -50 \mu\text{A}$ | |
| 9-S | 0.3 an 0.3 a.a. | 4.5 5.5 | Guan | 3.86 4.86 | 3.70 4.70 | 3.76 4.76 | ٧ | $\label{eq:VIN} \begin{array}{ll} ^{*}\text{V}_{\text{IN}} = \text{V}_{\text{IL}} \text{or} \text{V}_{\text{IH}} \\ -24 \text{mA} \\ -24 \text{mA} \end{array}$ | |
| V _{OL} | Maximum Low Level Output Voltage | 4.5 5.5 | 0.001 0.001 | 0.1 0.1 | 0.1 0.1 | 0.1 0.1 | ٧ | $I_{OUT} = 50 \mu A$ | |
| | an dia | 4.5 5.5 | | 0.36 0.36 | 0.50 0.50 | 0.44 0.44 | V | $^*V_{IN} = V_{IL} \text{ or } V_{IH}$ I_{OL} $^{24} \text{ mA}$ $^{24} \text{ mA}$ | |
| I _{IN} | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | ±1.0 | μΑ | $V_I = V_{CC}$, GND | |
| loz | Maximum TRI-STATE® Current | 5.5 | | ±0.5 | ±10.0 | ±5.0 | μА | $V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}, GND$ | |
| ICCT | Maximum I _{CC} /Input | 5.5 | 0.6 | | 1.6 | 1.5 | mA | $V_{I} = V_{CC} - 2.1V$ | |
| I _{OLD} | †Minimum Dynamic | 5.5 | | | 50 | 75 | mA | V _{OLD} = 1.65V Max | |
| IOHD | Output Current | | | | -50 | −75 | mA | V _{OHD} = 3.85V Min | |
| Icc | Maximum Quiescent Supply Current | 5.5 | | 8.0 | 160.0 | 80.0 | μА | $V_{IN} = V_{CC}$ or GND | |

^{*}All outputs loaded; thresholds on input associated with output under test.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

[†]Maximum test duration 2.0 ms, one output loaded at a time.

[†]Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics

| Symbol | Parameter | DAM | 74AC T _A = +25°C C _L = 50 pF | | | 54 | AC | 74 | AC | | |
|------------------|---|-------------------|---|-------------|--------------|--|--------------|--|--------------|-------|------|
| | | V _{CC} * | | | | T _A = -55°C to + 125°C C _L = 50 pF | | $T_A = -40^{\circ}C$ to $+85^{\circ}C$ $C_L = 50 pF$ | | Units | Fig. |
| | | | Min | Тур | Max | Min | Max | Min | Max | | |
| t _{PLH} | Propagation Delay D _n to O _n | 3.3 5.0 | 1.5 1.5 | 10.0 7.0 | 13.5 9.5 | 1.0 1.0 | 16.5 11.5 | 1.5 1.5 | 15.0 10.5 | ns | 2-5 |
| t _{PHL} | Propagation Delay D _n to O _n | 3.3 5.0 | 1.5 1.5 | 9.5 7.0 | 13.0 9.5 | 1.0 1.0 | 16.0 11.5 | 1.5 1.5 | 14.5 10.5 | ns | 2-5 |
| t _{PLH} | Propagation Delay LE to O _n | 3.3 5.0 | 1.5 1.5 | 10.0 7.5 | 13.5 9.5 | 1.0 1.0 | 16.5 12.0 | 1.5 1.5 | 15.0 10.5 | ns | 2-6 |
| t _{PHL} | Propagation Delay LE to O _n | 3.3 5.0 | 1.5 1.5 | 9.5 7.0 | 12.5 9.5 | 1.0 | 15.0 11.0 | 1.5 1.5 | 14.0 10.5 | ns | 2-6 |
| t _{PZH} | Output Enable Time | 3.3 5.0 | 1.5 1.5 | 9.0 7.0 | 11.5 8.5 | 1.0 1.0 | 14.0 10.5 | 1.0 1.0 | 13.0 9.5 | ns | 2-7 |
| t _{PZL} | Output Enable Time | 3.3 5.0 | 1.5 1.5 | 8.5 6.5 | 11.5 8.5 | 1.0 1.0 | 13.5 10.0 | 1.0 1.0 | 13.0 9.5 | ns | 2-8 |
| t _{PHZ} | Output Disable Time | 3.3 5.0 | 1.5 1.5 | 10.0 8.0 | 12.5 11.0 | 1.0 1.0 | 16.0 13.5 | 1.0 1.0 | 14.5 12.5 | ns | 2-7 |
| t _{PLZ} | Output Disable Time | 3.3 5.0 | 1.5 1.5 | 8.0 6.5 | 11.5 8.5 | 1.0 1.0 | 13.0 10.5 | 1.0 1.0 | 12.5 10.0 | ns | 2-8 |

^{*}Voltage Range 3.3 is 3.3V ± 0.3 V Voltage Range 5.0 is 5.0V ± 0.5 V

AC Operating Requirements

| Symbol | Parameter | | 74AC T _A = +25°C C _L = 50 pF | | 54AC | 74AC | nunixeM. | Fig. No. |
|----------------------|---|-----------------------|--|------------|---|--|----------|-------------|
| | | V _{CC} * (V) | | | T _A = -55°C to +125°C C _L = 50 pF | $T_A = -40^{\circ}C$ to $+85^{\circ}C$ $C_L = 50 pF$ | Units | |
| | | | Тур | | Guaranteed Min | | | |
| t _s | Setup Time, HIGH or LOW D _n to LE | 3.3 5.0 | 3.5 2.0 | 5.5 4.0 | 6.5 5.0 | 6.0 4.5 | ns | 2-9 |
| t _h Au 08 | Hold Time, HIGH or LOW D _n to CP | 3.3 5.0 | -3.0 -1.5 | 1.0 1.0 | 1.0 1.0 | 1.0 1.0 | ns | 2-9 |
| t _w | LE Pulse Width, HIGH | 3.3 5.0 | 4.0 2.0 | 5.5 4.0 | 6.5 5.0 | 6.0 4.5 | ns | 2-6 |

^{*}Voltage Range 3.3 is 3.3V ± 0.3 V Voltage Range 5.0 is 5.0V ± 0.5 V

AC Electrical Characteristics

| Symbol | Parameter | | | 74ACT | | 54ACT | | 74ACT | | | |
|------------------|---|--------------------------|--|-------|------|--|------|--|------|-------|-------------|
| | | V _{CC} * (V) | T _A = +25°C C _L = 50 pF | | | T _A = -55°C to + 125°C C _L = 50 pF | | T _A = -40°C to +85°C C _L = 50 pF | | Units | Fig. No. |
| | | | Min | Тур | Max | Min | Max | Min | Max | Cilei | 00 |
| t _{PLH} | Propagation Delay D _n to O _n | 5.0 | 2.5 | 8.5 | 10.0 | 1.0 | 12.5 | 1.5 | 11.5 | ns | 2-5 |
| t _{PHL} | Propagation Delay D _n to O _n | 5.0 | 2.0 | 8.0 | 10.0 | 1.0 | 12.5 | 1.5 | 11.5 | ns | 2-5 |
| t _{PLH} | Propagation Delay LE to O _n | 5.0 | 2.5 | 8.5 | 11.0 | 1.0 | 12.5 | 2.0 | 11.5 | ns | 2-6 |
| t _{PHL} | Propagation Delay | 5.0 | 2.0 | 8.0 | 10.0 | 1.0 | 11.5 | 1.5 | 11.5 | ns | 2-6 |
| tpzH | Output Enable Time | 5.0 | 2.0 | 8.0 | 9.5 | 1.0 | 11.5 | 1.5 | 10.5 | ns | 2-7 |
| t _{PZL} | Output Enable Time | 5.0 | 2.0 | 7.5 | 9.0 | 1.0 | 11.0 | 1.5 | 10.5 | ns | 2-8 |
| t _{PHZ} | Output Disable Time | 5.0 | 2.5 | 9.0 | 11.0 | 1.0 | 14.0 | 2.5 | 12.5 | ns | 2-7 |
| t _{PLZ} | Output Disable Time | 5.0 | 1.5 | 7.5 | 8.5 | 1.0 | 11.0 | 1.0 | 10.0 | ns | 2-8 |

^{*}Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

| Symbol | | | 74ACT T _A = +25°C C _L = 50 pF | | 54ACT | 74ACT | | |
|----------------|---|--------------------------|--|-----|--|--|-------|------|
| | Parameter 11 | V _{CC} * (V) | | | T _A = -55°C to + 125°C C _L = 50 pF | T _A = -40°C to +85°C C _L = 50 pF | Units | Fig. |
| | | | Тур | 10 | Guaranteed Min | | | |
| ts | Setup Time, HIGH or LOW D _n to LE | 5.0 | 3.0 | 7.0 | 8.5 | 0 08.0 0 | ns | 2-9 |
| t _h | Hold Time, HIGH or LOW D _n to LE | 5.0 | 0 | 0 | 1.0 | aea\s\1.0 | ns | 2-9 |
| t _w | LE Pulse Width, HIGH | 5.0 | 2.0 | 7.0 | 8.5 | 8.0 | ns | 2-6 |

^{*}Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

| Symbol | Parameter | AC/ACT | Units | Conditions | | |
|-----------------|-------------------------------|--------|--------|------------------------|--|--|
| 6-986853VJT | rarameter | Тур | Oilito | Conditions | | |
| C _{IN} | Input Capacitance | 4.5 | pF | $V_{CC} = 5.0V$ | | |
| C _{PD} | Power Dissipation Capacitance | 40.0 | pF | V _{CC} = 5.0V | | |



54AC/74AC374 ◆ 54ACT/74ACT374 Octal D Flip-Flop with TRI-STATE® Outputs

General Description

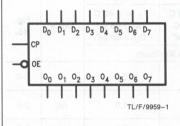
The 'AC/'ACT374 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and TRI-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable (\overline{OE}) are common to all flip-flops.

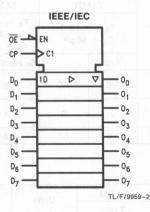
Features

- Buffered positive edge-triggered clock
- TRI-STATE outputs for bus-oriented applications
- Outputs source/sink 24 mA
- See '273 for reset version
- See '377 for clock enable version
- See '373 for transparent latch version
- See '574 for broadside pinout version
- See '564 for broadside pinout version with inverted outputs
- 'ACT374 has TTL-compatible inputs

Ordering Code: See Section 5

Logic Symbols





Connection Diagrams



 Pin Names
 Description

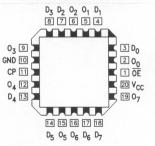
 D₀-D₇
 Data Inputs

 CP
 Clock Pulse Input

 OE
 TRI-STATE Output Enable Input

 O₀-O₇
 TRI-STATE Outputs

Pin Assignment for LCC and PCC



TL/F/9959-4

Functional Description

The 'AC/'ACT374 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{\text{OE}}$) LOW, the contents of the eight flip-flops are available at the outputs. When the $\overline{\text{OE}}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{\text{OE}}$ input does not affect the state of the flip-flops.

Truth Table

| uniupes es | Inputs | | Outputs |
|----------------|--------|---------|-------------------------|
| D _n | CP | ŌĒ | On |
| Н | · | L 6 | H/ visida |
| L | | G C men | O abelü l üçen (|
| X | X | н | Z |

H = HIGH Voltage Level

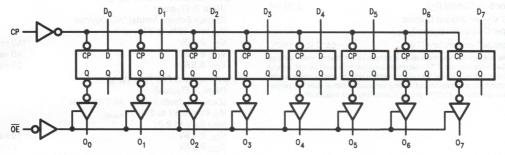
L = LOW Voltage Level

X = Immaterial

Z = High Impedance

✓ = LOW-to-HIGH Transition

Logic Diagram



TL/F/9959-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Supply Voltage (V _{CC}) | -0.5V to $+7.0V$ |
|---|---------------------------------|
| DC Input Diode Current (I _{IK}) | |
| $V_1 = -0.5V$ | -20 mA |
| $V_I = V_{CC} + 0.5V$ | + 20 mA |
| DC Input Voltage (V _I) | -0.5 V to $V_{CC}+0.5$ V |
| DC Output Diode Current (IOK) | |
| $V_0 = -0.5V$ | -20 mA |
| $V_O = V_{CC} + 0.5V$ | + 20 mA |
| DC Output Voltage (V _O) | -0.5 V to to $V_{CC} + 0.5$ V |
| DC Output Source | |
| or Sink Current (IO) | ±50 mA |
| DC V _{CC} or Ground Current | |
| per Output Pin (I _{CC} or I _{GND}) | ± 50 mA |
| Storage Temperature (T _{STG}) | -65°C to +150°C |
| Note 1: Absolute maximum ratings are t | hose values beyond which damage |

to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

Recommended Operating Conditions

| Supply Voltage (V _{CC}) | |
|--|-----------------------|
| 'AC | 2.0V to 6.0V |
| 'ACT state that acut on that sail | 4.57 10 5.57 |
| Input Voltage (V _I) | 01/10// |
| Output Voltage (V _O) | 0V to V _{CC} |
| Operating Temperature (T _A) | |
| 74AC/ACT | |
| 54AC/ACT | -55°C to +125°C |
| Junction Temperature (T _J) | |
| CDIP | 175°C |
| PDIP | 140°C |
| Input Rise and Fall Time (t _r , t _f) (Note 2) (Typical) | |
| (Except Schmitt Inputs) 'AC Devices | 3 |
| V _{IN} from 30% to 70% of V _{CC} | |
| V _{CC} @ 3.0V | 150 ns/V |
| V _{CC} @ 4.5V | 40 ns/V |
| V _{CC} @ 5.5V | 25 ns/V |
| Input Rise and Fall Time (t _r , t _f) (Note 2) (Typical) | |
| (Except Schmitt Inputs) 'ACT Device | es |
| V _{IN} from 0.8V to 2.0V, V _{meas} | |

V_{CC} @ 5.5V Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

10 ns/V

8 ns/V

from 0.8V to 2.0V V_{CC} @ 4.5V

DC Characteristics for 'AC Family Devices

| | | | 74 | AC | 54AC | 74AC | | | |
|-----------------|--------------------------------------|------------------------|-------------------------|----------------------|-----------------------------------|---------------------------------|-------|--|--|
| Symbol | Parameter | V _{CC} (V) | T _A = +25°C | | T _A = -55°C to + 125°C | T _A = -40°C to +85°C | Units | Conditions | |
| | | | Typ Guaranteed Limits | | | | | | |
| V _{IH} | Minimum High Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{IL} | Maximum Low Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{OH} | Minimum High Level Output Voltage | 3.0 4.5 5.5 | 2.99 4.49 5.49 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | ٧ | $I_{OUT} = -50 \mu\text{A}$ | |
| | | 3.0 4.5 5.5 | | 2.56 3.86 4.86 | 2.4 3.7 4.7 | 2.46 3.76 4.76 | ٧ | *V _{IN} = V _{IL} or V _{II} -12 m I _{OH} -24 m -24 m | |
| V _{OL} | Maximum Low Level Output Voltage | 3.0 4.5 5.5 | 0.002 0.001 0.001 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | ٧ | $I_{OUT} = 50 \mu A$ | |
| | | 3.0 4.5 5.5 | | 0.36 0.36 0.36 | 0.50 0.50 0.50 | 0.44 0.44 0.44 | v | *V _{IN} = V _{IL} or V _{II} 12 m/ I _{OL} 24 m/ 24 m/ | |
| I _{IN} | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | ±1.0 | μА | $V_{I} = V_{CC}$, GND | |

DC Characteristics for 'AC Family Devices (Continued)

| | 5445 | | 74AC T _A = +25°C | | 54AC | 74AC | | | |
|------------------|-------------------------------------|------------------------|--------------------------------|------|----------------------------------|---------------------------------|-------|--|--|
| Symbol | Parameter | V _{CC} (V) | | | T _A = -55°C to +125°C | T _A = -40°C to +85°C | Units | Conditions | |
| | | | Тур | -2 | Guaranteed L | imits | | | |
| loz | Maximum TRI-STATE® Current | 5.5 | 1,865 | ±0.5 | ±10.0 | ±5.0 | μΑ | V_{I} (OE) = V_{IL} , V_{IH} V_{I} = V_{CC} , GND V_{O} = V_{CC} , GND | |
| I _{OLD} | †Minimum Dynamic | 5.5 | 2.81 | 0.1 | 50 | 75 | mA | V _{OLD} = 1.65V Max | |
| I _{OHD} | Output Current | 5.5 | | a k | -50 | -75 | mA | V _{OHD} = 3.85V Min | |
| Icc | Maximum Quiescent Supply Current | 5.5 | Ott | 8.0 | 160.0 | 80.0 | μΑ | V _{IN} = V _{CC} or GND | |

^{*}All outputs loaded; thresholds on input associated with output under test.

DC Characteristics for 'ACT Family Devices

| | Parameter | | | | 54ACT | 74ACT | | | |
|------------------|--------------------------------------|------------------------|----------------|--------------|----------------------------------|---------------------------------|-------|---|--|
| Symbol | | V _{CC} (V) | | | T _A = -55°C to +125°C | T _A = -40°C to +85°C | Units | Conditions | |
| | | | Тур | | Guaranteed Li | mits | | AP Proposition | |
| V _{IH} | Minimum High Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 2.0 2.0 | 2.0 2.0 | 2.0 2.0 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{IL} | Maximum Low Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 0.8 | 0.8 0.8 | 0.8 0.8 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{OH} | Minimum High Level Output Voltage | 4.5 5.5 | 4.49 5.49 | 4.4 5.4 | 4.4 5.4 | 4.4 5.4 | ٧ | $I_{OUT} = -50 \mu\text{A}$ | |
| 2.9 | 80 0.8 8.k | 4.5 5.5 | 6.5 | 3.86 4.86 | 3.70 4.70 | 3.76 4.76 | ٧ | $\begin{tabular}{ll} *V_{\mbox{\scriptsize IN}} &= V_{\mbox{\scriptsize IL}} \mbox{\ or } V_{\mbox{\scriptsize IH}} \\ &-24 \mbox{\ mA} \\ &-24 \mbox{\ mA} \end{tabular}$ | |
| V _{OL} | Maximum Low Level Output Voltage | 4.5 5.5 | 0.001 0.001 | 0.1 0.1 | 0.1 0.1 | 0.1 0.1 | V | $I_{OUT} = 50 \mu A$ | |
| | 36 34 | 4.5 5.5 | 5,0 | 0.36 0.36 | 0.50 0.50 | 0.44 0.44 | ٧ | $\label{eq:VIN} \begin{split} ^*\text{V}_{\text{IN}} &= \text{V}_{\text{IL}} \text{or} \text{V}_{\text{IH}} \\ \text{I}_{\text{OL}} & 24 \text{mA} \\ & 24 \text{mA} \end{split}$ | |
| I _{IN} | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | ±1.0 | μΑ | $V_I = V_{CC}$, GND | |
| loz | Maximum TRI-STATE® Current | 5.5 | | ±0.5 | ±10.0 | ±5.0 | μА | $V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}, GND$ | |
| Ісст | Maximum I _{CC} /Input | 5.5 | 0.6 | | 1.6 | 1.5 | mA | $V_{\rm I} = V_{\rm CC} - 2.1V$ | |
| I _{OLD} | †Minimum Dynamic | 5.5 | | | 50 | 75 | mA | V _{OLD} = 1.65V Max | |
| I _{OHD} | Output Current | 5.5 | | | -50 | -75 | mA | V _{OHD} = 3.85V Min | |
| lcc | Maximum Quiescent Supply Current | 5.5 | | 8.0 | 160.0 | 80.0 | μΑ | V _{IN} = V _{CC} or GND | |

^{*}All outputs loaded; thresholds on input associated with output under test.

[†]Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC} . I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

[†]Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

| | | 78,80 | | 74AC | 86/ | 54 | AC | 74 | AC | | |
|------------------|---|-------------------|--|-------------|--------------|---|--------------|--|--------------|-------|-------------|
| Symbol | Parameter | V _{CC} * | T _A = +25°C C _L = 50 pF | | | $T_A = -55^{\circ}C$ to + 125°C $C_L = 50 pF$ | | T _A = -40°C to +85°C C _L = 50 pF | | Units | Fig. No. |
| | | | Min | Тур | Max | Min | Max | Min | Max | | |
| f _{max} | Maximum Clock Frequency | 3.3 5.0 | 60 100 | 110 155 | 15 | 60 95 | ě | 60 100 | | MHz | 2-3 |
| ^t PLH | Propagation Delay CP to O _n | 3.3 5.0 | 3.0 2.5 | 11.0 | 13.5 9.5 | 1.0 1.0 | 16.5 12.0 | 1.5 1.5 | 15.5 10.5 | ns | 2-6 |
| t _{PHL} | Propagation Delay CP to On | 3.3 5.0 | 2.5 2.0 | 10.0 7.0 | 12.5 9.0 | 1.0 1.0 | 15.0 11.0 | 2.0 1.5 | 14.0 10.0 | ns | 2-6 |
| t _{PZH} | Output Enable Time | 3.3 5.0 | 3.0 2.0 | 9.5 7.0 | 11.5 8.5 | 1.0 1.0 | 14.0 10.5 | 1.5 1.0 | 13.0 9.5 | ns | 2-7 |
| t _{PZL} | Output Enable Time | 3.3 5.0 | 2.5 2.0 | 9.0 6.5 | 11.5 8.5 | 1.0 1.0 | 14.0 10.5 | 1.5 1.0 | 13.0 9.5 | ns | 2-8 |
| t _{PHZ} | Output Disable Time | 3.3 5.0 | 3.0 2.0 | 10.5 8.0 | 12.5 11.0 | 1.0 1.0 | 16.0 12.5 | 2.0 2.0 | 14.5 12.5 | ns | 2-7 |
| t _{PLZ} | Output Disable Time | 3.3 5.0 | 2.0 1.5 | 8.0 6.5 | 11.5 8.5 | 1.0 | 13.0 10.5 | 1.0 1.0 | 12.5 10.0 | ns | 2-8 |

^{*}Voltage Range 3.3 is 3.3V ±0.3V Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

| V .0 | | V _{CC} * (V) | 74AC T _A = +25°C C _L = 50 pF | | 54AC | 74AC | | Fig. |
|---------------------|---|--------------------------|---|------------|--|--|----------|------|
| Symbol | Parameter | | | | T _A = -55°C to + 125°C C _L = 50 pF | T _A = -40°C to +85°C C _L = 50 pF | Units | |
| | | | Тур | la fila | Guaranteed Min | imum | Tright C | |
| t _s to A | Setup Time, HIGH or LOW D _n to CP | 3.3 5.0 | 2.0 1.0 | 5.5 4.0 | 6.5 5.0 | 6.0 4.5 | ns | 2-9 |
| t _h | Hold Time, HIGH or LOW D _n to CP | 3.3 5.0 | -1.0 0 | 1.0 1.5 | 1.0 | 1.0 1.5 wo lim | ns | 2-9 |
| t _w | CP Pulse Width, HIGH or LOW | 3.3 5.0 | 4.0 2.5 | 5.5 4.0 | 6.5 5.0 | 6.0 4.5 | ns | 2-6 |

^{*}Voltage Range 3.3 is 3.3V ± 0.3 V Voltage Range 5.0 is 5.0V ± 0.5 V

AC Electrical Characteristics

| | | V _{CC} * (V) | | 74ACT | | 54/ | ACT | 74ACT | | | |
|------------------|---|--------------------------|--|-------|-------|---|------|--|------|---------|-------------|
| Symbol | Parameter | | T _A = +25°C C _L = 50 pF | | | $T_A = -55^{\circ}C$ to + 125°C $C_L = 50 pF$ | | T _A = -40°C to +85°C C _L = 50 pF | | Units | Fig. No. |
| | | | Min | Тур | Max | Min | Max | Min | Max | CT Fact | |
| f _{max} | Maximum Clock Frequency | 5.0 | 100 | 160 | mm 13 | 70 | | 90 | | MHz | 2-3 |
| t _{PLH} | Propagation Delay CP to O _n | 5.0 | 2.0 | 8.5 | 10.0 | 1.0 | 12.0 | 2.0 | 11.5 | ns | 2-6 |
| t _{PHL} | Propagation Delay CP to O _n | 5.0 | 2.0 | 8.0 | 9.5 | 1.0 | 11.5 | 1.5 | 11.0 | ns | 2-6 |
| t _{PZH} | Output Enable Time | 5.0 | 2.0 | 8.0 | 9.5 | 1.0 | 11.5 | 1.5 | 10.5 | ns | 2-7 |
| t _{PZL} | Output Enable Time | 5.0 | 1.5 | 8.0 | 9.0 | 1.0 | 11.5 | 1.5 | 10.5 | ns | 2-8 |
| t _{PHZ} | Output Disable Time | 5.0 | 1.5 | 8.5 | 11.5 | 1.0 | 13.0 | 1.0 | 12.5 | ns | 2-7 |
| t _{PLZ} | Output Disable Time | 5.0 | 1.5 | 7.0 | 8.5 | 1.0 | 11.0 | 1.0 | 10.0 | ns | 2-8 |

^{*}Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

| | 149 | 50 | 74ACT T _A = +25°C C _L = 50 pF | | 54ACT | 74ACT | Units | Fig. No. |
|----------------|---|-------------------|--|-----|---|--|---------|-------------|
| Symbol | Parameter | V _{CC} * | | | $T_A = -55^{\circ}C$ to $+125^{\circ}C$ $C_L = 50 pF$ | T _A = -40°C to +85°C C _L = 50 pF | | |
| | grant and the second second second | | Тур | | Guaranteed Min | imum | and the | energy (|
| t _s | Setup Time, HIGH or LOW D _n to CP | 5.0 | 1.0 | 7.0 | 8.5 | 8.0 | ns | 2-9 |
| t _h | Hold Time, HIGH or LOW D _n to CP | 5.0 | 0 | 1.5 | 1.5 | 1.5 | ns | 2-9 |
| t _w | CP Pulse Width, HIGH or LOW | 5.0 | 2.5 | 7.0 | 8.5 | 8.0 | ns | 2-6 |

^{*}Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

| Symbol | Parameter | AC/ACT | Units | Conditions | |
|-----------------|-------------------------------|--------|-------|-----------------|--|
| n-race value | raiameter | Тур | Onits | Conditions | |
| C _{IN} | Input Capacitance | 4.5 | pF | $V_{CC} = 5.0V$ | |
| C _{PD} | Power Dissipation Capacitance | 80.0 | pF | $V_{CC} = 5.0V$ | |



54AC/74AC377 • 54ACT/74ACT377 Octal D Flip-Flop with Clock Enable

General Description

The 'AC/'ACT377 has eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously. when the Clock Enable (CE) is LOW.

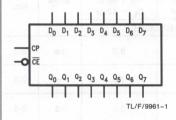
The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The CE input must be stable only one setup time prior to the LOW-to-HIGH clock transition for predictable operation.

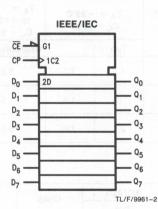
Features

- Ideal for addressable register applications
- Clock enable for address and data synchronization applications
- Eight edge-triggered D flip-flops
- Buffered common clock
- Outputs source/sink 24 mA
- See '273 for master reset version
- See '373 for transparent latch version
- See '374 for TRI-STATE® version
- 'ACT377 has TTL-compatible inputs

Ordering Code: See Section 5

Logic Symbols



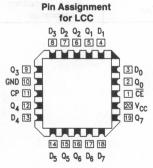


Connection Diagrams Pin Assignment

for DIP, Flatpak and SOIC CE 20 Q₀ 19 Q7 D₀ 18 D7 D₁-17 D_R Q1-16 -Qg Q₂· 15 -Q5 D2 -14 -D5 -D₄ 13 D3 . -Q4 12 Q_3 GND 10 11

TL/F/9961-3

| Pin Names | Description |
|--------------------------------|--|
| D ₀ -D ₇ | Data Inputs |
| $Q_0 - Q_7$ | Clock Enable (Active LOW) Data Outputs |
| CP | Clock Pulse Input |



TL/F/9961-4

| - N | lod | 0 | Sel | ect- | Funct | ion 1 | Γahi | ie |
|-----|-----|---|-----|------|-------|-------|------|----|
| | | | | | | | | |

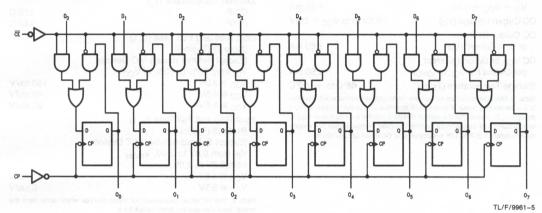
| Operating Mode | | Inputs | noitil | Outputs | |
|-------------------|----|--------|----------|-----------------|--|
| Operating mode | СР | CE | Dn | Q _n | |
| Load '1' | | L | Н | Н | |
| Load '0' | _ | L | va Losil | v geni L | |
| Hold (Do Nothing) | × | H | X | No Change | |

H = HIGH Voltage Level L = LOW Voltage Level

X = Immaterial

— = LOW-to-HIGH Clock Transition

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Supply Voltage (V _{CC}) | -0.5V to $+7.0V$ |
|---|-----------------------------------|
| DC Input Diode Current (I _{IK}) | |
| $V_1 = -0.5V$ | -20 mA |
| $V_I = V_{CC} + 0.5V$ | + 20 mA |
| DC Input Voltage (V _I) | -0.5 V to $V_{CC} + 0.5$ V |
| DC Output Diode Current (IOK) | |
| $V_{O} = -0.5V$ | -20 mA |
| $V_O = V_{CC} + 0.5V$ | + 20 mA |
| DC Output Voltage (V _O) | -0.5 V to to V_{CC} + 0.5 V |
| DC Output Source or Sink Current (Io) | ±50 mA |

Storage Temperature (T_{STG}) -65°C to +150°C Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recom-

mend operation of FACTTM circuits outside databook specifications.

DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})

Recommended Operating Conditions

| Supply Voltage (V _{CC}) | |
|--|-----------------------|
| 'AC | 2.0V to 6.0V |
| 'ACT | 4.5V to 5.5V |
| Input Voltage (V _I) | 0V to V _{CC} |
| Output Voltage (V _O) | 0V to V _{CC} |
| Operating Temperature (T _A) | |
| 74AC/ACT | -40°C to +85°C |
| 54AC/ACT | -55°C to +125°C |
| Junction Temperature (T _J) | |
| CDIP | 175°C |
| PDIP | 140°C |
| Input Rise and Fall Time (t _r , t _f) (Note 2) (Typical) (Except Schmitt Inputs) 'AC Devices | |
| V _{IN} from 30% to 70% of V _{CC} | |
| V _{CC} @ 3.0V | 150 ns/V |
| V _{CC} @ 4.5V | 40 ns/V |
| V _{CC} @ 5.5V | 25 ns/V |
| Input Rise and Fall Time (t _r , t _f) (Note 2) (Typical) | |
| (Except Schmitt Inputs) 'ACT Devices V _{IN} from 0.8V to 2.0V, V _{meas} from 0.8V to 2.0V | |
| V _{CC} @ 4.5V | 10 ns/V |
| | |

V_{CC} @ 5.5V Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

8 ns/V

DC Characteristics for 'AC Family Devices

| | Parameter | | 74. | AC | 54AC | 74AC | | | |
|-----------------|--------------------------------------|---------------------|-------------------------|----------------------|-----------------------------------|---------------------------------|-------|---|--|
| Symbol | | V _{CC} (V) | T _A = +25°C | | T _A = -55°C to + 125°C | T _A = -40°C to +85°C | Units | Conditions | |
| | | | Тур | | Guaranteed Li | imits | | | |
| V _{IH} | Minimum High Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{IL} | Maximum Low Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{OH} | Minimum High Level Output Voltage | 3.0 4.5 5.5 | 2.99 4.49 5.49 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | ٧ | $I_{OUT} = -50 \mu\text{A}$ | |
| | | 3.0 4.5 5.5 | | 2.56 3.86 4.86 | 2.4 3.7 4.7 | 2.46 3.76 4.76 | v | $\begin{tabular}{ll} *V_{\text{IN}} &= V_{\text{IL}} \text{ or } V_{\text{IH}} \\ &-12 \text{ mA} \\ I_{\text{OH}} &-24 \text{ mA} \\ &-24 \text{ mA} \\ \end{tabular}$ | |
| V _{OL} | Maximum Low Level Output Voltage | 3.0 4.5 5.5 | 0.002 0.001 0.001 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | V | I _{OUT} = 50 μA | |
| | | 3.0 4.5 5.5 | | 0.36 0.36 0.36 | 0.50 0.50 0.50 | 0.44 0.44 0.44 | v | $\begin{tabular}{ll} *V_{IN} &= V_{IL} \mbox{ or } V_{IH} \\ &= 12 \mbox{ mA} \\ I_{OL} &= 24 \mbox{ mA} \\ &= 24 \mbox{ mA} \\ \end{tabular}$ | |
| I _{IN} | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | ± 1.0 | μΑ | $V_{I} = V_{CC}$, GND | |

±50 mA

DC Characteristics for 'AC Family Devices (Continued)

| | TARC | | 74AC T _A = +25°C | | 54AC | 74AC | | |
|------------------|-------------------------------------|------------------------|--------------------------------|-------|----------------------------------|---|-------|------------------------------|
| Symbol | Parameter | V _{CC} (V) | | | T _A = -55°C to +125°C | $T_A = -40^{\circ}C \text{ to } +85^{\circ}C$ | Units | Conditions |
| | | | Тур | 10 | Guaranteed Li | mits | | |
| I _{OLD} | †Minimum Dynamic | 5.5 | £ 10-109 | 11100 | 50 | 75 | mA | V _{OLD} = 1.65V Max |
| IOHD | Output Current | 5.5 | | 88 | -50 | -75 | mA | V _{OHD} = 3.85V Min |
| Icc | Maximum Quiescent Supply Current | 5.5 | 14.0 | 8.0 | 160.0 | 80.0 | μА | $V_{IN} = V_{CC}$ or GND |

^{*}All outputs loaded; thresholds on input associated with output under test.

Note: I_{1N} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC} . I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

| | CAAS | | 744 | CT | 54ACT | 74ACT | | | |
|------------------|--------------------------------------|---------------------|------------------------|--------------|-----------------------------------|---------------------------------|-------|--|--|
| Symbol | Parameter | V _{CC} (V) | T _A = +25°C | | T _A = -55°C to + 125°C | T _A = -40°C to +85°C | Units | Conditions | |
| | C1 = 20 0F | | Typ Guaranteed Limits | | | | | | |
| V _{IH} | Minimum High Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 2.0 2.0 | 2.0 2.0 | 2.0 2.0 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{IL} | Maximum Low Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 0.8 0.8 | 0.8 0.8 | 0.8 0.8 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{OH} | Minimum High Level Output Voltage | 4.5 5.5 | 4.49 5.49 | 4.4 5.4 | 4.4 5.4 | 4.4 5.4 | V | $I_{OUT} = -50 \mu\text{A}$ | |
| | en 0.1 | 4.5 5.5 | 9.1 0.3 | 3.86 4.86 | 3.70 4.70 | 3.76 4.76 | ٧ | $\begin{tabular}{ll} *V_{IN} &= V_{IL} \mbox{ or } V_{IH} \\ &-24 \mbox{ mA} \\ &-24 \mbox{ mA} \end{tabular}$ | |
| V _{OL} | Maximum Low Level Output Voltage | 4.5 5.5 | 0.001 0.001 | 0.1 0.1 | 0.1 0.1 | 0.1 0.1 | V | I _{OUT} = 50 μA | |
| | | 4.5 5.5 | | 0.36 0.36 | 0.50 0.50 | 0.44 0.44 | V | $\begin{tabular}{ll} *V_{IN} &= V_{IL} \mbox{ or } V_{IH} \\ I_{OL} & 24 \mbox{ mA} \\ & 24 \mbox{ mA} \\ \end{tabular}$ | |
| I _{IN} | Maximum Input Leakage Current | 5.5 | | ±0.1 | ± 1.0 | ±1.0 | μА | $V_I = V_{CC}$, GND | |
| I _{CCT} | Maximum I _{CC} /Input | 5.5 | 0.6 | | 1.6 | 1.5 | mA | $V_I = V_{CC} - 2.1V$ | |
| I _{OLD} | †Minimum Dynamic | 5.5 | | | 50 | 75 | mA | V _{OLD} = 1.65V Max | |
| I _{OHD} | Output Current | 5.5 | | | -50 | -75 | mA | V _{OHD} = 3.85V Min | |
| Icc | Maximum Quiescent Supply Current | 5.5 | | 8.0 | 160.0 | 80.0 | μА | V _{IN} = V _{CC} or GND | |

^{*}All outputs loaded; thresholds on input associated with output under test.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

[†]Maximum test duration 2.0 ms, one output loaded at a time.

[†]Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics and applied viling 3 0.4° to 1 applied as an 0.00

| Symbol | Parameter | CAL | 74AC T _A = +25°C C _L = 50 pF | | | 54AC T _A = -55°C to + 125°C C _L = 50 pF | | 74 | AC | | |
|------------------|---|-----------------------|--|------------|--------------|--|--------------|--|--------------|-------|-------------|
| | | V _{CC} * (V) | | | | | | T _A = -40°C to +85°C C _L = 50 pF | | Units | Fig. No. |
| | | | Min | Тур | Max | Min | Max | Min | Max | | |
| f _{max} | Maximum Clock Frequency | 3.3 5.0 | 90 140 | 125 175 | | 75 95 | 6 | 75 125 | ine nuolit | MHz | 2-3 |
| t _{PLH} | Propagation Delay CP to Q _n | 3.3 5.0 | 3.0 2.0 | 8.0 6.0 | 13.0 9.0 | 1.0 | 14.0 10.0 | 1.5 1.5 | 14.0 10.0 | ns | 2-6 |
| t _{PHL} | Propagation Delay CP to Q _n | 3.3 5.0 | 3.5 2.5 | 8.5 6.5 | 13.0 10.0 | 1.0 1.0 | 15.0 11.0 | 2.0 1.5 | 14.5 11.0 | ns | 2-6 |

^{*}Voltage Range 3.3 is 3.3V \pm 0.3V Voltage Range 5.0 is 5.0V \pm 0.5V

AC Operating Requirements

| Symbol | 1544 | | 74 | AC | 54AC | 74AC | | |
|---------------------|---|-------------------|--|------------|--|--|-------|-------------|
| | Parameter | V _{CC} * | T _A = +25°C C _L = 50 pF | | T _A = -55°C to + 125°C C _L = 50 pF | T _A = -40°C to +85°C C _L = 50 pF | Units | Fig. No. |
| | | orac repair | Тур | | Guaranteed Minimum | | | |
| t _s valo | Setup Time, HIGH or LOW D _n to CP | 3.3 5.0 | 3.5 2.5 | 5.5 4.0 | 7.5 6.0 | 6.0 4.5 | ns | 2-9 |
| t _h | Hold Time, HIGH or LOW D _n to CP | 3.3 5.0 | -2.0 -1.0 | 0 | 1.5 2.5 | 0 1.0 | ns | 2-9 |
| ts | Setup Time, HIGH or LOW CE to CP | 3.3 5.0 | 4.0 2.5 | 6.0 4.0 | 9.5 6.0 | 7.5 4.5 | ns | 2-9 |
| t _h | Hold Time, HIGH or LOW CE to CP | 3.3 5.0 | -3.5 -2.0 | 0 1.0 | 1.0 2.0 | 0 1.0 | ns | 2-9 |
| t _w | CP Pulse Width HIGH or LOW | 3.3 5.0 | 3.5 2.5 | 5.5 4.0 | 6.5 5.0 | 6.0 4.5 | ns | 2-6 |

^{*}Voltage Range 3.3 is 3.0V ± 0.3 V Voltage Range 5.0 is 5.0V ± 0.5 V

AC Electrical Characteristics

| Symbol | Parameter | V _{CC} * (V) | 74ACT T _A = +25°C C _L = 50 pF | | | 54ACT T _A = -55°C to +125°C C _L = 50 pF | | 74 | ACT | | La Laboratoria |
|------------------|---|--------------------------|--|-----|------|--|-----------------|--|------|---------|----------------|
| | | | | | | | | T _A = -40°C to +85°C C _L = 50 pF | | Units | Fig. No. |
| | | | Min | Тур | Max | Min | Max | Min | Max | X3 33 1 | |
| f _{max} | Maximum Clock Frequency | 5.0 | 140 | 175 | | 85 | AND THE NAME OF | 125 | | MHz | 2-3 |
| t _{PLH} | Propagation Delay CP to Q _n | 5.0 | 3.0 | 6.5 | 9.0 | 1.0 | 11.0 | 2.5 | 10.0 | ns | 2-6 |
| t _{PHL} | Propagation Delay CP to Q _n | 5.0 | 3.5 | 7.0 | 10.0 | 1.0 | 12.0 | 2.5 | 11.0 | ns | 2-6 |

^{*}Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

| | 2016100 | O noi | 74A | CT | 54ACT | 74ACT | me a | ipa. |
|----------------|---|-------------------|--|-----|--|--|-------|-------------|
| Symbol | Parameter | V _{CC} * | T _A = +25°C C _L = 50 pF | | T _A = -55°C to + 125°C C _L = 50 pF | T _A = -40°C to +85°C C _L = 50 pF | Units | Fig. No. |
| | | | Typ Guaranteed Minimum | | imum | | | |
| ts | Setup Time, HIGH or LOW D _n to CP | 5.0 | 2.5 | 4.5 | 7.0 | 5.5 | ns | 2-9 |
| t _h | Hold Time, HIGH or LOW D _n to CP | 5.0 | -1.0 | 1.0 | 1.0 | 1.0 | ns | 2-9 |
| t _s | Setup Time, HIGH or LOW CE to CP | 5.0 | 2.5 | 4.5 | 7.0 | 5.5 | ns | 2-9 |
| t _h | Hold Time, HIGH or LOW CE to CP | 5.0 | -1.0 | 1.0 | 1.0 | 1.0 | ns | 2-9 |
| t _w | CP Pulse Width HIGH or LOW | 5.0 | 2.0 | 4.0 | 5.5 | 4.5 | ns | 2-6 |

^{*}Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

| Symbol | Parameter | AC/ACT | Units | Conditions | |
|-----------------|----------------------------------|--------|--------|------------------------|--|
| Оушьог | r arameter erugni t | Тур | Office | | |
| CIN | Input Capacitance | 4.5 | pF | $V_{CC} = 5.0V$ | |
| C _{PD} | Power Dissipation Capacitance | 90.0 | pF | V _{CC} = 5.0V | |



ADVANCE INFORMATION

54ACT/74ACT381 4-Bit Arithmetic Logic Unit

General Description

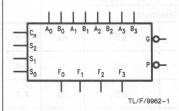
The 'ACT381 performs three arithmetic and three logic operations on two 4-bit words, A and B. Two additional select input codes force the function outputs LOW or HIGH. Carry propagate and generate outputs are provided for use with the 'AC/'ACT182 carry lookahead generator for high-speed expansion to longer word lengths.

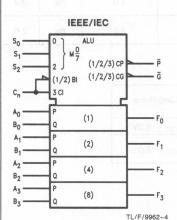
Features

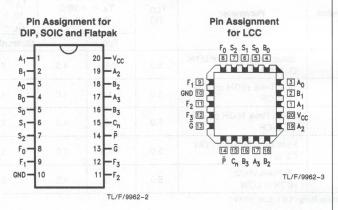
- Low input loading minimizes drive requirements
- Performs six arithmetic and logic functions
- Selectable LOW (clear) and HIGH (preset) functions
- Carry generate and propagate outputs for use with carry lookahead generator
- 'ACT381 has TTL-compatible inputs

Logic Symbols

Connection Diagrams







| Pin Names | Description | | | | | | |
|--------------------------------|-------------------------------------|--|--|--|--|--|--|
| A ₀ -A ₃ | A Operand Inputs | | | | | | |
| B ₀ -B ₃ | B Operand Inputs | | | | | | |
| S0-S2 | Function Select Inputs | | | | | | |
| Cn | Carry Input | | | | | | |
| G | Carry Generate Output (Active LOW) | | | | | | |
| P | Carry Propagate Output (Active LOW) | | | | | | |
| F ₀ -F ₃ | Function Outputs | | | | | | |



54ACT/74ACT399 Quad 2-Port Register

General Description

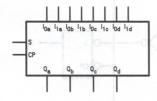
The 'ACT399 is the logical equivalent of a quad 2-input multiplexer feeding into four edge-triggered flip-flops. A common Select input determines which of the two 4-bit words is accepted. The selected data enters the flip-flop on the rising edge of the clock.

Features

- Select inputs from two data sources
- Fully positive edge-triggered operation
- Outputs source/sink 24 mA
- 'ACT399 has TTL-compatible inputs

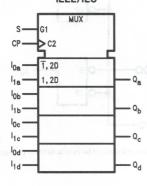
Ordering Code: See Section 5

Logic Symbols



TL/F/9789-1

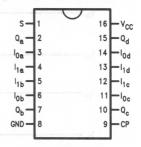
IEEE/IEC



TL/F/9789-5

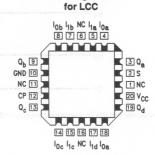
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



Pin Assignment

TL/F/9789-3



TL/F/9789-2

| Pin Names | Description |
|----------------------------------|---------------------------|
| S | Common Select Input |
| CP | Clock Pulse Input |
| $I_{0a}-I_{0d}$ | Data Inputs from Source 0 |
| I _{1a} -I _{1d} | Data Inputs from Source 1 |
| Q _a -Q _d | Register True Outputs |

Functional Description

The 'ACT399 is a high-speed quad 2-port register. It selects four bits of data from either of two sources (Ports) under control of a common Select input (S). The selected data is transferred to a 4-bit output register synchronous with the LOW-to-HIGH transition of the Clock input (CP). The 4-bit D-type output register is fully edge-triggered. The Data inputs ($I_{\rm Ox}$, $I_{\rm 1x}$) and Select input (S) must be stable only a setup time prior to and hold time after the LOW-to-HIGH transition of the Clock input for predictable operation.

Function Table

| | In | puts | · 数别,数数数多数。 | Out | puts |
|---|----------------|----------------|-------------|-----|------|
| S | I ₀ | l ₁ | СР | Q | Q |
| L | L | X | _ | L | Н |
| L | HO | X | - | Н | L |
| Н | X | L | _ | L | Н |
| Н | X | Н | 5 | Н | L |

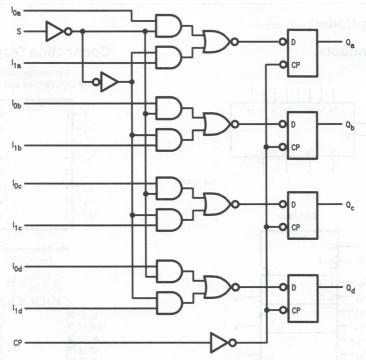
H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

__ = LOW-to-HIGH Clock Transition

Logic Diagram



TL/F/9789-4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (VCC) -0.5V to +7.0VDC Input Diode Current (IIK) $V_1 = -0.5V$ -20 mA $V_I = V_{CC} + 0.5V$ +20 mA DC Input Voltage (VI) -0.5V to $V_{CC} + 0.5V$

DC Output Diode Current (IOK) $V_0 = -0.5V$

-20 mA $V_0 = V_{CC} + 0.5V$ +20 mA DC Output Voltage (Vo) -0.5V to $V_{CC} + 0.5V$ DC Output Source or Sink Current (IO)

DC V_{CC} or Ground Current

 $\pm 50 \text{ mA}$ per Output Pin (I_{CC} or I_{GND}) Storage Temperature (TSTG) -65°C to +150°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (VCC) 'AC 2.0V to 6.0V 'ACT 4.5V to 5.5V Input Voltage (VI) OV to Vcc Output Voltage (VO) 0V to V_{CC} Operating Temperature (TA) 74AC/ACT -40°C to +85°C 54AC/ACT -55°C to +125°C Junction Temperature (T_J) +175°C PDIP +140°C Input Rise and Fall Time (tr, tf) (Note 2) (Typical)

(Except Schmitt Inputs) 'AC Devices

VIN from 30% to 70% of VCC

VCC @ 3.0V 150 ns/V V_{CC} @ 4.5V 40 ns/V V_{CC} @ 5.5V 25 ns/V Input Rise and Fall Time (tr., tf)

(Note 2) (Typical) (Except Schmitt Inputs) 'ACT Devices VIN from 0.8V to 2.0V, Vmeas

from 0.8V to 2.0V VCC @ 4.5V

10 ns/V V_{CC} @ 5.5V 8 ns/V

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Electrical Characteristics for 'ACT Family Devices

| 95 21 | Parameter | | 744 | CT | 54ACT | 74ACT | | 80.48 | |
|-----------------|-------------------------------------|---------------------|-----------------------|--------------|-----------------------------------|---------------------------------|-------|--|--|
| Symbol | | V _{CC} (V) | T _A = 25°C | | T _A = -55°C to + 125°C | T _A = -40°C to +85°C | Units | Conditions | |
| | | | Typ Guaranteed Limits | | | | | id a Uli egg i sgatavi | |
| V _{IH} | Minimum High Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 2.0 2.0 | 2.0 2.0 | 2.0 2.0 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} = 0.1V$ | |
| V _{IL} | Maximum Low Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 0.8 | 0.8 0.8 | 0.8 0.8 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{OH} | Minimum High Level | 4.5 5.5 | 4.49 5.49 | 4.4 5.4 | 4.4 5.4 | 4.4 5.4 | V | $I_{OUT} = -50 \mu\text{A}$ | |
| | 30V | 4.5 5.5 | | 3.86 4.85 | 3.70 4.70 | 3.76 4.76 | V | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IOH} = -24 \text{ mA}$ $V_{IOH} = -24 \text{ mA}$ | |
| V _{OL} | Maximum Low Level Output Voltage | 4.5 5.5 | 0.001 0.001 | 0.1 0.1 | 0.1 0.1 | 0.1 0.1 | ٧ | I _{OUT} = 50 μA | |
| | | 4.5 5.5 | | 0.36 0.36 | 0.50 0.50 | 0.44 0.44 | ٧ | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = 24 \text{ mA}$ $V_{IOL} = 24 \text{ mA}$ | |
| IIN | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | ±1.0 | μА | $V_I = V_{CC}$, GND | |
| ICCT | Maximum I _{CC} /Input | 5.5 | 0.6 | | 1.6 | 1.5 | mA | $V_I = V_{CC} - 2.1V$ | |
| IOLD | †Minimum Dynamic | 5.5 | | | 50 | 75 | mA | V _{OLD} = 1.65V Max | |
| IOHD | Output Current | 5.5 | | | -50 | −75 | mA | V _{OHD} = 3.85V Min | |
| lcc | Maximum Quiescent Supply Current | 5.5 | | 8.0 | 160 | 80 | μΑ | V _{IN} = V _{CC} or Ground (Note 3) | |

Note 3: ICC for the 54ACT device is identical to the 74ACT device at 25°C.

^{*}All outputs loaded; thresholds on input associated with output under test.

[†]Maximum test duration 2.0 ms, one output loaded at a time

AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

| Symbol | | | enom | 74ACT | , The | 54A | СТ | 7 | 4ACT | MANGASON Modela | n o soto |
|------------------|------------------------------|-----------------------|--|-------|-------|--|----------|-----|----------|--------------------|-------------|
| | Parameter | V _{CC} * (V) | $\begin{aligned} \textbf{T}_{\textbf{A}} &= +25^{\circ}\textbf{C} \\ \textbf{V}_{\textbf{CC}} &= +5.0\textbf{V} \\ \textbf{C}_{\textbf{L}} &= \textbf{50}~\textbf{pF} \end{aligned}$ | | | $ \begin{array}{c c} T_{A}, V_{CC} = Mil \\ C_{L} = 50 \ pF \end{array} \qquad \begin{array}{c} T_{A}, V_{CC} = Col \\ C_{L} = 50 \ pF \end{array} $ | | | Units | Fig. No. | |
| | /0 | | Min | Тур | Max | Min | Max | Min | Max | /B.O~ = | V |
| f _{max} | Input Clock Frequency | 5.0 | 165 | 160 | va. | 90 | n Vã 0 - | 160 | (iV) and | MHz | 2-3 |
| t _{PLH} | Propagation Delay CP to Q | 5.0 | 1.5 | 7.0 | 8.0 | 20 | 10.0 | 1.5 | 8.5 | ns | 2-6 |
| t _{PHL} | Propagation Delay CP to Q | 5.0 | 2.0 | 6.0 | 9.0 | 0 + coV8 | 10.0 | 2.0 | 9.5 | ns | 2-6 |

^{*}Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements: See Section 2 for Waveforms

| Symbol | | | 74 | ACT | 54ACT | 74ACT | losither | 11019 |
|----------------|--|-------------------|--|-------|--|---|--------------|-------------|
| | Parameter | V _{CC} * | $T_A = +25^{\circ}C$ $C_L = 50 \text{ pF}$ | | $T_A = -55^{\circ}\text{C to} + 125^{\circ}\text{C}$ $C_L = 50 \text{ pF}$ | $T_A = -40^{\circ}\text{C to} + 85^{\circ}\text{C}$ $C_L = 50 \text{ pF}$ | Units | Fig. No. |
| | No. of the last of | (let | Тур | deVi) | Guaranteed Minimu | m | Propies alto | 10013 |
| t _s | Setup Time, HIGH or LOW In to CP | 5.0 | 3.0 | 2.5 | 3.5 | 2.5 | ns | 2-9 |
| th Vivan 8 | Hold Time, HIGH or LOW In to CP | 5.0 | 0 | 1.0 | 3.0 | 1.0 | ns | 2-9 |
| t _s | Setup Time, HIGH or LOW S to CP | 5.0 | 3.0 | 4.0 | 6.0 | 4.0 | ns | 2-9 |
| t _h | Hold Time, HIGH or LOW S to CP | 5.0 | -1.0 | 0.5 | 2.5 | 0.5 | ns | 2-9 |
| t _w | CP Pulse Width HIGH or LOW | 5.0 | 5.5 | 3.5 | 5.0 | 3.5 | ns | 2-6 |

^{*}Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

| Symbol | Parameter | AC/ACT | Units | Conditions |
|-----------------|-------------------------------|--------|-------|-----------------|
| Cymbol | T diameter | Тур | Onito | Conditions |
| CIN | Input Capacitance | 4.5 | pF | $V_{CC} = 5.0V$ |
| C _{PD} | Power Dissipation Capacitance | 30 | pF | $V_{CC} = 5.0V$ |



54AC/74AC520 • 54ACT/74ACT520 8-Bit Identity Comparator

General Description

The 'AC/'ACT520 are expandable 8-bit comparators. They compare two words of up to eight bits each and provide a LOW output when the two words match bit for bit. The expansion input $\tilde{l}_{A\ =\ B}$ also serves as an active LOW enable input.

Features

- Compares two 8-bit words in 6.5 ns typ
- Expandable to any word length
- 20-pin package
- Outputs source/sink 24 mA
- 'ACT520 has TTL-compatible inputs

Ordering Code: See Section 5 **Logic Symbols Connection Diagrams** Pin Assignment for DIP, Flatpak and SOIC B6 A6 B5 A5 B4 A4 B3 A3 B2 A2 B₁ T_{A=B} 20 V_{CC} - Ō_{A=B} A₀ 19 18 · B₇ Bo · A₁ 17 - A₇ -B₆ 16 TL/F/10194-1 A2 15 - A₆ IEEE/IEC B₂ -14 -B₅ COMP 1.3 B3 · 9 12 -B₄ A₀ GND TL/F/10194-2 A2 A₃ Pin Assignment for LCC A₃ B₂ A₂ B₁ A₁ 8 7 6 5 4 A₅ ō_{A=B} 1P=Q A₇ ■ 3 B₀ B₃ 9 B_0 GND 10 A₄ 11 B₄ 12 A₅ 13 2 A₀ B₁ 20 V_{CC} 19 Ō_{A=B} B_2 B3 Q B_4 B_5 14 15 16 17 18

| Pin Names | Description |
|--------------------------------|---------------------------|
| A ₀ -A ₇ | Word A Inputs |
| B ₀ -B ₇ | Word B Inputs |
| $T_A = B$ | Expansion or Enable Input |
| $\overline{O}_A = B$ | Identity Output |

 B_6

B5 A6 B6 A7 B7

TL/F/10194-3

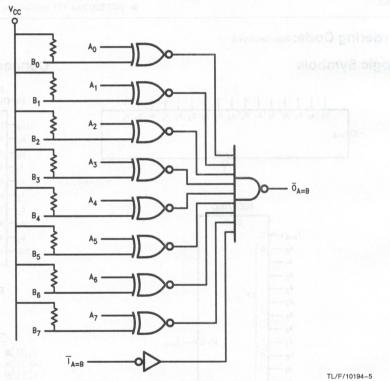
TL/F/10194-4

Truth Table

| Inj | outs | Outputs |
|--------------------|------------|----------------------|
| Ī _A = B | A, B | $\overline{O}_A = B$ |
| L | A = B* | m Lagran |
| L | $A \neq B$ | Н |
| Н | $A = B^*$ | н |
| Н | $A \neq B$ | Н |

$$\begin{split} &H = \text{HIGH Voltage Level} \\ &L = \text{LOW Voltage Level} \\ &*A_0 = B_0, \, A_1 = B_1, \, A_2 = B_2, \, \text{etc.} \end{split}$$

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| -0.5V to $+7.0V$ |
|-------------------------------|
| −20 mA +20 mA |
| -0.5 V to $V_{CC} + 0.5$ V |
| −20 mA +20 mA |
| $-0.5V$ to to $V_{CC} + 0.5V$ |
| ±50 mA |
| ±50 mA |
| |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

-65°C to +150°C

Storage Temperature (T_{STG})

Recommended Operating Conditions

| o o i i di ti o i i o | |
|--|-----------------------|
| Supply Voltage (V _{CC}) | |
| 'AC | 2.0V to 6.0V |
| 'ACT | 4.5V to 5.5V |
| Input Voltage (V _I) | 0V to V _{CC} |
| Output Voltage (V _O) | 0V to V _{CC} |
| Operating Temperature (T _A) | |
| 74AC/ACT | -40°C to +85°C |
| 54AC/ACT | -55°C to +125°C |
| Junction Temperature (T _J) | |
| CDIP | 175°C |
| PDIP | 140°C |
| Input Rise and Fall Time (t _r , t _f) (Note 2) (Typical) (Except Schmitt Inputs) 'AC Devic | es |
| V _{CC} @ 3.0V | 150 ns/V |
| V _{CC} @ 4.5V | 40 ns/V |
| V _{CC} @ 5.5V | 25 ns/V |
| (Note 2) (Typical) (Except Schmitt Inputs) 'ACT Devi V _{IN} from 0.8V to 2.0V, V _{meas} | ices |
| from 0.8V to 2.0V | 10 ns/V |
| V _{CC} @ 4.5V V _{CC} @ 5.5V | 10 ns/V 8 ns/V |
| vCC @ 0.3 v | O IIS/ V |

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

| ыV 10 д | Parameter | 74AC | | 54AC | 74AC | | | | |
|--------------------------|--------------------------------------|------------------------|-------------------------|----------------------|-----------------------------------|---------------------------------|---------|--|--|
| Symbol | | V _{CC} (V) | | | T _A = -55°C to + 125°C | T _A = -40°C to +85°C | Units | Conditions | |
| Ag f | 1 of V | 1.0 | Тур | | Guaranteed L | imits | d was n | Vo. Maximur | |
| V _{IH} Am 4S | Minimum High Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{IL} | Maximum Low Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{OH} | Minimum High Level Output Voltage | 3.0 4.5 5.5 | 2.99 4.49 5.49 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | ٧ | $I_{OUT} = -50 \mu\text{A}$ | |
| niM V28.s | = оноV Am oV a veV GMD so Aщ | 3.0 4.5 5.5 | | 2.56 3.86 4.86 | 2.4 3.7 4.7 | 2.46 3.76 4.76 | ٧ | $\label{eq:VIN} \begin{split} *V_{\text{IN}} &= V_{\text{IL}} \text{or} V_{\text{IH}} \\ &- 12 \text{mA} \\ I_{\text{OH}} &- 24 \text{mA} \\ &- 24 \text{mA} \end{split}$ | |
| V _{OL} | Maximum Low Level Output Voltage | 3.0 4.5 5.5 | 0.002 0.001 0.001 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | ٧ | I _{OUT} = 50 μA | |
| | | 3.0 4.5 5.5 | | 0.36 0.36 0.36 | 0.50 0.50 0.50 | 0.44 0.44 0.44 | V | $*V_{IN} = V_{IL} \text{ or } V_{IH}$ 12 mA I_{OL} 24 mA 24 mA | |
| I _{IN} | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | ±1.0 | μΑ | $V_I = V_{CC}$, GND | |

DC Characteristics for 'AC Family Devices (Continued)

| Symbol | | | 74AC | | 54AC | 74AC | liga sus | Lagran Transmit | |
|---------|-------------------------------------|---------------------|------------------|-----------------------|-----------------------------------|---------------------------------|------------|------------------------------|--|
| | Parameter | V _{CC} (V) | T _A = | + 25°C | T _A = -55°C to + 125°C | T _A = -40°C to +85°C | Units | Conditions | |
| 36V 913 | 0 | | Тур | garlov i | Guaranteed L | imits | Self) tops | iO abdiG kaqqi 0 1 | |
| IOLD | †Minimum Dynamic | 5.5 | (cV) eg | alov tao | 50 | 75 | mA | V _{OLD} = 1.65V Max | |
| IOHD | Output Current | 5.5 | 70.9GM6 | P. Private PANCIAL | -50 | € 75 C−75 | mA | V _{OHD} = 3.85V Min | |
| lcc | Maximum Quiescent Supply Current | 5.5 | ndetegn | 8.0 | 160.0 | 80.0 | μΑ | $V_{IN} = V_{CC}$ or GND | |

^{*}All outputs loaded; thresholds on input associated with output under test.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

| Symbol | | | 74ACT | | 54ACT | 74ACT | egnikas mu | mixem offmend 2.17 e3u32 - | |
|------------------|--------------------------------------|----------------------|--------------|-----------------------------------|---------------------------------|--------------|------------|---|--|
| | Parameter | Darameter T. = +25°C | | T _A = -55°C to + 125°C | T _A = -40°C to +85°C | Units | Conditions | | |
| | CT Devices | (altro | Тур | 239800 | Guaranteed L | imits | HANKO II O | | |
| V _{IH} | Minimum High Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 2.0 2.0 | 2.0 2.0 | 2.0 2.0 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{IL} | Maximum Low Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 0.8 0.8 | 0.8 0.8 | 0.8 0.8 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{OH} | Minimum High Level Output Voltage | 4.5 5.5 | 4.49 5.49 | 4.4 5.4 | 4.4 5.4 | 4.4 5.4 | ٧ | $I_{OUT} = -50 \mu\text{A}$ | |
| | med sinu | 4.5 5.5 | r Seen | 3.86 4.86 | 3.70 4.70 | 3.76 4.76 | V | $\begin{tabular}{ll} *V_{\text{IN}} &= V_{\text{IL}} \text{ or } V_{\text{IH}} \\ &-24 \text{ mA} \\ &-24 \text{ mA} \\ \end{tabular}$ | |
| V _{OL} | Maximum Low Level Output Voltage | 4.5 5.5 | 0.001 | 0.1 | 0.1 0.1 | 0.1 0.1 | V | I _{OUT} = 50 μA | |
| | 7 VOV | 4.5 5.5 | | 0.36 0.36 | 0.50 0.50 | 0.44 0.44 | V | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IN} = V_{IL} \text{ or } V_{IH}$ | |
| INVIO | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | ±1.0 | μА | $V_{I} = V_{CC}$, GND | |
| ICCT | Maximum I _{CC} /Input | 5.5 | 0.6 | | 0.3 1.6 | 98 S 1.5 8 | mA | $V_{\rm I} = V_{\rm CC} - 2.1V$ | |
| I _{OLD} | †Minimum Dynamic | 5.5 | | | 50 | 04.8 75 8 | mA | V _{OLD} = 1.65V Max | |
| IOHD | Output Current | 5.5 | | | -50 | -75 | mA | V _{OHD} = 3.85V Min | |
| Icc | Maximum Quiescent Supply Current | 5.5 | | 8.0 | 160.0 | 80.0 | μА | V _{IN} = V _{CC} or GND | |

^{*}All outputs loaded; thresholds on input associated with output under test.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

[†]Maximum test duration 2.0 ms, one output loaded at a time.

[†]Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics

| Symbol | | | | 74AC | | 54 | AC | 74 | AC | le des | 100 |
|------------------|--|-------------------|------------|-----------------------|-------------|--|------------------|--|--------------|-------------|-----|
| | Parameter | V _{CC} * | | C _L = +25° | | $T_A = -55^{\circ}C$ $to + 125^{\circ}C$ $C_L = 50 pF$ | to + | T _A = -40°C to +85°C C _L = 50 pF | | Fig. No. | |
| | | . Yu | Min | Тур | Max | Min | Max | Min | Max | 0 | 0 |
| t _{PLH} | Propagation Delay A_n or B_n to $\overline{O}_A = B$ | 3.3 5.0 | 4.0 2.5 | 7.5 5.5 | 11.5 8.5 | | | 3.0 2.0 | 13.0 9.5 | ns | 2-6 |
| t _{PHL} | Propagation Delay A_n or B_n to $\overline{O}_A = B$ | 3.3 5.0 | 4.5 | 8.0 5.5 | 12.0 9.0 | 70 -A | Ao Da | 3.5 2.5 | 13.5 10.0 | ns | 2-6 |
| t _{PLH} | Propagation Delay $\overline{I}_{A = B}$ to $\overline{O}_{A = B}$ | 3.3 5.0 | 3.5 2.5 | 5.5 4.5 | 8.5 6.5 | | | 2.5 2.0 | 9.5 7.0 | ns | 2-6 |
| t _{PHL} | Propagation Delay $\overline{I}_{A = B}$ to $\overline{O}_{A = B}$ | 3.3 5.0 | 3.5 2.5 | 5.5 4.5 | 8.5 6.5 | | 6=x ¹ | 2.5 2.0 | 9.5 7.0 | ns | 2-6 |

^{*}Voltage Range 3.3 is 3.3V \pm 0.3V Voltage Range 5.0 is 5.0V \pm 0.5V

AC Electrical Characteristics

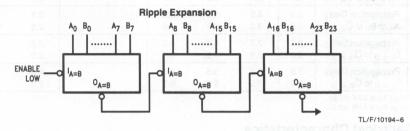
| Symbol | | | | 74ACT | | 54ACT | | 74ACT | | | Fig. No. 2-6 2-6 | |
|------------------|--|-------------------|-----|------------------------------------|------|---------------|-------------------------|-------|------------------------|-------|------------------|--|
| | Parameter | V _{CC} * | | A = +25° C _L = 50 pl | | to + | −55°C 125°C 50 pF | to + | -40°C 85°C 50 pF | Units | | |
| | | | Min | Тур | Max | Min | Max | Min | Max | | | |
| t _{PLH} | Propagation Delay A_n or B_n to $\overline{O}_A = B$ | 5.0 | 3.0 | 5.5 | 8.5 | Activities of | N=40 | 2.5 | 9.5 | ns | 2-6 | |
| t _{PHL} | Propagation Delay A_n or B_n to $\overline{O}_A = B$ | 5.0 | 3.0 | 6.0 | 10.0 | | | 2.5 | 11.5 | ns | 2-6 | |
| t _{PLH} | Propagation Delay $\overline{I}_{A = B}$ to $\overline{O}_{A = B}$ | 5.0 | 2.0 | 4.0 | 6.0 | | | 2.0 | 6.5 | ns | 2-6 | |
| t _{PHL} | Propagation Delay $\overline{I}_{A = B}$ to $\overline{O}_{A = B}$ | 5.0 | 2.5 | 5.0 | 7.5 | | | 2.0 | 8.5 | ns | 2-6 | |

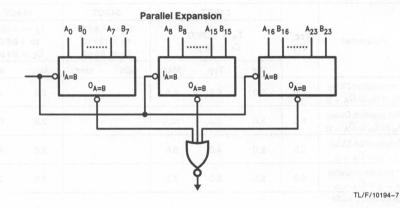
^{*}Voltage Range 5.0 is 5.0V $\pm 0.5 \text{V}$

Capacitance

| Symbol | Parameter | AC/ACT | Units | Conditions | |
|-----------------|-------------------------------|--------|--------|------------------------|--|
| Symbol | 0.04 = 41 0.32 = = | Тур | Olinta | | |
| CIN | Input Capacitance | 4.5 | pF | $V_{CC} = 5.0V$ | |
| C _{PD} | Power Dissipation Capacitance | 40 | pF | V _{CC} = 5.0V | |

Applications







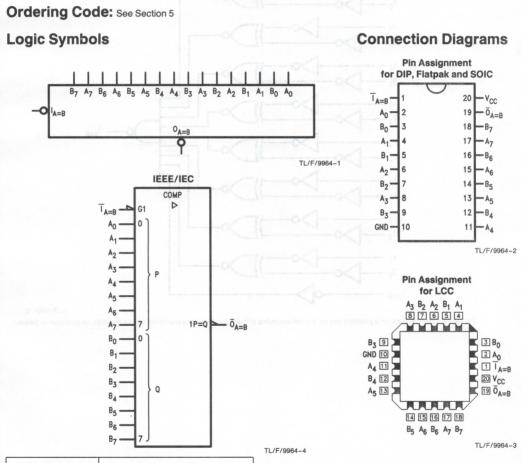
54AC/74AC521 • 54ACT/74ACT521 8-Bit Identity Comparator

General Description

The 'AC/'ACT521 is an expandable 8-bit comparator. It compares two words of up to eight bits each and provides a LOW output when the two words match bit for bit. The expansion input $\overline{I}_{A\ =\ B}$ also serves as an active LOW enable input.

Features

- Compares two 8-bit words in 6.5 ns typ
- Expandable to any word length
- 20-pin package
- Outputs source/sink 24 mA
- 'ACT521 has TTL-compatible inputs



| Pin Names | Description |
|--------------------------------|---------------------------|
| A ₀ -A ₇ | Word A Inputs |
| B ₀ -B ₇ | Word B Inputs |
| $T_A = B$ | Expansion or Enable Input |
| $\overline{O}_A = B$ | Identity Output |

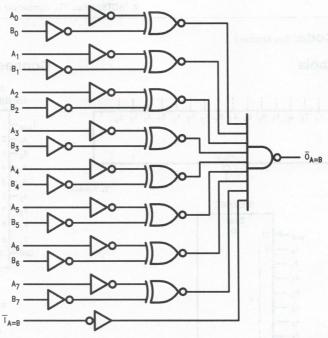
4

Truth Table

| Ing | outs | Outputs |
|-----------------|------------|----------------------|
| $\bar{I}_A = B$ | A, B | $\overline{O}_A = B$ |
| L | $A = B^*$ | Leven |
| L | $A \neq B$ | н |
| Н | $A = B^*$ | Н |
| Н | $A \neq B$ | Н |

$$\begin{split} &H = \text{HIGH Voltage Level} \\ &L = \text{LOW Voltage Level} \\ &*A_0 = B_0, \, A_1 = B_1, \, A_2 = B_2, \, \text{etc.} \end{split}$$

Logic Diagram



TL/F/9964-5 Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1) Recommended Operating

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Supply Voltage (V _{CC}) | 0 - 0 - 0 | .5V to +7.0V |
|--|-------------|------------------------|
| DC Input Diode Current (I_{IK}) $V_I = -0.5V$ | | -20 mA |
| $V_I = V_{CC} + 0.5V$ | | +20 mA |
| DC Input Voltage (V _I) | -0.5V to | V _{CC} + 0.5V |
| DC Output Diode Current (I_O $V_O = -0.5V$ $V_O = V_{CC} + 0.5V$ | κ) | -20 mA +20 mA |
| DC Output Voltage (V _O) | -0.5V to to | V _{CC} + 0.5V |
| DC Output Source or Sink Current (I _O) | | ±50 mA |
| DC V _{CC} or Ground Current per Output Pin (I _{CC} or I _{GND} |) | ±50 mA |
| Storage Temperature (T _{STG}) | -65° | C to +150°C |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

Recommended Operating Conditions

| Conditions | |
|--|-----------------------------------|
| Supply Voltage (V _{CC}) | |
| 'AC | 2.0V to 6.0V |
| 7101 | 4.5V to 5.5V |
| Input Voltage (V _I) | 0V to V _{CC} |
| Output Voltage (V _O) | 0V to V _{CC} |
| Operating Temperature (T _A) 74AC/ACT | -40°C to +85°C |
| 54AC/ACT | -55°C to +125°C |
| Junction Temperature (T _J) | |
| CDIP | 175°C |
| PDIP | 140°C |
| (Note 2) (Typical) (Except Schmitt Inputs) 'A | 1 |
| V _{CC} @ 3.0V | /CC 150 ns/V |
| V _{CC} @ 4.5V | 40 ns/V |
| V _{CC} @ 5.5V | 25 ns/V |
| Input Rise and Fall Time (t _r , (Note 2) (Typical) (Except Schmitt Inputs) 'A | towns in a second |
| V_{IN} from 0.8V to 2.0V, V_{mo} | |
| from 0.8V to 2.0V | eas Teve I doi: I muminist LaV |
| V _{CC} @ 4.5V | 10 ns/V |
| 1/0 0 5 5 1/ | 10 1137 V |

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

| | Parameter | | 74 | AC | 54AC | 74AC | | |
|--------------------------|--------------------------------------|------------------------|-------------------------|----------------------|----------------------------------|---------------------------------|---|--|
| Symbol | | V _{CC} (V) | $T_A =$ | + 25°C | T _A = -55°C to +125°C | T _A = -40°C to +85°C | Units | Conditions |
| Au 0F = TUOI V | | 1.0 | Тур | | Guaranteed L | Guaranteed Limits | | |
| VIH HIV TO H Am AS | Minimum High Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ |
| V _{IL} | Maximum Low Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | n byst Current | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ |
| V _{OH} | Minimum High Level Output Voltage | 3.0 4.5 5.5 | 2.99 4.49 5.49 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | V to the state of | $I_{OUT} = -50 \mu\text{A}$ |
| | E GHOV Am | 3.0 4.5 5.5 | | 2.56 3.86 4.86 | 2.4 3.7 4.7 | 2.46 3.76 4.76 | anent a Oujesc | $\label{eq:VIN} \begin{split} *V_{IN} &= V_{IL} or V_{IH} \\ &- 12 mA \\ I_{OH} &- 24 mA \\ &- 24 mA \end{split}$ |
| V _{OL} | Maximum Low Level Output Voltage | 3.0 4.5 5.5 | 0.002 0.001 0.001 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | Ves | I _{OUT} = 50 μA |
| | | 3.0 4.5 5.5 | | 0.36 0.36 0.36 | 0.50 0.50 0.50 | 0.44 0.44 0.44 | ٧ | $\begin{tabular}{lllllllllllllllllllllllllllllllllll$ |
| I _{IN} | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | ±1.0 | μΑ | $V_{I} = V_{CC}$, GND |

DC Characteristics for 'AC Family Devices (Continued)

| Symbol Parameter | | | 74AC | | 54AC | 74AC | aif en | instruo sauski |
|------------------|-------------------------------------|------------------------|-------------|----------------------------------|---------------------------------|---------------|-------------------|------------------------------|
| | V _{CC} (V) | T _A = +25°C | | T _A = -55°C to +125°C | T _A = -40°C to +85°C | Units | Conditions | |
| | | Тур | psilo?"L | Guaranteed L | imits | byi) they | DC (nout Biode Cu | |
| IOLD | †Minimum Dynamic | 5.5 | (6)4-6) | ellov Jung | 50 | 75 | mA | V _{OLD} = 1.65V Max |
| I _{OHD} | Output Current | 5.5 | ine isoline | DANDAS | -50 | / cf Vd. (-75 | mA | V _{OHD} = 3.85V Min |
| Icc | Maximum Quiescent Supply Current | 5.5 | | 8.0 | 160.0 | 80.0 | μΑ | $V_{IN} = V_{CC}$ or GND |

^{*}All outputs loaded; thresholds on input associated with output under test.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC} . I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

| | Parameter | | 74 | ACT | 54ACT | 74ACT | aggiller mu | avigra olalozus al e-i uz |
|----------------------------|--------------------------------------|------------------------|----------------|--------------|---------------|--------------|-------------|--|
| Symbol | | V _{CC} (V) | | | Units | Conditions | | |
| | CT Devices | (e) (e) (f) | Тур | 8 feath | Guaranteed Li | mits | | The state of the s |
| V _{IH} V\ea 01 | Minimum High Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 2.0 | 2.0 2.0 | 2.0 2.0 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ |
| VIL | Maximum Low Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 0.8 0.8 | 0.8 0.8 | 0.8 0.8 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ |
| V _{OH} | Minimum High Level Output Voltage | 4.5 5.5 | 4.49 5.49 | 4.4 5.4 | 4.4 5.4 | 4.4 5.4 | V | $I_{OUT} = -50 \mu\text{A}$ |
| sectili | units Con | 4.5 5.5 | † † | 3.86 4.86 | 3.70 4.70 | 3.76 4.76 | ٧ | $\begin{tabular}{ll} *V_{IN} &= V_{IL} \mbox{ or } V_{IH} \\ &-24 \mbox{ mA} \\ -24 \mbox{ mA} \end{tabular}$ |
| V _{OL} | Maximum Low Level Output Voltage | 4.5 5.5 | 0.001 0.001 | 0.1 | 0.1 0.1 | 0.1 0.1 | ٧ | $I_{OUT} = 50 \mu A$ |
| VI.O. | 2. A to A | 4.5 5.5 | | 0.36 0.36 | 0.50 0.50 | 0.44 0.44 | V | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IN} = V_{IL} \text{ or } V_{IH}$ |
| IN | Maximum Input Leakage Current | 5.5 | n. | ±0.1 | ±1.0 | 85.5 ±1.0 | μА | $V_{I} = V_{CC}$, GND |
| ГССТ | Maximum I _{CC} /Input | 5.5 | 0.6 | | 1.6 | 80 S 1.5 8 | mA | $V_{\rm I} = V_{\rm CC} - 2.1V$ |
| lold | †Minimum Dynamic | 5.5 | | | 50 | 94.8 75 8 | mA | V _{OLD} = 1.65V Max |
| IOHD | Output Current | 5.5 | | | -50 | -75 | mA | V _{OHD} = 3.85V Min |
| Icc | Maximum Quiescent Supply Current | 5.5 | | 8.0 | 160.0 | 80,0 | μА | V _{IN} = V _{CC} or GND |

^{*}All outputs loaded; thresholds on input associated with output under test.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

[†]Maximum test duration 2.0 ms, one output loaded at a time.

[†]Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics

| | | 74AC - 54 | AC | 74 | AC | | | | | | | |
|------------------|--|-------------------|------------|-----------------------|-------------|----------|-------------------------|------------|------------------------|-------|-------------|-----|
| Symbol | Parameter | V _{CC} * | | A = +25° CL = 50 p | | to + | -55°C 125°C 50 pF | to + | -40°C 85°C 50 pF | Units | Fig. No. | |
| | | | | Min | Тур | Max | Min | Max | Min | Max | | 2-6 |
| t _{PLH} | Propagation Delay $A_n \text{ or } B_n \text{ to } \overline{O}_A = B$ | 3.3 5.0 | 3.5 2.5 | 7.0 5.0 | 11.0 8.0 | I a | V - See | 3.0 2.0 | 12.0 9.0 | ns | 2-6 | |
| t _{PHL} | Propagation Delay A_n or B_n to $\overline{O}_A = B$ | 3.3 5.0 | 4.5 3.0 | 7.5 5.5 | 11.5 8.5 | | | 3.5 2.5 | 12.5 9.0 | ns | 2-6 | |
| t _{PLH} | Propagation Delay $\overline{I}_{A = B}$ to $\overline{O}_{A = B}$ | 3.3 5.0 | 3.0 2.5 | 5.5 4.0 | 8.0 6.0 | ments as | grammer. | 2.5 2.0 | 9.0 7.0 | ns | 2-6 | |
| t _{PHL} | Propagation Delay $\overline{I}_A = B$ to $\overline{O}_A = B$ | 3.3 5.0 | 3.0 2.0 | 5.5 4.0 | 8.0 6.0 | | | 2.5 2.0 | 9.0 7.0 | ns | 2-6 | |

*Voltage Range 3.3 is 3.3V ± 0.3 V Voltage Range 5.0 is 5.0V ± 0.5 V

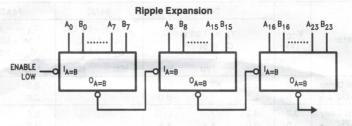
AC Electrical Characteristics

| | | | | 74ACT | | | ACT | 74ACT | | | |
|------------------|--|--------------------------|-----|-----------------------|------|------|-------------------------|-------|------------------------|-------|-------------|
| Symbol | Parameter | V _{CC} * (V) | | C _L = +25° | | to + | −55°C 125°C 50 pF | to + | -40°C 85°C 50 pF | Units | Fig. No. |
| | | | Min | Тур | Max | Min | Max | Min | Max | 1 | |
| t _{PLH} | Propagation Delay A_n or B_n to $\overline{O}_A = B$ | 5.0 | 3.0 | 5.5 | 9.0 | | | 2.5 | 9.5 | ns | 2-6 |
| t _{PHL} | Propagation Delay A_n or B_n to $\overline{O}_A = B$ | 5.0 | 3.0 | 6.0 | 10.0 | | | 2.5 | 11.0 | ns | 2-6 |
| t _{PLH} | Propagation Delay $\overline{I}_{A = B}$ to $\overline{O}_{A = B}$ | 5.0 | 2.0 | 4.0 | 6.5 | | | 2.0 | 7.0 | ns | 2-6 |
| t _{PHL} | Propagation Delay $\overline{I}_{A = B}$ to $\overline{O}_{A = B}$ | 5.0 | 2.5 | 5.0 | 7.5 | | | 2.0 | 8.0 | ns | 2-6 |

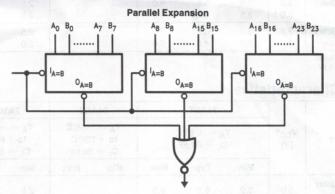
*Voltage Range 5.0 is 5.0V ±0.5V

| Symbol | Parameter | AC/ACT | Units | Conditions |
|-----------------|-------------------------------|--------|--------|-----------------|
| Symbol | raiametei | Тур | Oilito | Conditions |
| C _{IN} | Input Capacitance | 4.5 | pF | $V_{CC} = 5.0V$ |
| C _{PD} | Power Dissipation Capacitance | 40 | pF | $V_{CC} = 5.0V$ |

Applications



TL/F/9964-6



TL/F/9964-7



54ACT/74ACT534 Octal D Flip-Flop with TRI-STATE® Outputs

General Description

The 'ACT534 is a high-speed, low-power octal D-type flipflop featuring separate D-type inputs for each flip-flop and TRI-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable (OE) are common to all flip-flops. The 'ACT534 is the same as the 'ACT374 except that the outputs are inverted.

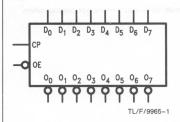
Features

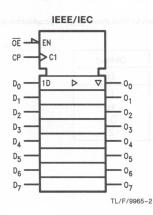
- Edge-triggered D-type inputs
- Buffered positive edge-triggered clock
- TRI-STATE outputs for bus-oriented applications
- Outputs source/sink 24 mA
- 'ACT534 has TTL-compatible inputs
- Inverted output version of 'ACT374

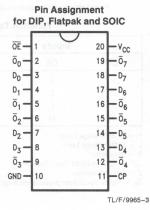
Ordering Code: See Section 5

Logic Symbols

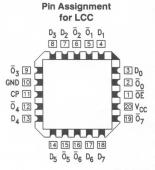
Connection Diagrams







| Pin Names | Description | | | | | | |
|-----------------------------------|---------------------------------|--|--|--|--|--|--|
| D ₀ -D ₇ | Data Inputs | | | | | | |
| CP | Clock Pulse Input | | | | | | |
| ŌĒ | TRI-STATE Output Enable Input | | | | | | |
| $\overline{O}_0 - \overline{O}_7$ | Complementary TRI-STATE Outputs | | | | | | |



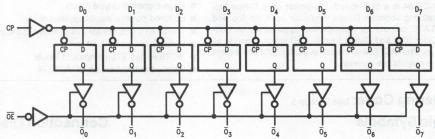
TL/F/9965-4

Functional Description

The 'ACT534 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE complementary outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH Clock (CP)

transition. With the Output Enable (\overline{OE}) LOW, the contents of the eight flip-flops are available at the outputs. When the \overline{OE} is HIGH, the outputs go to the high impedance state. Operation of the \overline{OE} input does not affect the state of the flip-flops.

Logic Diagram



TL/F/9965-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Function Table

| 1 30/ 105 | Inputs | Output | | |
|-----------|--------|--------|---|------------------|
| CP | OE | - 0E | D | ō |
| _ | L | 00 | Н | L |
| _ | L | | L | Н |
| L | L | | X | \overline{O}_0 |
| X | Н | | X | Z |

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

= LOW-to-HIGH Clock Transition

Z = High Impedance

 \overline{O}_0 = Value stored from previous clock cycle

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Office/Distributors for available | lity and specifications. |
|---|------------------------------|
| Supply Voltage (V _{CC}) | -0.5V to +7.0\ |
| DC Input Diode Current (I_{IK}) $V_I = -0.5V$ $V_I = V_{CC} + 0.5V$ | -20 mA +20 mA |
| DC Input Voltage (V _I) | -0.5 V to $V_{CC} + 0.5$ V |
| DC Output Diode Current (IOK) | |

 $\begin{array}{c} {\rm V_O} = -0.5{\rm V} & -20~{\rm mA} \\ {\rm V_O} = {\rm V_{CC}} + 0.5{\rm V} & +20~{\rm mA} \\ {\rm DC~Output~Voltage~(V_O)} & -0.5{\rm V~to~to~V_{CC}} + 0.5{\rm V} \\ \end{array}$

or Sink Current (I_O) ± 50 mA

DC V_{CC} or Ground Current
per Output Pin (I_{CC} or I_{GND}) ± 50 mA

Storage Temperature (T_{STG}) -65° C to $+150^{\circ}$ C

DC Output Source

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

Recommended Operating Conditions

| 0011011101110 | |
|---|------------------------------|
| Supply Voltage (V _{CC}) 'AC | 2.0V to 6.0V |
| ACT | 2.0V to 6.0V 4.5V to 5.5V |
| Input Voltage (V _I) | 0V to V _{CC} |
| | |
| | 0V to V _{CC} |
| Operating Temperature (T _A) | |
| 74AC/ACT | -40°C to +85°C |
| 54AC/ACT | -55°C to +125°C |
| Junction Temperature (T _{.I}) | |
| CDIP | 175°C |
| PIDIP | 140°C |
| Input Rise and Fall Time (t _r , t _f) (Note 2) (Typical) (Except Schmitt Inputs) 'AC D V _{IN} from 30% to 70% of V _{CC} | |
| V _{CC} @ 3.0V | 150 ns/V |
| V _{CC} @ 4.5V | 40 ns/V |
| V _{CC} @ 5.5V | 25 ns/V |
| Input Rise and Fall Time (t _r , t _f) (Note 2) (Typical) (Except Schmitt Inputs) 'ACT | Devices |
| V _{IN} from 0.8V to 2.0V, V _{meas} from 0.8V to 2.0V | |
| V _{CC} @ 4.5V | 10 ns/V |
| | 8 ns/V |
| | |

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'ACT Family Devices

| 1-5 | en der 0.5 0.41 | | 74 | CT | 54ACT | 74ACT | BUBUE | advard HZm | |
|-----------------|--------------------------------------|------------------------|-------------------------|--------------|----------------------------------|---------------------------------|--------|---|--|
| Symbol | Parameter | V _{CC} (V) | T _A = + 25°C | | T _A = -55°C to +125°C | T _A = -40°C to +85°C | Units | Conditions | |
| | an i dior on land | | Тур | 10.5 | Guaranteed | Limits | idne/0 | ading Zidi. | |
| V _{IH} | Minimum High Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 2.0 2.0 | 2.0 2.0 | 2.0 2.0 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{IL} | Maximum Low Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 0.8 | 0.8 | 0.8 0.8 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{OH} | Minimum High Level Output Voltage | 4.5 5.5 | 4.49 5.49 | 4.4 5.4 | 4.4 5.4 | 4.4 5.4 | V | $I_{OUT} = -50 \mu\text{A}$ | |
| 9-5 | ed Manigrams 4.0 ns | 4.5 5.5 | 900 | 3.86 4.86 | 3.70 4.70 | 3.76 4.76 | V | $V_{\text{IN}} = V_{\text{IL}} \text{ or } V_{\text{IH}}$ -24 mA -24 mA | |
| V _{OL} | Maximum Low Level Output Voltage | 4.5 5.5 | 0.001 0.001 | 0.1 0.1 | 0.1 0.1 0.6 | 0.1 0.1 | ٧ | $I_{OUT} = 50 \mu A$ | |
| 2-6 | an 3.5 | 4.5 5.5 | | 0.36 0.36 | 0.50 0.50 | 0.44 0.44 | ٧ | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IN} = V_{IL} \text{ or } V_{IH}$ | |
| I _{IN} | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | ±1.0 | μΑ | $V_I = V_{CC}$, GND | |
| loz | Maximum TRI-STATE® Current | 5.5 | | ±0.5 | ±10.0 | ±5.0 | μА | $V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}, GND$ | |
| ГССТ | Maximum I _{CC} /Input | 5.5 | 0.6 | | 1.6 | 1.5 | mA | $V_{\rm I} = V_{\rm CC} - 2.1V$ | |

| Symbol | Parameter | | 74ACT T _A = + 25°C | | 54ACT | 74ACT | Units | Conditions | |
|--------|-------------------------------------|------------------------|--------------------------------|--------|----------------------------------|---------------------------------|-----------|------------------------------|--|
| | | V _{CC} (V) | | | T _A = -55°C to +125°C | T _A = -40°C to +85°C | | | |
| | | | Тур | estlov | Guaranteed I | Limits | (hil) the | DC input Diade Curt | |
| IOLD | †Minimum Dynamic | 5.5 | lov) se | Mov i | 50 | 75 | mA | V _{OLD} = 1.65V Max | |
| IOHD | Output Current | 5.5 | STUGME | DAYO) | -50 | ov or √2475 | mA | V _{OHD} = 3.85V Min | |
| Icc | Maximum Quiescent Supply Current | 5.5 | T Manager | 8.0 | 160.0 | 80.0 | μА | $V_{IN} = V_{CC}$ or GND | |

^{*}All outputs loaded; thresholds on input associated with output under test.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

| | | | V0.6 | 74ACT | | 54/ | ACT | 74ACT T _A = -40°C | 2101 | | |
|------------------|---|-------------------|----------------------------------|-----------------------------------|------|------|-------------------------|-------------------------------|------------------------|--------------|-------------|
| Symbol | Parameter | V _{CC} * | | A = +25° C _L = 50 p | | to + | −55°C 125°C 50 pF | to + | -40°C 85°C 50 pF | Units | Fig. No. |
| | ACT Devices | (stadul | Min | Тур | Max | Min | Max | Min | Max | e in masuujo | press |
| f _{max} | Maximum Clock Frequency | 5.0 | 0.5 of V8: 0.5 of V8: ¥6.5 | 100 | | 85 | | 120 | | MHz | 2-3 |
| tpLH 8 | Propagation Delay CP to \overline{Q}_n | 5.0 | 2.5 | 6.5 | 11.5 | 1.0 | 14.0 | 2.0 | 12.5 | ns | 2-6 |
| t _{PHL} | Propagation Delay CP to $\overline{\mathbb{Q}}_n$ | 5.0 | 2.0 | 6.0 | 10.5 | 1.0 | 13.0 | 2.0 | 12.0 | ns | 2-6 |
| t _{PZH} | Output Enable Time | 5.0 | 2.5 | 6.5 | 12.0 | 1.0 | 14.0 | 2.0 | 12.5 | ns | 2-7 |
| t _{PZL} | Output Enable Time | 5.0 | 2.0 | 6.0 | 11.0 | 1.0 | 13.0 | 2.0 | 11.5 | ns | 2-8 |
| t _{PHZ} | Output Disable Time | 5.0 | 1.5 | 7.0 | 12.5 | 1.0 | 14.5 | 1.0 | 13.5 | ns | 2-7 |
| t _{PLZ} | Output Disable Time | 5.0 | 1.5 | 5.5 | 10.5 | 1.0 | 11.5 | 1.0 | 10.5 | ns | 2-8 |

^{*}Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

| | TUOV 8.0 | | 74 | ACT | 54ACT | 74ACT | i input ve juago | 38 |
|----------------------|---|--------------------------|-------|-----------------|--|--|-----------------------------|------|
| Symbol | Parameter | V _{CC} * (V) | | + 25°C 50 pF | $T_A = -55^{\circ}C$ to $+ 125^{\circ}C$ $C_L = 50 pF$ | $T_{A} = -40^{\circ}C$ to $+85^{\circ}C$ $C_{L} = 50 \text{ pF}$ | Units | Fig. |
| | MIV* | | Тур | | Guaranteed Min | imum | | |
| ts | Setup Time, HIGH or LOW D _n to CP | 5.0 | 0.1.0 | 3.5 | 5.0 | 4.0 | ns | 2-9 |
| t _h Au 08 | Hold Time, HIGH or LOW D _n to CP | 5.0 | -1.0 | 1.0 | 3.0 | level wod n 1.5 epaño | ns | 2-9 |
| t _w | CP Pulse Width HIGH or LOW | 5.0 | 2.0 | 3.5 | 5.0 | 3.5 | ns | 2-6 |

^{*}Voltage Range 5.0 is 5.0V \pm 0.5V

[†]Maximum test duration 2.0 ms, one output loaded at a time.

| Symbol | Parameter | AC/ACT | Units | Conditions | |
|-----------------|----------------------------------|--------|-------|-----------------|--|
| Symbol | Farameter | Тур | Onits | Conditions | |
| CIN | Input Capacitance | 4.5 | pF | $V_{CC} = 5.0V$ | |
| C _{PD} | Power Dissipation Capacitance | 40.0 | pF | $V_{CC} = 5.0V$ | |





54AC/74AC540 • 54ACT/74ACT540 Octal Buffer/Line Driver with TRI-STATE® Outputs

General Description

The 'AC/'ACT540 is an octal buffer/line drivers designed to be employed as memory and address drivers, clock drivers and bus oriented transmitter/receivers.

These devices are similar in function to the 'AC/'ACT240 while providing flow-through architecture (inputs on opposite side from outputs). This pinout arrangement makes these devices especially useful as output ports for microprocessors, allowing ease of layout and greater PC board density.

Features

- TRI-STATE inverting outputs
- Inputs and outputs opposite side of package, allowing easier interface to microprocessors
- Output source/sink 24 mA
- 'ACT540 has TTL-compatible inputs

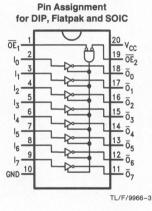
The information for the 'ACT540 is Advanced Information only.

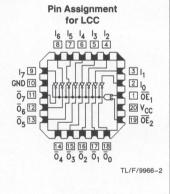
Ordering Code: See Section 5

Logic Symbol

IEEE/IEC EN ōo D 0, 0, 12 Ōz 13 O, 14 - Ō5 15 - Ō6 - 07 TL/F/9966-1

Connection Diagrams





Truth Table

| | Inputs | | Outputs |
|-----------------|-----------------|-----|---------|
| OE ₁ | OE ₂ | - 1 | Outputs |
| L | L | Н | L |
| Н | X | X | Z |
| X | Н | X | Z |
| L | L | L | Н |

- H = HIGH Voltage Level
- L = LOW Voltage Level
- X = Immaterial
- Z = High Impedance

Absolute Maximum Rating (Note 1) (Note 1)

Supply Voltage (Vcc)

Storage Temperature (T_{STG})

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

-0.5V to +7.0V

-65°C to +150°C

| Supply voltage (vCC) | 0.57 10 17.07 |
|---|---------------------------------|
| DC Input Diode Current (IIK) | |
| $V_{I} = -0.5V$ | -20 mA |
| $V_I = V_{CC} + 0.5V$ | + 20 mA |
| DC Input Voltage (V _I) | $-0.5V$ to $V_{CC} + 0.5V$ |
| DC Output Diode Current (IO | K) |
| $V_0 = -0.5V$ | -20 mA |
| $V_O = V_{CC} + 0.5V$ | + 20 mA |
| DC Output Voltage (V _O) | -0.5 V to to $V_{CC} + 0.5$ V |
| DC Output Source | |
| or Sink Current (IO) | ± 50 mA |
| DC V _{CC} or Ground Current | |
| per Output Pin (I _{CC} or I _{GND} | ± 50 mA |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

Recommended Operating Conditions

| 001101110110 | |
|--|-------------------------------------|
| Supply Voltage (V _{CC}) 'AC 'ACT | 2.0V to 6.0V 4.5V to 5.5V |
| | |
| Input Voltage (V _I) | 0V to V _{CC} |
| Output Voltage (V _O) | 0V to V _{CC} |
| Operating Temperature (T _A) 74AC/ACT 54AC/ACT | -40°C to +85°C -55°C to +125°C |
| Junction Temperature (T _{.I}) | |
| CDIP | 175°C |
| PDIP | 140°C |
| | CO OFF Maximum Objescent |
| Input Rise and Fall Time (t _r , t _f) (Note 2) (Typical) (Except Schmitt Inputs) 'AC I V _{IN} from 30% to 70% of V _{Cl} V _{CC} @ 3.0V | 150 ns/V |
| V _{CC} @ 4.5V | 40 ns/V |
| V _{CC} @ 5.5V | 25 ns/V |
| Input Rise and Fall Time (t _r , t _f) (Note 2) (Typical) (Except Schmitt Inputs) 'ACT V _{IN} from 0.8V to 2.0V, V _{meas} | |
| from 0.8V to 2.0V | Symbol Parameter |
| V _{CC} @ 4.5V | 10 ns/V |
| V _{CC} @ 5.5V | 8 ns/V |
| Note 2: See individual datasheets for | those devices which differ from the |
| | |

typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

| Symbol | Parameter | à | 74. | AC | 54AC | 74AC | | at staC | |
|-----------------|--|------------------------|-------------------------|----------------------|-----------------------------------|---------------------------------|--|--|--|
| | | V _{CC} (V) | T _A = +25°C | | T _A = -55°C to + 125°C | T _A = -40°C to +85°C | Units | Conditions | |
| | 2.0 11.0 | 0.1 | Тур | 0.1 | Guaranteed L | imits | T alden. | | |
| V _{IH} | Minimum High Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | T oldaal | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{IL} | Maximum Low Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| 011 | Minimum High Level 3.0 Output Voltage 4.5 5.5 3.0 4.5 5.5 | 4.5 | 2.99 4.49 5.49 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | V | $I_{OUT} = -50 \mu\text{A}$ | |
| | | / | 2.56 3.86 4.86 | 2.4 3.7 4.7 | 2.46 3.76 4.76 | igni <mark>v</mark> | $\label{eq:VIN} \begin{split} *V_{IN} &= V_{IL} or V_{IH} \\ &- 12 mA \\ I_{OH} &- 24 mA \\ &- 24 mA \end{split}$ | | |
| V _{OL} | Maximum Low Level Output Voltage | 3.0 4.5 5.5 | 0.002 0.001 0.001 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | ٧ | $I_{OUT} = 50 \mu\text{A}$ | |
| | | 3.0 4.5 5.5 | | 0.36 0.36 0.36 | 0.50 0.50 0.50 | 0.44 0.44 0.44 | ٧ | $\begin{tabular}{ll} *V_{IN} &= V_{IL} \mbox{ or } V_{IH} \\ &= 12 \mbox{ mA} \\ I_{OL} &= 24 \mbox{ mA} \\ &= 24 \mbox{ mA} \\ \end{tabular}$ | |
| I _{IN} | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | ±1.0 | μА | $V_{I} = V_{CC}$, GND | |

DC Characteristics for 'AC Family Devices (Continued)

| Symbol | Parameter | | 74AC T _A = +25°C | | 54AC | 74AC | Units | piense ventact |
|------------------|-------------------------------------|---------------------|--------------------------------|------------------------|----------------------------------|---------------------------------|---------|--|
| | | V _{CC} (V) | | | T _A = -55°C to +125°C | T _A = -40°C to +85°C | | Conditions |
| | | | Тур | allev sign | Guaranteed Lin | mits | il) man | DC Input Diade Ou |
| loz | Maximum TRI-STATE® Current | 5.5 | lade (Vo) Lempalot CT | ±0.5 | ±10.0 | ±5.0 | μА | V_{I} (OE) = V_{IL} , V_{IH} $V_{I} = V_{CC}$, GND $V_{O} = V_{CC}$, GND |
| I _{OLD} | †Minimum Dynamic | 5.5 | in diament | rational de la company | 50 | 75 | mA | V _{OLD} = 1.65V Max |
| IOHD | Output Current | 5.5 | | 960 | -50 | -75 | mA | V _{OHD} = 3.85V Min |
| Icc | Maximum Quiescent Supply Current | 5.5 | He i bas | 8.0 | 160.0 | 80.0 | μА | $V_{IN} = V_{CC}$ or GND |

^{*}All outputs loaded; thresholds on input associated with output under test.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC} . I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

AC Electrical Characteristics

| Symbol | Parameter | | anayt) (S | 74AC | | 54 | AC | 74 | AC | de noteriaga | отъп | |
|------------------|-------------------------------------|------------|--------------------------|------------|--|------------|--------------|------------|---|--------------|--|--|
| | | Parameter | V _{CC} * (V) | | T _A = +25°C C _L = 50 pF | | | | $T_A = -55^{\circ}C$ to + 125°C $C_L = 50 pF$ | | $T_{A} = -40^{\circ} \text{C}$ $to +85^{\circ} \text{C}$ $C_{L} = 50 \text{ pF}$ | |
| Viten 8 | | | Min | Тур | Max | Min | Max | Min | Max | | | |
| t _{PLH} | Propagation Delay Data to Output | 3.3 5.0 | 1.5 1.5 | 5.5 4.0 | 7.5 6.0 | 1.0 | 9.0 7.0 | 1.0 | 8.0 6.5 | ns | 2-5 | |
| t _{PHL} | Propagation Delay Data to Output | 3.3 5.0 | 1.5 1.5 | 5.0 4.0 | 7.0 5.5 | 1.0 1.0 | 8.0 6.5 | 1.0 1.0 | 7.5 6.0 | ns | 2-5 | |
| t _{PZH} | Output Enable Time | 3.3 5.0 | 3.0 2.0 | 8.5 6.5 | 11.0 8.5 | 1.0 1.0 | 13.0 10.0 | 2.5 2.0 | 12.0 9.5 | ns | 2-7 | |
| t _{PZL} | Output Enable Time | 3.3 5.0 | 2.5 | 7.5 6.0 | 10.0 7.5 | 1.0 1.0 | 12.0 9.0 | 2.0 1.5 | 11.0 8.5 | ns | 2-8 | |
| t _{PHZ} | Output Disable Time | 3.3 5.0 | 2.5 1.5 | 8.5 7.5 | 13.0 10.5 | 1.0 1.0 | 15.5 12.0 | 1.5 1.0 | 14.0 11.0 | ns | 2-7 | |
| t _{PLZ} | Output Disable Time | 3.3 5.0 | 2.5 1.5 | 7.0 6.0 | 10.0 8.0 | 1.0 1.0 | 12.0 10.0 | 2.0 1.5 | 11.0 9.0 | ns | 2-8 | |

^{*}Voltage Range 3.3 is 3.3V ± 0.3 V Voltage Range 5.0 is 5.0V ± 0.5 V

| Symbol | Parameter | AC/ACT | Units | Conditions | | |
|-----------------|----------------------------------|--------|-------|------------------------|--|--|
| Symbol | raiameter | Тур | Onits | Conditions | | |
| C _{IN} | Input Capacitance | 4.5 | pF | $V_{CC} = 5.0V$ | | |
| C _{PD} | Power Dissipation Capacitance | 30.0 | pF | V _{CC} = 5.0V | | |

[†]Maximum test duration 2.0 ms, one output loaded at a time.



54AC/74AC541 ◆ 54ACT/74ACT541 Octal Buffer/Line Driver with TRI-STATE® Outputs

General Description

The 'AC/'ACT541 is an octal buffer/line driver designed to be employed as memory and address drivers, clock drivers and bus oriented transmitter/receivers. The 'AC/'ACT541 is a noninverting option of the 'AC/'ACT540.

This device is similar in function to the 'AC/'ACT244 while providing flow-through architecture (inputs on opposite side from outputs). This pinout arrangement makes this device especially useful as an output port for microprocessors, allowing ease of layout and greater PC board density.

The information for the ACT541 is Advanced Information only.

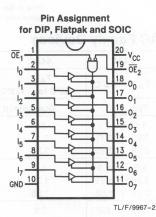
Features

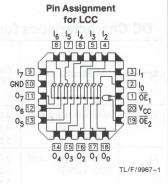
- TRI-STATE outputs
- Inputs and outputs opposite side of package, allowing easier interface to microprocessors
- Output source/sink 24 mA
- 'ACT541 has TTL-compatible inputs
- 'AC/'ACT540 provides inverted outputs

Ordering Code: See Section 5

Logic Symbol

Connection Diagrams





Truth Table

| | Inputs | Outputs | | |
|-----------------|-----------------|---------|---------|--|
| OE ₁ | OE ₂ | 0/15 | Cutputs | |
| L | L | Н | Н | |
| Н | X | X | Z | |
| X | Н | X | Z | |
| L | L | L | L | |

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Z = High Impedance

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| -0.5V to $+7.0V$ |
|-----------------------------------|
| |
| -20 mA |
| + 20 mA |
| -0.5 V to V_{CC} + 0.5 V |
| |
| -20 mA |
| + 20 mA |
| -0.5 V to to V_{CC} + 0.5 V |
| |
| ± 50 mA |
| |
| ±50 mA |
| -65°C to +150°C |
| |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

Recommended Operating Conditions

| Supply Voltage (V _{CC}) | |
|--|-----------------------|
| 'AC | 2.0V to 6.0V |
| 'ACT | 4.5V to 5.5V |
| Input Voltage (V _I) | 0V to V _{CC} |
| Output Voltage (V _O) | 0V to V _{CC} |
| Operating Temperature (T _A) | |
| 74AC/ACT | -40°C to +85°C |
| 54AC/ACT | -55°C to +125°C |
| Junction Temperature (T _J) | |
| CDIP | 175°C |
| PDIP | 140°C |
| Input Rise and Fall Time (t _r , t _f) (Note 2) (Typical) | |

(Except Schmitt Inputs) 'AC Devices
V_{IN} from 30% to 70% of V_{CC}
V_{CC} @ 3.0V
150
40

 VCC @ 3.0V
 150 ns/V

 VCC @ 4.5V
 40 ns/V

 VCC @ 5.5V
 25 ns/V

Input Rise and Fall Time (t_r, t_f)
(Note 2) (Typical)
(Except Schmitt Inputs) 'ACT Devices
V_{IN} from 0.8V to 2.0V, V_{meas}
from 0.8V to 2.0V
V_{CC} @ 4.5V
V_{CC} @ 5.5V

8 ns/V

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

| Symbol | Parameter | | 74 | AC | 54AC | 74AC | | |
|-----------------|--------------------------------------|---------------------|-------------------------|----------------------|---------------------------------|----------------------|----------------------------|--|
| | | V _{CC} (V) | | | T _A = -40°C to +85°C | Units | Conditions | |
| , 50 CU) | 12. 山山山山南田。 | | Тур | 41 | Guaranteed Li | imits | eng turn ar ar a sa | all section of |
| VIH | Minimum High Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ |
| V _{IL} | Maximum Low Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ |
| V _{OH} | Minimum High Level Output Voltage | 3.0 4.5 5.5 | 2.99 4.49 5.49 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | ٧ | $I_{OUT} = -50 \mu\text{A}$ |
| | | 3.0 4.5 5.5 | | 2.56 3.86 4.86 | 2.4 3.7 4.7 | 2.46 3.76 4.76 | ٧ | $\label{eq:VIN} \begin{split} *V_{IN} &= V_{IL} or V_{IH} \\ &- 12 mA \\ I_{OH} &- 24 mA \\ &- 24 mA \end{split}$ |
| V _{OL} | Maximum Low Level Output Voltage | 3.0 4.5 5.5 | 0.002 0.001 0.001 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | V | $I_{OUT} = 50 \mu A$ |
| | | 3.0 4.5 5.5 | | 0.36 0.36 0.36 | 0.50 0.50 0.50 | 0.44 0.44 0.44 | levou sos levou ap V | $*V_{IN} = V_{IL} \text{ or } V_{IH}$ 12 mA I_{OL} 24 mA 24 mA |
| I _{IN} | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | ±1.0 | μΑ | $V_{I} = V_{CC}$, GND |

DC Characteristics for 'AC Family Devices (Continued)

| Symbol | Parameter | | | | 74AC | m n | | |
|------------------|---------------------------------------|---------------------|----------|------------|--------------|----------|-------|--|
| | | V _{CC} (V) | | | | | Units | Conditions |
| | | | Тур | 1 8 60 | Guaranteed L | imits | | PANIUMAG |
| loz | Maximum TRI-STATE® Leakage Current | 5.5 | 19/1908 | ±0.5 | ±10.0 | ±5.0 | μΑ | V_{I} (OE) = V_{IL} , V_{IH} $V_{I} = V_{CC}$, GND $V_{O} = V_{CC}$, GND |
| I _{OLD} | †Minimum Dynamic Output Current | 5.5 | hot alor | Hoo sis | 50 | 75 SO SO | mA | V _{OLD} = 1.65V Max |
| I _{OHD} | | 5.5 | egsxne | a mile lir | -50 | -75 | mA | V _{OHD} = 3.85V Min |
| Icc | Maximum Quiescent Supply Current | 5.5 | | 8.0 | 160.0 | 80.0 | μА | $V_{IN} = V_{CC}$ or GND |

^{*}All outputs loaded; thresholds on input associated with output under test.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC} . I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

AC Electrical Characteristics

| | 28 CE8A | 5 - AE30 | | 74AC | 15 | 54 | AC | 74 | AC | | |
|------------------|-------------------------------------|-------------------|------------|-----------------------|-------------|------------|-------------------------|------------|------------------------|--------|-------------|
| Symbol | Parameter | V _{CC} * | | A = +25° CL = 50 p | | to + | -55°C 125°C 50 pF | to + | -40°C 85°C 50 pF | Units | Fig. No. |
| | - 12 mod 2 l | 8 A | Min | Тур | Max | Min | Max | Min | Max | B0 10- | |
| t _{PLH} | Propagation Delay Data to Output | 3.3 5.0 | 2.0 | 5.5 4.0 | 8.0 6.0 | 1.0 | 10.0 | 1.5 1.0 | 9.0 6.5 | ns | 2-5 |
| t _{PHL} | Propagation Delay Data to Output | 3.3 5.0 | 2.0 1.5 | 5.5 4.0 | 8.0 6.0 | 1.0 1.0 | 9.5 7.0 | 1.5 1.0 | 8.5 6.5 | ns | 2-5 |
| t _{PZH} | Output Enable Time | 3.3 5.0 | 3.0 | 8.0 6.0 | 11.5 8.5 | 1.0 1.0 | 13.5 | 3.0 1.5 | 12.5 9.5 | ns | 2-7 |
| t _{PZL} | Output Enable Time | 3.3 5.0 | 2.5 | 7.0 5.5 | 10.0 7.5 | 1.0 1.0 | 12.5 9.0 | 2.5 1.0 | 11.5 8.5 | ns | 2-8 |
| t _{PHZ} | Output Disable Time | 3.3 5.0 | 3.5 2.0 | 9.0 7.0 | 12.5 9.5 | 1.0 1.0 | 15.0 12.0 | 2.5 1.0 | 14.0 10.5 | ns | 2-7 |
| t _{PLZ} | Output Disable Time | 3.3 5.0 | 2.5 2.0 | 6.5 5.5 | 9.5 7.5 | 1.0 1.0 | 11.0 9.0 | 2.0 1.0 | 10.5 8.5 | ns | 2-8 |

*Voltage Range 3.3 is 3.3V ± 0.3 V Voltage Range 5.0 is 5.0V ± 0.5 V

| Symbol | Parameter | AC/ACT | Units | Conditions |
|-----------------|-------------------------------|--------|-------|---------------------|
| Symbol | raiameter (1931) | Тур | Onito | Olevinalium |
| C _{IN} | Input Capacitance | 4.5 | pF O | $V_{\rm CC} = 5.0V$ |
| C _{PD} | Power Dissipation Capacitance | 30.0 | pF | $V_{CC} = 5.0V$ |

[†]Maximum test duration 2.0 ms, one output loaded at a time.





54ACT/74ACT543 Octal Registered Transceiver

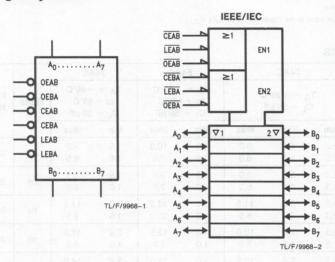
General Description

The 'ACT543 octal transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable and Output Enable inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow.

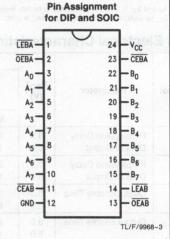
Features

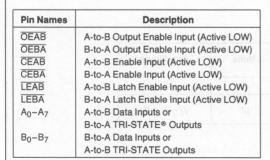
- 8-bit octal transceiver
- Back-to-back registers for storage
- Separate controls for data flow in each direction
- 300 mil slim package
- 'ACT543 has TTL-compatible inputs

Logic Symbols



Connection Diagrams





FOR LCC A₆ A₅ A₄ NC A₃ A₂ A₁ 1 10 9 8 7 5 5 A₇ 12 CEAB 13 GND 14 NC 15 OEAB 16 LEBA T NC 22 CEBA B₇ B T L/F/9968-4

Pin Assignment

ADVANCE INFORMATION



54ACT/74ACT544 Octal Registered Transceiver TATE AND AND ADD

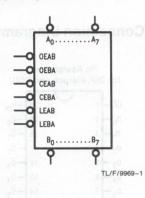
General Description

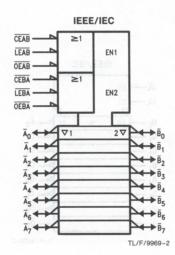
The 'ACT544 octal transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable and Output Enable inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow. The 'ACT544 inverts data in both directions.

Features

- 8-bit octal transceiver
- Back-to-back registers for storage
- Separate controls for data flow in each direction
- 300 mil slim package
- 'ACT544 has TTL-compatible inputs

Logic Symbols

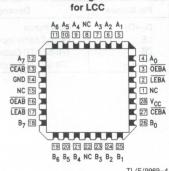




Connection Diagrams



| Pin Names | Description | | | | | | |
|-----------------------------------|---|--|--|--|--|--|--|
| OEAB | A-to-B Output Enable Input (Active LOW) | | | | | | |
| OEBA | B-to-A Output Enable Input (Active LOW) | | | | | | |
| CEAB | A-to-B Enable Input (Active LOW) | | | | | | |
| CEBA | B-to-A Enable Input (Active LOW) | | | | | | |
| LEAB | A-to-B Latch Enable Input (Active LOW) | | | | | | |
| LEBA | B-to-A Latch Enable Input (Active LOW) | | | | | | |
| $\overline{A}_0 - \overline{A}_7$ | A-to-B Data Inputs or B-to-A TRI-STATE® Outputs | | | | | | |
| $\overline{B}_0 - \overline{B}_7$ | B-to-A Data Inputs or A-to-B TRI-STATE Outputs | | | | | | |



Pin Assignment

TL/F/9969-4



54ACT/74ACT563 Octal Latch with TRI-STATE® Outputs

General Description

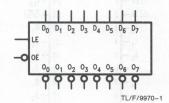
The 'ACT563 is a high-speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable (OE) inputs.

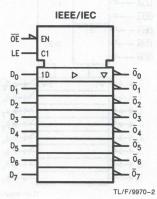
Features

- Inputs and outputs on opposite sides of package allow easy interface with microprocessors
- Useful as input or output port for microprocessors
- Functionally identical to 'ACT573 but with inverted outputs
- Outputs source/sink 24 mA
- 'ACT563 has TTL-compatible inputs

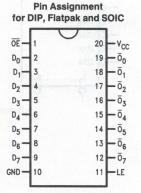
Ordering Code: See Section 5

Logic Symbols



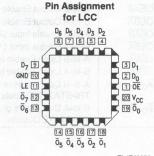


Connection Diagrams



TL/F/9970-3

| Pin Names | Description | | | | | |
|-----------------------------------|-------------------------------|--|--|--|--|--|
| D ₀ -D ₇ | Data Inputs | | | | | |
| LE | Latch Enable Input | | | | | |
| ŌĒ | TRI-STATE Output Enable Input | | | | | |
| $\overline{O}_0 - \overline{O}_7$ | TRI-STATE Latch Outputs | | | | | |



TL/F/9970-4

Functional Description

The 'ACT563 contains eight D-type latches with TRI-STATE complementary outputs. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE buffers are controlled by the Output Enable $(\overline{\rm OE})$ input. When $\overline{\rm OE}$ is LOW, the buffers are in the bi-state mode. When $\overline{\rm OE}$ is HIGH the buffers are in the high impedance mode but that does not interfere with entering new data into the latches.

Function Table

| Inputs | | Internal | Outputs | Function | |
|--------|----|----------|---------|-------------|-----------------|
| OE | LE | D | Q | 0 | uel del O confi |
| Н | X | X | X | Z | High-Z |
| Н | Н | L | Н | (m) Z 1100 | High-Z |
| H | Н | Н | L | Z | High-Z |
| H | L | X | NC | Z | Latched |
| _C | H | L | Н | H (W) 8 | Transparent |
| L | Н | Н | L (%) | o Ougani (t | Transparent |
| LOS | L | X | NC | NC | Latched |

H = HIGH Voltage Level

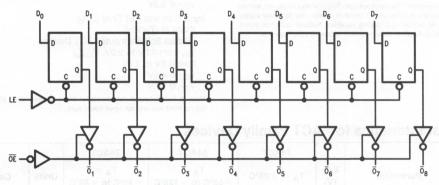
L = LOW Voltage Level

X = Immaterial

Z = High Impedance

NC = No Change

Logic Diagram



TL/F/9970-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Supply Voltage (V _{CC}) | -0.5V to $+7.0$ V |
|---|---------------------------------|
| DC Input Diode Current (I _{IK}) | |
| $V_{I} = -0.5V$ | -20 mA |
| $V_I = V_{CC} + 0.5V$ | + 20 mA |
| DC Input Voltage (V _I) | -0.5 V to $V_{CC} + 0.5$ V |
| DC Output Diode Current (IOK) | |
| $V_0 = -0.5V$ | -20 mA |
| $V_O = V_{CC} + 0.5V$ | + 20 mA |
| DC Output Voltage (V _O) | -0.5 V to to $V_{CC} + 0.5$ V |
| DC Output Source | |
| or Sink Current (IO) | ± 50 mA |
| DC V _{CC} or Ground Current | |
| per Output Pin (I _{CC} or I _{GND}) | ± 50 mA |
| Storage Temperature (TSTG) | -65°C to +150°C |
| | |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

| Supply Voltage (V _{CC}) | |
|---|------------------------------------|
| 'AC | |
| 'ACT someth from G at more | 1 5\/ to 5 5\/ |
| Input Voltage (V _I) | |
| Output Voltage (VO) | 0V to V _{CC} |
| Operating Temperature (T _A) | |
| 74AC/ACT | -40° C to $+85^{\circ}$ C |
| 54AC/ACT | -55°C to +125°C |
| Junction Temperature (T _{.I}) | |
| CDIP | 175°C |
| PDIP | 140°C |
| Input Rise and Fall Time (t _r , t _f) | |
| (Note 2) (Typical) | |
| (Except Schmitt Inputs) 'AC Devices | |
| V _{IN} from 30% to 70% of V _{CC} | |

V_{CC} @ 5.5V Input Rise and Fall Time (t_r, t_f)

(Note 2) (Typical) (Except Schmitt Inputs) 'ACT Devices V_{IN} from 0.8V to 2.0V, V_{meas}

from 0.8V to 2.0V V_{CC} @ 4.5V V_{CC} @ 5.5V

V_{CC} @ 3.0V

V_{CC} @ 4.5V

10 ns/V 8 ns/V

150 ns/V 40 ns/V

25 ns/V

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'ACT Family Devices

| | 9 9 | | 74/ | ACT | 54ACT | 74ACT | -3 | - Tr |
|-----------------|--------------------------------------|------------------------|----------------|--------------|----------------------------------|--------------------------------------|--------------|--|
| Symbol | Parameter | V _{CC} (V) | | | T _A = -55°C to +125°C | T _A = 0 -40°C to +85°C | Units | Conditions |
| | i to estimate precisación oclays. | Coe yes | Тур | | Guaranteed Li | mits | o eint tert. | ston easelfs |
| V _{IH} | Minimum High Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 2.0 2.0 | 2.0 2.0 | 2.0 2.0 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ |
| V _{IL} | Maximum Low Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 0.8 | 0.8 0.8 | 0.8 0.8 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ |
| V _{OH} | Minimum High Level Output Voltage | 4.5 5.5 | 4.49 5.49 | 4.4 5.4 | 4.4 5.4 | 4.4 5.4 | ٧ | $I_{OUT} = -50 \mu$ |
| | | 4.5 5.5 | | 3.86 4.86 | 3.70 4.70 | 3.76 4.76 | v | $V_{IN} = V_{IL} \text{ or } V_{IOH}$ $V_{IOH} = V_{IL} \text{ or } V_{IL} $ |
| V _{OL} | Maximum Low Level Output Voltage | 4.5 5.5 | 0.001 0.001 | 0.1 0.1 | 0.1 0.1 | 0.1 0.1 | V | $I_{OUT} = 50 \mu A$ |
| | | 4.5 5.5 | | 0.36 0.36 | 0.50 0.50 | 0.44 0.44 | V | $V_{IN} = V_{IL} \text{ or } V_{IN}$ $I_{OL} \qquad 24 \text{ r}$ 24 r |
| I _{IN} | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | ±1.0 | μА | $V_{I} = V_{CC}$, GNE |
| l _{OZ} | Maximum TRI-STATE® Current | 5.5 | | ±0.5 | ±10.0 | ±5.0 | μΑ | $V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}, GN$ |
| ГССТ | Maximum I _{CC} /Input | 5.5 | 0.6 | | 1.6 | 1.5 | mA | $V_I = V_{CC} - 2.$ |

DC Characteristics for 'ACT Family Devices (Continued)

| Symbol | an | oitions | 74A | CT | 54ACT | 74ACT | | Symbol | |
|------------------|-------------------------------------|------------------------|------------------------|-------|-----------------------------------|---------------------------------|------------|------------------------------|--|
| | Parameter | V _{CC} (V) | T _A = +25°C | | T _A = -55°C to + 125°C | T _A = -40°C to +85°C | Units | Conditions | |
| | VC | 0 = 5. | Тур | PF PF | Guaranteed Li | mits | MPH HeO | 093 | |
| IOLD | †Minimum Dynamic | 5.5 | | | 50 | 75 | mA | V _{OLD} = 1.65V Max | |
| I _{OHD} | Output Current | 5.5 | | | -50 | -75 | mA | V _{OHD} = 3.85V Min | |
| Icc | Maximum Quiescent Supply Current | 5.5 | | 8.0 | 160.0 | 80.0 | μА | $V_{IN} = V_{CC}$ or GND | |

^{*}All outputs loaded; thresholds on input associated with output under test.

AC Electrical Characteristics

| | | | | 74ACT | | 54 | ACT | 74/ | ACT | | |
|------------------|---|--------------------------|-----|--|------|---|------|--|------|-------|-------------|
| Symbol Parameter | | V _{CC} * (V) | | T _A = +25°C C _L = 50 pF | | $T_A = -55^{\circ}C$ to $+125^{\circ}C$ $C_L = 50 pF$ | | $T_A = -40^{\circ}C$ $to +85^{\circ}C$ $C_L = 50 pF$ | | Units | Fig. No. |
| | | | Min | Тур | Max | Min | Max | Min | Max | | |
| t _{PLH} | Propagation Delay D_n to \overline{O}_n | 5.0 | 3.0 | 7.0 | 11.5 | 1.0 | 14.5 | 2.5 | 12.5 | ns | 2-5 |
| t _{PHL} | Propagation Delay D_n to \overline{O}_n | 5.0 | 3.0 | 6.0 | 10.0 | 1.0 | 12.0 | 2.5 | 11.0 | ns | 2-5 |
| t _{PLH} | Propagation Delay LE to On | 5.0 | 3.0 | 6.5 | 10.5 | 1.0 | 12.5 | 2.5 | 11.5 | ns | 2-6 |
| t _{PHL} | Propagation Delay LE to On | 5.0 | 2.5 | 5.5 | 9.5 | 1.0 | 11.5 | 2.0 | 10.5 | ns | 2-6 |
| t _{PZH} | Output Enable Time | 5.0 | 2.5 | 5.5 | 9.0 | 1.0 | 11.5 | 2.0 | 10.0 | ns | 2-7 |
| t _{PZL} | Output Enable Time | 5.0 | 2.0 | 5.5 | 8.5 | 1.0 | 11.0 | 2.0 | 9.5 | ns | 2-8 |
| t _{PHZ} | Output Disable Time | 5.0 | 3.5 | 6.5 | 10.5 | 1.0 | 12.0 | 2.5 | 11.5 | ns | 2-7 |
| t _{PLZ} | Output Disable Time | 5.0 | 2.0 | 4.5 | 8.0 | 1.0 | 9.5 | 1.0 | 8.5 | ns | 2-8 |

^{*}Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

| | | | 744 | CT | 54ACT | 74ACT | | |
|----------------|---|-------------------|------|-----|---|--|-------|-------------|
| Symbol | Parameter | V _{CC} * | | | $T_A = -55^{\circ}C$ to $+125^{\circ}C$ $C_L = 50 pF$ | $T_A = -40^{\circ}C$ $to +85^{\circ}C$ $C_L = 50 pF$ | Units | Fig. No. |
| | | | Тур | | Guaranteed Min | imum | | |
| t _s | Setup Time, HIGH or LOW D _n to LE | 5.0 | 1.5 | 4.0 | 4.5 | 4.5 | ns | 2-9 |
| t _h | Hold Time, HIGH or LOW D _n to LE | 5.0 | -2.0 | 0 | 1.5 | 0 | ns | 2-9 |
| t _w | LE Pulse Width, HIGH | 5.0 | 2.0 | 3.0 | 5.0 | 3.0 | ns | 2-6 |

^{*}Voltage Range 5.0 is 5.0V \pm 0.5V

[†]Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

| Symbol | Parameter | AC/ACT | Units | Conditions | |
|-----------------|----------------------------------|--------|-------|-----------------|--|
| Oyiiiboi | raiameter | Тур | Oille | Conditions | |
| CIN | Input Capacitance | 4.5 | pF | $V_{CC} = 5.0V$ | |
| C _{PD} | Power Dissipation Capacitance | 50.0 | pF | $V_{CC} = 5.0V$ | |



54ACT/74ACT564 Octal D Flip-Flop with TRI-STATE® Outputs

General Description

The 'ACT564 is a high-speed, low power octal flip-flop with a buffered common Clock (CP) and a buffered common Output Enable (\overline{OE}). The information presented to the D inputs is stored in the flip-flops on the LOW-to-HIGH Clock (CP) transition.

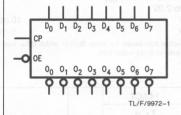
The 'ACT564 device is functionally identical to the 'ACT574, but with inverted outputs.

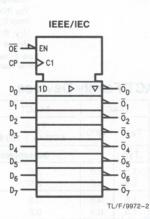
Features

- Inputs and outputs on opposite sides of package allow easy interface with microprocessors
- Useful as input or output port for microprocessors
- Functionally identical to 'ACT574 but with inverted outputs
- TRI-STATE outputs for bus-oriented applications
- Outputs source/sink 24 mA
- 'ACT564 has TTL-compatible inputs

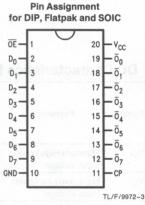
Ordering Code: See Section 5

Logic Symbols

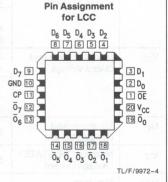




Connection Diagrams



| Pin Names | Description | |
|-----------------------------------|---------------------|------------|
| D ₀ -D ₇ | Data Inputs | |
| CP | Clock Pulse Input | |
| ŌĒ | TRI-STATE Output En | able Input |
| $\overline{O}_0 - \overline{O}_7$ | TRI-STATE Outputs | |



Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Supply Voltage (V _{CC}) | -0.5V to $+7.0V$ |
|---|-----------------------------------|
| DC Input Diode Current (I _{IK}) | |
| $V_{I} = -0.5V$ | -20 mA |
| $V_I = V_{CC} + 0.5V$ | +20 mA |
| DC Input Voltage (V _I) | -0.5 V to $V_{CC} + 0.5$ V |
| DC Output Diode Current (IOK) | |
| $V_0 = -0.5V$ | no efuctio bale = -20 mA |
| $V_O = V_{CC} + 0.5V$ | + 20 mA |
| DC Output Voltage (V _O) | -0.5 V to to V_{CC} + 0.5 V |
| DC Output Source | |
| or Sink Current (IO) | ±50 mA |

Storage Temperature (TSTG) -65°C to +150°C Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recom-

mend operation of FACTTM circuits outside databook specifications.

DC V_{CC} or Ground Current per Output Pin (ICC or IGND)

Recommended Operating Conditions

Supply Voltage (V_{CC})

from 0.8V to 2.0V V_{CC} @ 4.5V

| 'AC | 2.0V to 6.0V |
|---|-----------------------|
| 'ACT | 4.5V to 5.5V |
| Input Voltage (V _I) | 0V to V _{CC} |
| Output Voltage (V _O) | 0V to V _{CC} |
| Operating Temperature (T _A) | |
| 74AC/ACT | -40°C to +85°C |
| 54AC/ACT | -55°C to +125°C |
| | |
| CDID | 175°C |
| PDIP resetu nodamo m s (20) | |
| Input Rise and Fall Time (t _r , t _f) | |
| (Note 2) (Typical) | |
| (Except Schmitt Inputs) 'AC Devices | |
| VIN from 30% to 70% of VCC | |
| V _{CC} @ 3.0V | 150 ns/V |
| V _{CC} @ 4.5V | 40 ns/V |
| V _{CC} @ 5.5V | 25 ns/V |
| Input Rise and Fall Time (t _r , t _f) | |
| (Note 2) (Typical) | |
| (Except Schmitt Inputs) 'ACT Device | S |
| V _{IN} from 0.8V to 2.0V, V _{meas} | |
| | |

V_{CC} @ 5.5V Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

10 ns/V

8 ns/V

DC Characteristics for 'ACT Family Devices

| 0.344 | [F] b (i) | | 74A | CT | 54ACT | 74ACT | 1 1 | |
|----------------------------|--|---------------------|------------------|--------------------|----------------------------------|---------------------------------|-------|---|
| Symbol | Parameter | V _{CC} (V) | T _A = | + 25°C | T _A = -55°C to +125°C | T _A = -40°C to +85°C | Units | Conditions |
| | \$1 \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ | | Тур | - Name of the last | Guaranteed L | imits | | |
| VIH | Minimum High Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 2.0 2.0 | 2.0 2.0 | 2.0 2.0 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ |
| V _{IL} | Maximum Low Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 0.8 0.8 | 0.8 0.8 | 0.8 0.8 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ |
| V _{OH} | Minimum High Level Output Voltage | 4.5 5.5 | 4.49 5.49 | 4.4 5.4 | 4.4 5.4 | 4.4 5.4 | ٧ | $I_{OUT} = -50 \mu\text{A}$ |
| | 6 16 18 10 10 10 10 10 10 10 10 10 10 10 10 10 | 4.5 5.5 | | 3.86 4.86 | 3.70 4.70 | 3.76 4.76 | V | $V_{IN} = V_{IL} \text{ or } V_{IH}$ -24 mA -24 mA |
| V _{OL} | Maximum Low Level Output Voltage | 4.5 5.5 | 0.001 0.001 | 0.1 | 0.1 d oldered 0.1 | 0.1 | V | I _{OUT} = 50 μA |
| 20 (E) 30 (E) 30 (E) | | 4.5 5.5 | | 0.36 0.36 | 0.50 0.50 | 0.44 0.44 | v | $\begin{tabular}{ll} *V_{IN} = V_{IL} \mbox{ or } V_{IH} \\ I_{OL} & 24 \mbox{ mA} \\ 24 \mbox{ mA} \\ \end{tabular}$ |
| IIN | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | ±1.0 | μΑ | $V_I = V_{CC}$, GND |
| loz | Maximum TRI-STATE® Leakage Current | 5.5 | | ±0.5 | ± 10.0 | ±5.0 | μΑ | $V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}, GND$ |
| Ісст | Maximum I _{CC} /Input | 5.5 | 0.6 | | 1.6 | 1.5 | mA | $V_{\rm I} = V_{\rm CC} - 2.1V$ |
| IOLD | †Minimum Dynamic | 5.5 | | | 50 | 75 | mA | V _{OLD} = 1.65V Max |
| I _{OHD} | Output Current | 5.5 | | | -50 | -75 | mA | V _{OHD} = 3.85V Min |

DC Characteristics for 'ACT Family Devices (Continued)

| | | | 74 | ACT | 54ACT | 74ACT | | |
|--------|-------------------------------------|--|-----|--------|---|-------|---------|--|
| Symbol | Parameter | V _{CC} (V) T _A = +25°C | | + 25°C | $ \begin{array}{c c} T_{A} = & T_{A} = \\ -55^{\circ}\text{C to} + 125^{\circ}\text{C} & -40^{\circ}\text{C to} + 85^{\circ}\text{C} \\ \end{array} $ | | | Conditions |
| | | | Тур | | Guaranteed Lin | nits | es no s | I SPORT |
| lcc | Maximum Quiescent Supply Current | 5.5 | | 8.0 | 160.0 | 80.0 | μА | V _{IN} = V _{CC} or GND |

^{*}All outputs loaded; thresholds on input associated with output under test.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

| Symbol | | Lors rock | puo o sa someos s | 74ACT | | 54/ | ACT | 7 | 4ACT | MIC OF E | SIUUN | |
|------------------|---|-----------|-----------------------|-------|----------------------------------|-----|------|-------------------------|-------|-----------------------------|-------|--------------------|
| | Symbol | Parameter | V _{CC} * (V) | | A = +25 C _L = 50 p | | to + | −55°C 125°C 50 pF | to | = -40°C +85°C = 50 pF | Units | Fig. |
| | | | | | Min | Тур | Max | Min | Max | Min | Max | and a least of the |
| f _{max} | Maximum Clock Frequency | 5.0 | 85 | 90 | | 65 | | 75 | alodm | MHz | 2-3 | |
| f _{PLH} | Propagation Delay, CP to \overline{O}_n | 5.0 | 2.0 | 6.5 | 10.5 | 1.0 | 12.5 | 1.5 | 11.5 | ns | 2-6 | |
| f _{PHL} | Propagation Delay, CP to \overline{O}_n | 5.0 | 1.5 | 6.0 | 9.5 | 1.0 | 11.5 | 1.5 | 10.5 | ns | 2-6 | |
| t _{PZH} | Output Enable Time | 5.0 | 1.5 | 5.5 | 9.0 | 1.0 | 10.5 | 1.5 | 9.5 | ns | 2-7 | |
| t _{PZL} | Output Enable Time | 5.0 | 1.5 | 5.5 | 8.5 | 1.0 | 10.5 | 1.0 | 9.5 | ns | 2-8 | |
| t _{PHZ} | Output Disable Time | 5.0 | 1.5 | 7.0 | 10.5 | 1.0 | 12.5 | 1.5 | 11.5 | ns | 2-7 | |
| t _{PLZ} | Output Disable Time | 5.0 | 1.5 | 5.0 | 8.0 | 1.0 | 9.5 | 1.0 | 8.5 | ns | 2-8 | |

^{*}Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

| Symbol | Parameter | | 74A | CT | 54ACT | 74ACT | | |
|----------------|---|-------------------|------|-----|---|--|-------|-------------|
| | | V _{CC} * | | | $T_A = -55^{\circ}C$ to $+125^{\circ}C$ $C_L = 50 pF$ | $T_A = -40^{\circ}C$ $to +85^{\circ}C$ $C_L = 50 pF$ | Units | Fig. No. |
| | | | Тур | | Guaranteed Min | imum | esmov | ale |
| t _s | Setup Time, HIGH or LOW D _n to CP | 5.0 | 1.0 | 2.5 | 3.5 | atuori 3.0°C | ns | 2-9 |
| t _h | Hold Time, HIGH or LOW D _n to CP | 5.0 | -0.5 | 1.0 | dugni elden E Argiui el 2.5 O nota | TATALO.T | ns - | 2-9 |
| t _w | LE Pulse Width, HIGH or LOW | 5.0 | 2.5 | 3.0 | 5.0 | 3.5 | ns | 2-6 |

^{*}Voltage Range 5.0 is 5.0V \pm 0.5V

| Symbol | Parameter | AC/ACT | Units | Conditions |
|-----------------|-------------------------------|--------|--------|-----------------|
| Symbol | Falameter | Тур | Oilito | Conditions |
| C _{IN} | Input Capacitance | 4.5 | pF | $V_{CC} = 5.0V$ |
| C _{PD} | Power Dissipation Capacitance | 50.0 | pF | $V_{CC} = 5.0V$ |

[†]Maximum test duration 2.0 ms, one output loaded at a time.



54ACT/74ACT573 Octal Latch with TRI-STATE® Outputs

General Description

The 'ACT573 is a high-speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable ($\overline{\text{OE}}$) inputs.

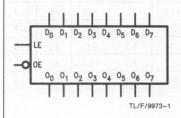
The 'ACT573 is functionally identical to the 'ACT373 but has inputs and outputs on opposite sides.

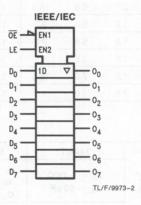
Features

- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors
- Functionally identical to 'ACT373
- TRI-STATE outputs for bus interfacing
- Outputs source/sink 24 mA
- 'ACT573 has TTL-compatible inputs

Ordering Code: See Section 5

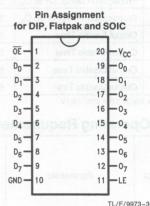
Logic Symbols





| Pin Names | Description |
|--------------------------------|-------------------------------|
| D ₀ -D ₇ | Data Inputs |
| LE | Latch Enable Input |
| ŌĒ | TRI-STATE Output Enable Input |
| 00-07 | TRI-STATE Latch Outputs |

Connection Diagrams



Pin Assignment for LCC D6 D5 D4 D3 D2 87654 D₇ 9 GND 10 3 D1 2 D₀ LE [11] 1 OE 07 12 20 V_{CC} 06 13 19 00 14 15 16 17 18 05 04 03 02 01

TL/F/9973-4

Functional Description

The 'ACT573 contains eight D-type latches with TRI-STATE output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE buffers are controlled by the Output Enable $(\overline{\text{OE}})$ input. When $\overline{\text{OE}}$ is LOW, the buffers are enabled. When $\overline{\text{OE}}$ is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

Truth Table

| howiper sa | Outputs | | |
|----------------|---------|---------------|--------------------------------|
| ŌĒ | equile | tellayD tol a | notucini On \abiii |
| 1.5V to 1.7.0V | Н | Н | OA) ebali ^H A Aldde |
| L | Н | (MF) ques | O Input Pieds Cu |
| L | L | X | 00 |
| H | X | X | Z |

H = HIGH Voltage

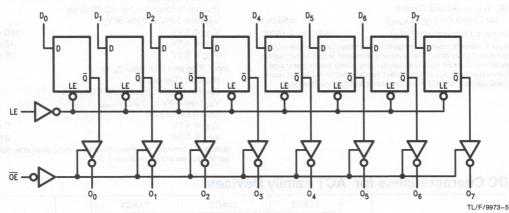
L = LOW Voltage

Z = High Impedance

X = Immaterial

O₀ = Previous O₀ before HIGH-to-LOW transition of Latch Enable

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required. please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| +7.0V |
|---------|
| |
| |
| -20 mA |
| - 20 mA |
| + 0.5V |
| |
| -20 mA |
| +20 mA |
| + 0.5V |
| |
| ± 50 mA |
| |
| ± 50 mA |
| + 150°C |
| |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

| 00.1.0.1.0 | |
|--|-----------------------|
| Supply Voltage (V _{CC}) | |
| 'AC | 2.0V to 6.0V |
| 'ACT | 4 by to b by |
| Input Voltage (V _I) | 0V to V _{CC} |
| Output Voltage (V _O) | 0V to V _{CC} |
| Operating Temperature (T _A) | |
| 74AC/ACT | -40°C to +85°C |
| 54AC/ACT | -55°C to +125°C |
| Junction Temperature (T _{.I}) | |
| CDIP | 175°C |
| PDIP | 140°C |
| Input Rise and Fall Time (t _r , t _f) (Note 2) (Typical) | |
| (Except Schmitt Inputs) 'AC Devices | S |
| V _{IN} from 30% to 70% of V _{CC} | .=0 0/ |
| V _{CC} @ 3.0V | 150 ns/V |
| V _{CC} @ 4.5V | 40 ns/V |
| V _{CC} @ 5.5V | 25 ns/V |
| Input Rise and Fall Time (t _r , t _f) (Note 2) (Typical) | |
| (Except Schmitt Inputs) 'ACT Devic | es |
| V _{IN} from 0.8V to 2.0V, V _{meas} from 0.8V to 2.0V | |

VCC @ 5.5V Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

V_{CC} @ 4.5V

10 ns/V

8 ns/V

DC Characteristics for 'ACT Family Devices

| | | | 74A | CT | 54ACT | 74ACT | | | |
|-----------------|--------------------------------------|---------------------|----------------|--------------|---|--------------|-------|--|--|
| Symbol | Parameter | V _{CC} (V) | | | T _A = T _A = -55°C to + 125°C -40°C to +85° | | Units | Conditions | |
| | | | Тур | | Guaranteed Li | mits | | | |
| V _{IH} | Minimum High Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 2.0 | 2.0 2.0 | 2.0 2.0 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{IL} | Maximum Low Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 0.8 0.8 | 0.8 0.8 | 0.8 0.8 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{OH} | Minimum High Level Output Voltage | 4.5 5.5 | 4.49 5.49 | 4.4 5.4 | 4.4 5.4 | 4.4 5.4 | ٧ | $I_{OUT} = -50 \mu\text{A}$ | |
| | | 4.5 5.5 | | 3.86 4.86 | 3.70 4.70 | 3.76 4.76 | ٧ | $V_{IN} = V_{IL} \text{ or } V_{I}$ -24 m -24 m | |
| V _{OL} | Maximum Low Level Output Voltage | 4.5 5.5 | 0.001 0.001 | 0.1 0.1 | 0.1 0.1 | 0.1 0.1 | ٧ | $I_{OUT} = 50 \mu A$ | |
| | | 4.5 5.5 | | 0.36 0.36 | 0.50 0.50 | 0.44 0.44 | V | $V_{IN} = V_{IL} \text{ or } V_{IL}$ $V_{IOL} = V_{IL} \text{ or } V_{IL}$ $V_{IOL} = V_{IL} \text{ or } V_{IL}$ $V_{IOL} = V_{IL} \text{ or } V_{IL}$ | |
| I _{IN} | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | ±1.0 | μА | $V_I = V_{CC}$, GND | |
| loz | Maximum TRI-STATE Current | 5.5 | | ±0.5 | ±10.0 | ±5.0 | μΑ | $V_{I} = V_{IL}, V_{IH}$ $V_{O} = V_{CC}, GNE$ | |

DC Characteristics for 'ACT Family Devices (Continued) The Property of the Continued of the

| Symbol | Parameter | | 74ACT | | 54ACT | 74ACT | Units | |
|--------|-------------------------------------|------------------------|---------------------------|--|---------------|---------------------------------|-------|------------------------------|
| | | V _{CC} (V) | T _A = + | + 25°C T _A = -55°C to + 125°C | | T _A = -40°C to +85°C | | Conditions |
| | Ng 08 = _20 | | Тур | | Guaranteed Li | mits | | |
| ГССТ | Maximum I _{CC} /Input | 5.5 | 0.6 | 323 | 1.6 | 1.5000 H | mA | $V_{I} = V_{CC} - 2.1V$ |
| IOLD | †Minimum Dynamic | 5.5 | | | 50 | 75 | mA | V _{OLD} = 1.65V Max |
| IOHD | Output Current | 5.5 | 0.1 | | -50 | -75 | mA | V _{OHD} = 3.85V Min |
| Icc | Maximum Quiescent Supply Current | 5.5 | 8.0 | 8.0 | 160.0 | 80.0 HOIH | μА | $V_{IN} = V_{CC}$ or GND |

^{*}All outputs loaded; thresholds on input associated with output under test.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

| | 1/0 | - 44 | | 74ACT | | 54 | ACT | 74/ | ACT | 040 | |
|------------------|---|--------------------------|-----|-------|--|-----|--|-----|------------------------|-------|-------------|
| Symbol | Parameter | V _{CC} * (V) | | | C _L = +25°C C _L = 50 pF | | T _A = -55°C to + 125°C C _L = 50 pF | | -40°C 85°C 50 pF | Units | Fig. No. |
| | | | Min | Тур | Max | Min | Max | Min | Max | | |
| t _{PLH} | Propagation Delay D _m to O _n | 5.0 | 2.5 | 6.0 | 10.5 | 1.0 | 13.5 | 2.0 | 12.0 | ns | 2-5 |
| t _{PHL} | Propagation Delay D _n to O _n | 5.0 | 2.5 | 6.0 | 10.5 | 1.0 | 13.5 | 2.0 | 12.0 | ns | 2-5 |
| t _{PLH} | Propagation Delay LE to O _n | 5.0 | 3.0 | 6.0 | 10.5 | 1.0 | 13.0 | 2.5 | 12.0 | ns | 2-6 |
| t _{PHL} | Propagation Delay LE to O _n | 5.0 | 2.5 | 5.5 | 9.5 | 1.0 | 12.0 | 2.0 | 10.5 | ns | 2-6 |
| t _{PZH} | Output Enable Time | 5.0 | 2.0 | 5.5 | 10.0 | 1.0 | 11.5 | 1.5 | 11.0 | ns | 2-7 |
| t _{PZL} | Output Enable Time | 5.0 | 1.5 | 5.5 | 9.5 | 1.0 | 11.0 | 1.5 | 10.5 | ns | 2-8 |
| t _{PHZ} | Output Disable Time | 5.0 | 2.5 | 6.5 | 11.0 | 1.0 | 13.5 | 1.5 | 12.5 | ns | 2-7 |
| t _{PLZ} | Output Disable Time | 5.0 | 1.5 | 5.0 | 8.5 | 1.0 | 10.5 | 1.0 | 9.5 | ns | 2-8 |

^{*}Voltage Range 5.0 is 5.0V $\pm 0.5 \text{V}$

[†]Maximum test duration 2.0 ms, one output loaded at a time.

AC Operating Requirements

| Symbol | Parameter S | | 74A | CT | 54ACT | 74ACT | | |
|----------------|---|---------------------------------------|-------------------------|-----|--|--|-------------------|-------------|
| | | V _{CC} * | $C_{L} = 50 \text{ pF}$ | | T _A = -55°C to + 125°C C _L = 50 pF | T _A = -40°C to +85°C C _L = 50 pF | Units | Fig. No. |
| | | · · · · · · · · · · · · · · · · · · · | Тур | | Guaranteed Min | imum | - Continue to the | |
| ts | Setup Time, HIGH or LOW D _n to LE | 5.0 | 1.5 | 3.0 | 4.5 | 3.5 | ns | 2-9 |
| t _h | Hold Time, HIGH or LOW D _n to LE | 5.0 | -1.5 | 0 | 1.0 | Ouronic | ns | 2-9 |
| t _w | LE Pulse Width, HIGH | 5.0 | 2.0 | 3.5 | 5.0 | 4.0 | ns | 2-6 |

^{*}Voltage Range 5.0 is 5.0V ±0.5V

| Symbol | Parameter | AC/ACT | Units | Conditions | CONTRACTOR (COLOR) |
|-----------------|----------------------------------|--------|-------|------------------------|--------------------|
| Oyinboi | rarameter | Тур | Omto | Conditions | Desired and Co. |
| C _{IN} | Input Capacitance | 5.0 | pF | $V_{CC} = 5.0V$ | |
| C _{PD} | Power Dissipation Capacitance | 25.0 | pF | V _{CC} = 5.0V | |



54AC/74AC574 • 54ACT/74ACT574 Octal D-Type Flip-Flop with TRI-STATE® Outputs

General Description

The 'AC/'ACT574 is a high-speed, low power octal flip-flop with a buffered common Clock (CP) and a buffered common Output Enable (OE). The information presented to the D inputs is stored in the flip-flops on the LOW-to-HIGH Clock (CP) transition.

The 'AC/'ACT574 is functionally identical to the 'AC/ 'ACT374 except for the pinouts.

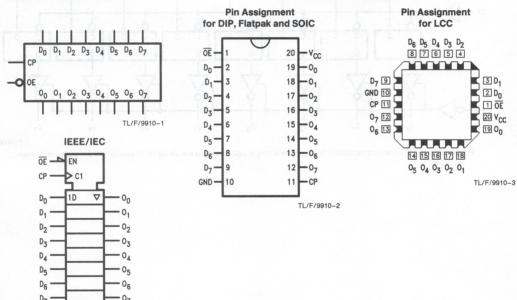
Features

- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors
- Functionally identical to 'AC/'ACT374
- TRI-STATE outputs for bus-oriented applications
- Outputs source/sink 24 mA
- 'ACT574 has TTL-compatible inputs

Ordering Code: See Section 5

Logic Symbols

Connection Diagrams



| Pin Names | Description |
|--------------------------------|-------------------------------|
| D ₀ -D ₇ | Data Inputs |
| CP | Clock Pulse Input |
| ŌĒ | TRI-STATE Output Enable Input |
| 00-07 | TRI-STATE Outputs |

TL/F/9910-4

Functional Description

The 'AC/'ACT574 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable $(\overline{\text{OE}})$ LOW, the contents of the eight flip-flops are available at the outputs. When $\overline{\text{OE}}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{\text{OE}}$ input does not affect the state of the flip-flops.

Function Table

| Inputs | | SaPi, | Internal | Outputs | Function |
|--------|----|-------|----------|---------|-------------------|
| OE | CP | D | Q | ON | |
| Н | Н | L | NC | Z | Hold |
| Н | Н | H | NC | Z | Hold |
| Н | 1 | L | L | Z | Load |
| Н | 5 | Н | Н | Z | Load |
| L | _ | L | L | L | Data Available |
| L | 1 | H | н | Н | Data Available |
| L | Н | L | NC | NC | No Change in Data |
| L | Н | H | NC | NC | No Change in Data |

H = HIGH Voltage Level

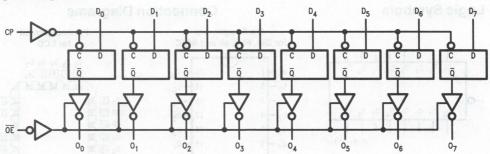
L = LOW Voltage Level

X = ImmaterialZ = High Impedance

= LOW-to-HIGH Transition

NC = No Change

Logic Diagram



TL/F/9910-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Office, Biotifibators for ave | andbinty and spe | cilications. |
|--------------------------------------|--------------------------|---------------------------|
| Supply Voltage (V _{CC}) | 70.55 + ot 5.67 | 0.5V to +7.0V |
| DC Input Diode Current (IIK) | 81 | |
| $V_{I} = -0.5V_{I}$ | | -20 mA |
| $V_I = V_{CC} + 0.5V$ | | + 20 mA |
| DC Input Voltage (V _I) | -0.5V | to $V_{CC} + 0.5V$ |
| DC Output Diode Current (Ic | ok) | |
| $V_O = -0.5V$ | | -20 mA |
| $V_O = V_{CC} + 0.5V$ | | + 20 mA |
| DC Output Voltage (VO) | -0.5V | to V _{CC} + 0.5V |
| DC Output Source or Sink Co | urrent (I _O) | ± 50 mA |
| DC V _{CC} or Ground Current | | |

Storage Temperature (T_{STG}) -65°C to +150°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Per Output Pin (I_{CC} or I_{GND})

Recommended Operating Conditions

| Supply Voltage (V _{CC}) (Unless Otherwise Specified) (AC) | 2.0V to 6.0V |
|---|-----------------------------------|
| (ACT) | 4.5V to 5.5V |
| Input Voltage (V _I) | 0V to V _{CC} |
| Output Voltage (VO) | |
| Operating Temperature (T _A) | spexise! |
| 74AC/ACT 54AC/ACT | -40°C to +85°C -55°C to +125°C |
| Junction Temperature (T _J) | |
| CDIP PDIP | 175°C 140°C |
| Input Rise and Fall Time (t _r , t _f) (Note 2) (Typical) (Except Schmitt Inputs) 'AC Devices V _{IN} from 30% to 70% of V _{CC} | |
| V _{CC} @ 3.0V | 150 ns/V |
| V _{CC} @ 4.5V | |
| V _{CC} @ 5.5V | 25 ns/V |
| Input Rise and Fall Time (t _r , t _f) (Note 2) (Typical) | |
| (Except Schmitt Inputs) 'ACT Devices V _{IN} from 0.8V to 2.0V, V _{meas} from 0.8V to 2.0V | |
| V _{CC} @ 4.5V V _{CC} @ 5.5V | 8 ns/V |
| Note to the state of the state | |

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

| | V | 5.4 | 74 | AC | 54AC | 74AC | | | |
|---------------------|--------------------------------------|---------------------|-------------------------|----------------------|-----------------------------------|---------------------------------|------------------------------------|--|--|
| Symbol | Parameter | V _{CC} (V) | | | T _A = -55°C to + 125°C | T _A = -40°C to +85°C | Units | Conditions | |
| | The Year | 67.4 | Тур | | Guaranteed L | imits | | | |
| V _{IH} 03 | Minimum High Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | ulwojn Vijo | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| VIL AS | Maximum Low Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{OH} | Minimum High Level Output Voltage | 3.0 4.5 5.5 | 2.99 4.49 5.49 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | V V IRLS | $I_{OUT} = -50 \mu\text{A}$ | |
| 06. GND 0 - 8.1V | V = oV | 3.0 4.5 5.5 | | 2.56 3.86 4.86 | 2.4 3.7 4.7 | 2.46 3.76 4.76 | Oureint Oureint V m Dynar | $\begin{tabular}{ll} *V_{IN} &= V_{IL} \mbox{ or } V_{IH} \\ &- 12 \mbox{ mA} \\ I_{OH} &- 24 \mbox{ mA} \\ &- 24 \mbox{ mA} \\ \end{tabular}$ | |
| V _{OL} | Maximum Low Level Output Voltage | 3.0 4.5 5.5 | 0.002 0.001 0.001 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | n C, V esc | Ι _{ΟUT} = 50 μΑ | |
| | | 3.0 4.5 5.5 | | 0.32 0.32 0.32 | 0.4 0.4 0.4 | 0.37 0.37 0.37 | em 0.5 n | $*V_{IN} = V_{IL} \text{ or } V_{IH}$ 12 mA I_{OL} 24 mA 24 mA | |
| I _{IN} | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | ±1.0 | μΑ | $V_{I} = V_{CC}$, GND | |

±50 mA

DC Characteristics for 'AC Family Devices (Continued) The Research Continued (Continue

| | | | 74 | AC | 54AC | 74AC | ge edet | enten south | |
|--------|--------------------------------------|------------------------|-----------------------|--------------|----------------------------------|---------------------------------|---------|--|--|
| Symbol | Parameter (DA) | V _{CC} (V) | T _A = 25°C | | T _A = -55°C to +125°C | T _A = -40°C to +85°C | Units | Conditions | |
| | | | Тур | Karati in se | Guaranteed L | imits | al) men | O about hank OO | |
| loz | Maximum TRI-STATE Leakage Current | 5.5 | 517) egr | ±0.5 | ± 10.0 | ±5.0 | μΑ | $\begin{aligned} & V_{l} \text{ (OE)} = V_{lL}, V_{lH} \\ & V_{l} = V_{CC}, V_{GND} \\ & V_{O} = V_{CC}, \text{GND} \end{aligned}$ | |
| IOLD | †Minimum Dynamic | 5.5 | | DAYOAN | 57 | 86 (50 | mA | V _{OLD} = 1.1V | |
| IOHD | Output Current | 5.5 | mperati | aT noimi | -50 | -75 | mA | $V_{OHD} = 3.85V$ | |
| Icc | Maximum Quiescent Supply Current | 5.5 | | 8.0 | 160 | 08. 0.5V10 | μА | V _{IN} = V _{CC} or GND | |

^{*}All outputs loaded; thresholds on input associated with output under test.

DC Characteristics for 'ACT Family Devices

| | 66 | | 1 A = 25 L | | 54ACT | 74ACT | Units | Conditions | |
|------------------|--------------------------------------|------------------------|----------------|--------------|----------------------------------|---------------------------------|---------|--|--|
| Symbol | Parameter OA | V _{CC} (V) | | | T _A = -55°C to +125°C | T _A = -40°C to +85°C | | | |
| | | | Тур | T soom | Guaranteed L | imits | | | |
| VIH | Minimum High Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 2.0 2.0 | 2.0 2.0 | 2.0 2.0 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{IL} | Maximum Low Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 0.8 | 0.8 0.8 | 0.8 0.8 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{OH} | Minimum High Level | 4.5 5.5 | 4.49 5.49 | 4.4 5.4 | 4.4 5.4 | 4.4 5.4 | ٧ | $I_{OUT} = -50 \mu\text{A}$ | |
| | sect stati gas | 4.5 5.5 | os. | 3.86 4.86 | 3.70 4.70 | 3.76 4.76 | V | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IOH} = -24 \text{ mA}$ -24 mA | |
| V _{OL} | Maximum Low Level Output Voltage | 4.5 5.5 | 0.001 0.001 | 0.1 0.1 | 0.1 0.1 | 0.1 0.1 | V | $I_{OUT} = 50 \mu A$ | |
| | = 1U0V 0 V 0 V | 4.5 5.5 | | 0.32 0.32 | 0.4 0.4 | 0.37 0.37 | J wo Ju | $V_{IN} = V_{IL} \text{ or } V_{IH}$ I_{OL} 24 mA | |
| I _{IN} | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | 98.5 ±1.0 | μΑ | $V_{I} = V_{CC}$, GND | |
| loz | Maximum TRI-STATE Leakage Current | 5.5 | | ±0.5 | ±10.0 | ±5.0 | μΑ | $V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}, GND$ | |
| ICCT | Maximum I _{CC} /Input | 5.5 | 0.6 | | 1.6 | 1.5 | mA | $V_I = V_{CC} - 2.1V$ | |
| lold | †Minimum Dynamic | 5.5 | | | 57 | 86 | mA | V _{OLD} = 1.1V | |
| I _{OHD} | Output Current | 5.5 | | | -50 | con 0 -75 | mA | V _{OHD} = 3.85V | |
| Icc | Maximum Quiescent Supply Current | 5.5 | | 8.0 | 160 | 80 | μΑ | V _{IN} = V _{CC} or GND | |

^{*}All outputs loaded; thresholds on input associated with output under test.

[†]Maximum test duration 20 ms, one output loaded at a time.

Note: $I_{|N}$ and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC} . I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

[†]Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

| | PAACT | | TOANS | 74AC | ro | 54 | AC | 74 | AC | | |
|------------------|---|-----------------------|--|------------|-------------|---|--------------|--|----------------------------|-------|-------------|
| Symbol | Parameter | V _{CC} * (V) | T _A = +25°C C _L = 50 pF | | | T _A = -55°C to +125°C C _L = 50 pF | | $T_A = -40^{\circ}C$ $to +85^{\circ}C$ $C_L = 50 pF$ | | Units | Fig. No. |
| | nati milit | xati | Min | Тур | Max | Min | Max | Min | Max | | |
| fMAX | Maximum Clock Frequency | 3.3 5.0 | 75 95 | 112 153 | 0 | 55 80 | 6.0 | 60 85 | num Glock I spation Dev | MHz | XAM |
| t _{PLH} | Propagation Delay CP to O _n | 3.3 5.0 | 3.5 2.0 | 8.5 6.0 | 13.5 9.5 | 1.0 1.0 | 16.5 11.5 | 3.5 2.0 | 15.0 11.0 | ns | 2-6 |
| t _{PHL} | Propagation Delay CP to On | 3.3 5.0 | 3.5 2.0 | 7.5 5.5 | 12.0 8.5 | 1.0 1.0 | 15.0 10.5 | 3.5 2.0 | 13.5 9.5 | ns | 2-6 |
| ^t PZH | Output Enable Time | 3.3 5.0 | 2.5 2.0 | 7.0 5.0 | 11.0 8.5 | 1.0 1.0 | 13.0 9.5 | 2.5 2.0 | 12.0 9.0 | ns | 2-7 |
| t _{PZL} | Output Enable Time | 3.3 5.0 | 3.0 1.5 | 6.5 5.0 | 10.5 8.0 | 1.0 1.0 | 12.5 9.5 | 3.5 2.0 | 11.5 9.0 | ns | 2-8 |
| t _{PHZ} | Output Disable Time | 3.3 5.0 | 4.0 | 7.5 6.0 | 12.0 9.5 | 1.0 1.0 | 14.0 11.0 | 4.5 2.0 | 13.0 10.5 | ns | 2-7 |
| t _{PLZ} | Output Disable Time | 3.3 5.0 | 2.0 1.5 | 5.5 4.5 | 9.0 7.5 | 1.0 1.0 | 10.5 9.0 | 2.5 1.5 | 10.0 8.5 | ns | 2-8 |

^{*}Voltage Range 3.3 is 3.3V \pm 0.3V Voltage Range 5.0 is 5.0V \pm 0.5V

AC Operating Requirements: See Section 2 for Waveforms

| | 2.5 | 8.5 | 74 | AC | 54AC | 74AC | Units | Fig. No. |
|----------------|--|-------------------|------------|-----------------|---|--|-------|-------------|
| Symbol | Parameter | V _{CC} * | | + 25°C 50 pF | T _A = -55°C to +125°C C _L = 50 pF | T _A = -40°C to +85°C C _L = 50 pF | | |
| | 20 0.5 | | Тур | 2.5 | Guaranteed Min | imum | | |
| t _s | Set-Up Time, HIGH or LOW D _n to CP | 3.3 5.0 | 0.5 0 | 2.5 1.5 | 3.0 2.0 | 3.0 2.0 | ns | 2-9 |
| t _h | Hold Time, HIGH or LOW D _n to CP | 3.3 5.0 | -0.5 0 | 1.5 1.5 | 1.5 1.5 | 1.5 1.5 | ns | 2-9 |
| t _w | CP Pulse Width HIGH or LOW | 3.3 5.0 | 3.5 2.0 | 6.0 4.0 | 7.5 5.5 | 7.0 5.0 | ns | 2-6 |

^{*}Voltage Range 3.3 is 3.3V ± 0.3 V Voltage Range 5.0 is 5.0V ± 0.5 V

AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

| | Zanc | 04 | 74ACT T _A = +25°C C _L = 50 pF | | | 54ACT T _A = -55°C to + 125°C C _L = 50 pF | | 74/ | ACT | | |
|------------------|-------------------------------|-------------------|--|-----|------|---|------|--|-----------|-------|-------------|
| Symbol | Parameter | V _{CC} * | | | | | | $T_A = -40^{\circ}C$ $to +85^{\circ}C$ $C_L = 50 pF$ | | Units | Fig. No. |
| | gata siiM | xsid | Min | Тур | Max | Min | Max | Min | Max | | |
| f _{MAX} | Maximum Clock Frequency | 5.0 | 100 | 110 | | 70 | 3.3 | 85 | oiÓ murab | ns | XAM |
| t _{PLH} | Propagation Delay CP to On | 5.0 | 2.5 | 7.0 | 11.0 | 1.0 | 13.5 | 2.0 | 12.0 | ns | 2-6 |
| t _{PHL} | Propagation Delay CP to On | 5.0 | 2.0 | 6.5 | 10.0 | 1.0 | 12.5 | 1.5 | 11.0 | ns | 2-6 |
| t _{PZH} | Output Enable Time | 5.0 | 2.0 | 6.4 | 9.5 | 1.0 | 11.0 | 1.5 | 10.0 | ns | 2-7 |
| t _{PZL} | Output Enable Time | 5.0 | 2.0 | 6.0 | 9.0 | 1.0 | 11.0 | 1.5 | 10.0 | ns | 2-8 |
| t _{PHZ} | Output Disable Time | 5.0 | 2.0 | 7.0 | 10.5 | 1.0 | 12.0 | 1.5 | 11.5 | ns | 2-7 |
| t _{PLZ} | Output Disable Time | 5.0 | 2.0 | 5.5 | 8.5 | 1.0 | 10.0 | 1.5 | 9.0 | ns | 2-8 |

^{*}Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements: See Section 2 for Waveforms

| | 3.5 1000 | .017 | 74/ | ACT | 54ACT | 74ACT | Units | Fig. |
|----------------|--|--------------------------|------|-----------------|---|--|-------|------|
| Symbol | Parameter | V _{CC} * (V) | | + 25°C 50 pF | $T_A = -55^{\circ}C$ to $+125^{\circ}C$ $C_L = 50 pF$ | $T_A = -40^{\circ}C$ $to +85^{\circ}C$ $C_L = 50 pF$ | | |
| | | 814 | Тур | Section R | Guaranteed Min | imum | eteq0 | OA |
| ts | Set-Up Time, HIGH or LOW D _n to CP | 5.0 | 1.5 | 2.5 | 3.5 | 2.5 | ns | 2-9 |
| th | Hold Time, HIGH or LOW D _n to CP | 5.0 | -0.5 | 1.0 | 2.0 | 1.0 | ns | 2-9 |
| t _w | CP Pulse Width HIGH or LOW | 5.0 | 2.5 | 3.0 | 5.0 | 4.0 | ns | 2-6 |

^{*}Voltage Range 3.3 is 3.3V ± 0.3 V Voltage Range 5.0 is 5.0V ± 0.5 V

| Symbol | Parameter | AC/ACT | Units | Conditions |
|-----------------|-------------------------------|--------|--------|-----------------|
| Symbol | raidificter 6.0 | Тур | Oilits | Conditions |
| C _{IN} | Input Capacitance | 4.5 | pF | $V_{CC} = 5.0V$ |
| C _{PD} | Power Dissipation Capacitance | 40.0 | pF | $V_{CC} = 5.0V$ |



54AC/74AC646 • 54ACT/74ACT646 Octal Transceiver/Register with TRI-STATE® Outputs

General Description

The 'AC/'ACT646 consist of registered bus transceiver circuits, with outputs, D-type flip-flops and control circuitry providing multiplexed transmission of data directly from the input bus or from the internal storage registers. Data on the A or B bus will be loaded into the respective registers on the LOW-to-HIGH transition of the appropriate clock pin (CPAB or CPBA). The four fundamental data handling functions available are illustrated in *Figures 1-4*.

Features

- Independent registers for A and B buses
- Multiplexed real-time and stored data transfers
- **TRI-STATE outputs**
- 300 mil slim dual-in-line package
- Outputs source/sink 24 mA
- 'ACT646 has TTL compatible inputs

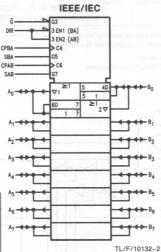
Ordering Code: See Section 5

Logic Symbols

CPAB AO A1 A2 A3 A4 A5 A6 A7 SAB DIR CPBA SBA

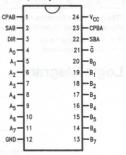
TL/F/10132-1

| Pin Names | Description |
|--------------------------------|-------------------------|
| A ₀ -A ₇ | Data Register A Inputs |
| | Data Register A Outputs |
| B ₀ -B ₇ | Data Register B Inputs |
| | Data Register B Outputs |
| CPAB, CPBA | Clock Pulse Inputs |
| SAB, SBA | Transmit/Receive Inputs |
| G | Output Enable Input |
| DIR | Direction Control Input |



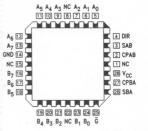
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC

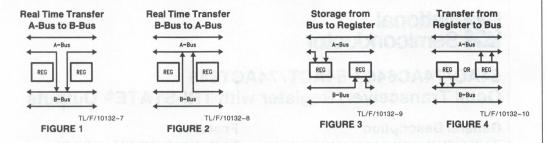


TL/F/10132-3

Pin Assignment for LCC and PCC



TL/F/10132-4



Function Table

| | | Ir | nputs | | | Data | 1/0* | Function |
|------|-------------|-------------|-------------|-------------|-------------|--------------------------------|--------------------------------|--|
| G | DIR | CPAB | СРВА | SAB | SBA | A ₀ -A ₇ | B ₀ -B ₇ | |
| HHH | X X X | H or L X | Hor L X | X X X | X X | Input | Input | Isolation Clock A _n Data into A Register Clock B _n Data into B Register |
| | H H H | X HorL | X X X | L H H | X X X | Input | Output | A _n to B _n —Real Time (Transparent Mode) Clock A _n Data into A Register A Register to B _n (Stored Mode) Clock A _n Data into A Register and Output to B _n |
| LLLL | L | X X X | X HorL | X X X | L H H | Output | Input | B _n to A _n —Real Time (Transparent Mode) Clock B _n Data into B Register B Register to A _n (Stored Mode) Clock B _n Data into B Register and Output to A _n |

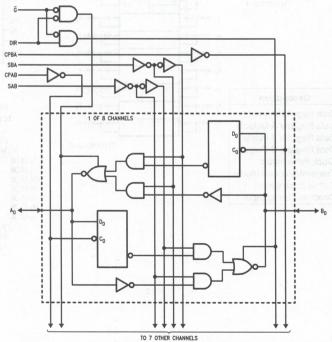
*The data output functions may be enabled or disabled by various signals at the G and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the appropriate clock inputs.

H = HIGH Voltage Level L = LOW Voltage Level

X = Immaterial

= LOW-to-HIGH Transition

Logic Diagram



TL/F/10132-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Part of the second seco | amily and operationalist |
|--|---------------------------------|
| Supply Voltage (V _{CC}) | -0.5V to $+7.0$ V |
| DC Input Diode Current (IIK) | |
| $V_{I} = -0.5V$ | -20 mA |
| $V_I = V_{CC} + 0.5V$ | + 20 mA |
| DC Input Voltage (V _I) | -0.5 V to $V_{CC} + 0.5$ V |
| DC Output Diode Current (IOK) | |
| $V_0 = -0.5V$ | -20 mA |
| $V_O = V_{CC} + 0.5V$ | + 20 mA |
| DC Output Voltage (V _O) | -0.5 V to to $V_{CC} + 0.5$ V |
| DC Output Source | |
| or Sink Current (IO) | ±50 mA |
| DC V _{CC} or Ground Current | |
| per Output Pin (I _{CC} or I _{GND}) | ±50 mA |
| Storage Temperature (T _{STG}) | -65°C to +150°C |
| | |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

Recommended Operating Conditions

| Supply Voltage (V _{CC}) 'AC 'ACT | 2.0V to 6.0V 4.5V to 5.5V |
|---|-----------------------------------|
| Input Voltage (V _I) | 0V to V _{CC} |
| Output Voltage (V _O) | 0V to V _{CC} |
| Operating Temperature (T _A) 74AC/ACT 54AC/ACT | -40°C to +85°C -55°C to +125°C |
| CDIP PDIP | 175°C 140°C |
| Input Rise and Fall Time (tr, tf) | |
| V _{CC} @ 3.0V | |
| V _{CC} @ 4.5V | |
| V _{CC} @ 5.5V Input Rise and Fall Time (t _r , t _f) (Note 2) (Typical) | |
| (Except Schmitt Inputs) 'ACT Devices V _{IN} from 0.8V to 2.0V, V _{meas} from 0.8V to 2.0V | DC Characti |
| V _{CC} @ 4.5V V _{CC} @ 5.5V | 10 ns/V 8 ns/V |

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

| | THOU I V | 8.6 | 74 | AC | 54AC | 74AC | eu Woule | Nevacos | |
|--|--|------------------------|-------------------------|----------------------|-----------------------------------|---------------------------------|------------------------|--|--|
| Symbol | Parameter | V _{CC} (V) | | | T _A = -55°C to + 125°C | T _A = -40°C to +85°C | Units | Conditions | |
| | $V = u_1 V^*$ | | Тур | | Guaranteed Li | mits | | | |
| V _{IH} AS AA (| Minimum High Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | V eJ Woji i | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{IL} HIV 10 () And NS | Maximum Low Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{OH} | Minimum High Level Output Voltage | 3.0 4.5 5.5 | 2.99 4.49 5.49 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | V | $I_{OUT} = -50 \mu\text{A}$ | |
| | | 3.0 4.5 5.5 | | 2.56 3.86 4.86 | 2.4 3.7 4.7 | 2.46 3.76 4.76 | V | $\label{eq:VIN} \begin{split} *V_{IN} &= V_{IL} or V_{IH} \\ &- 12 mA \\ I_{OH} &- 24 mA \\ &- 24 mA \end{split}$ | |
| V _{OL} | Maximum Low Level Output Voltage | 3.0 4.5 5.5 | 0.002 0.001 0.001 | 0.1 0.1 0.1 | 0.1 0.1 0.1 0.8 | 0.1 0.1 0.1 | inana V CarutO I | Ι _{ΟUT} = 50 μΑ | |
| | = (30) W coV = (V Au coV = (V Au | 3.0 4.5 5.5 | | 0.36 0.36 0.36 | 0.50 0.50 0.50 | 0.44 0.44 0.44 | Current V | $*V_{IN} = V_{IL} \text{ or } V_{IH}$ 12 mA I_{OL} 24 mA 24 mA | |
| I _{IN} | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | ±1.0 | μА | $V_I = V_{CC}$, GND | |

DC Characteristics for 'AC Family Devices (Continued)

| | | | 74 | AC | 54AC | 74AC | Qai Sun | Conditions | |
|------------------|-------------------------------------|------------------------|----------------------------------|-------------|----------------------------------|---------------------------------|-----------|---|--|
| Symbol | Parameter | V _{CC} (V) | T _A = | + 25°C | T _A = -55°C to +125°C | T _A = -40°C to +85°C | Units | | |
| | V S.A | | Тур | hatness com | Guaranteed Li | mits | ed) trien | | |
| loz | Maximum TRI-STATE® Current | 5.5 | (oV) egs s equip | ±0.5 | ±10.0 | ±5.0 | μА | $ \begin{array}{c} V_{I}\left(\text{OE}\right) = V_{IL}, V_{IH} \\ V_{I} = V_{CC}, V_{GND} \\ V_{O} = V_{CC}, GND \end{array} $ | |
| IOLD | †Minimum Dynamic | 5.5 | 1.73 | MANDALA | 50 | 75 | mA | V _{OLD} = 1.65V Max | |
| I _{OHD} | Output Current | 5.5 | distagini | T noises | -50 | -75 | mA | V _{OHD} = 3.85V Min | |
| Icc | Maximum Quiescent Supply Current | 5.5 | | 8.0 | 160.0 | 80.0 | μА | V _{IN} = V _{CC} or GND | |
| l _{OZT} | Maximum I/O Leakage Current | 5.5 | Oscio Oscio Oscio Oscio | ±0.6 | Am 00 ± 11.0 | ±6.0 | μΑ | $ \begin{aligned} & V_I\left(OE\right) = V_{IL}, V_{IH} \\ & V_I = V_{CC}, GND \\ & V_O = V_{CC}, GND \end{aligned} $ | |

^{*}All outputs loaded; thresholds on input associated with output under test.

Note: $I_{|N}$ and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC} . I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

| | 265 91 | | 74 | ACT | 54ACT | 74ACT | | | |
|-----------------|---|---|------------------------|--------------------------------|----------------------------------|--|-------|---|--|
| Symbol | Parameter | V _{CC} (V) | T _A = +25°C | | T _A = -55°C to +125°C | T _A = -40°C to +85°C | Units | Conditions | |
| | a for those devices which differ | reenau. | Тур | i neli 19, erb minimi trolo | Guaranteed Li | mits | | | |
| V _{IH} | Minimum High Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 2.0 2.0 | 2.0 2.0 | 2.0 2.0 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{IL} | Maximum Low Level Input Voltage | 이 경기 가게 되었다. 그리고 있는 그리고 있는 것이 없는데 | | 0.8 0.8 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | | | |
| V _{OH} | Minimum High Level Output Voltage | 4.5 5.5 | 4.49 5.49 | 4.4 5.4 | 4.4 5.4 | 4.4 5.4 | ٧ | $I_{OUT} = -50 \mu\text{A}$ | |
| | = TuoV | 4.5 5.5 | elink | 3.86 4.86 | 3.70 4.70 | 3.76 4.76 | V | $V_{IN} = V_{IL} \text{ or } V_{IH}$ -24 mA -24 mA | |
| V _{OL} | Maximum Low Level 4.5 Output Voltage 5.5 | | 0.001 0.001 | 0.1 0.1 | 0.1 0,1 | 0.1 0.1 | V | $I_{OUT} = 50 \mu A$ | |
| | = 30V to | 4.5 5.5 | | 0.36 0.36 | 0.50 0.50 | 0.44 0.44 | ٧ | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IN} = V_{IL} \text{ or } V_{IH}$ | |
| I _{IN} | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | ±1.0 | μА | $V_{I} = V_{CC}$, GND | |
| loz | Maximum TRI-STATE® Leakage Current | 5.5 | | ±0.5 | ±10.0 | ±5.0 | μА | $V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}, GND$ | |
| ICCT | Maximum I _{CC} /Input | 5.5 | 0.6 | β. 1. | 1.6 | 1.5 | mA | $V_{I} = V_{CC} - 2.1V$ | |
| lold | †Minimum Dynamic | 5.5 | | | 50 | 75 | mA | V _{OLD} = 1.65V Max | |
| IOHD | Output Current | 5.5 | | | -50 | -75 | mA | V _{OHD} = 3.85V Min | |
| ICC | Maximum Quiescent Supply Current | 5.5 | | 8.0 | 160.0 | 80.0 | μА | V _{IN} = V _{CC} or GND | |
| lozt | Maximum I/O Leakage Current | 5.5 | | ±0.6 ±11.0 | | ± 6.0 | μΑ | V_{I} (OE) = V_{IL} , V_{IH} V_{I} = V_{CC} , GND V_{O} = V_{CC} , GND | |

^{*}All outputs loaded; thresholds on input associated with output under test.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

[†]Maximum test duration 2.0 ms, one output loaded at a time.

[†]Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics

| | 2434 | DASS | | 74AC | | 54 | AC | 74 | AC | | |
|------------------|--|-------------------|--|-------------|--------------|------------|---|------------|------------------------|-------|------|
| Symbol | Parameter | V _{CC} * | $T_A = +25^{\circ}C$ $C_L = 50 \text{ pF}$ | | | to + | $T_A = -55^{\circ}C$ to $+125^{\circ}C$ $C_L = 50 pF$ | | -40°C 85°C 50 pF | Units | Fig. |
| | maminili | N beeing | Min | Тур | Max | Min | Max | Min | Max | | |
| t _{PLH} | Propagation Delay Clock to Bus | 3.3 5.0 | 4.0 2.5 | 10.5 7.5 | 16.5 12.0 | 1.0 1.0 | 20.0 14.0 | 3.0 2.0 | 18.5 13.0 | ns | 2-6 |
| t _{PHL} | Propagation Delay Clock to Bus | 3.3 5.0 | 3.0 2.0 | 9.5 6.5 | 14.5 10.5 | 1.0 1.0 | 17.5 12.0 | 2.5 1.5 | 16.0 11.5 | ns | 2-6 |
| t _{PLH} | Propagation Delay Bus to Bus | 3.3 5.0 | 2.5 1.5 | 7.5 5.0 | 12.0 8.0 | 1.0 1.0 | 15.0 10.0 | 2.0 1.0 | 13.5 9.0 | ns | 2-5 |
| t _{PHL} | Propagation Delay Bus to Bus | 3.3 5.0 | 1.5 1.5 | 7.5 5.0 | 12.5 9.0 | 1.0 1.0 | 14.5 9.5 | 1.5 1.0 | 13.5 9.5 | ns | 2-5 |
| ^t PLH | Propagation Delay SBA or SAB to A _n or B _n (w/ A _n or B _n HIGH or LOW) | 3.3 5.0 | 2.0 1.5 | 8.5 6.0 | 13.5 10.0 | 1.0 1.0 | 17.0 12.0 | 1.5 1.5 | 15.5 11.0 | ns | 2-6 |
| ^t PHL | Propagation Delay SBA or SAB to A _n or B _n (w/ A _n or B _n HIGH or LOW) | 3.3 5.0 | 1.5 1.5 | 8.5 6.0 | 13.5 10.0 | 1.0 1.0 | 17.0 12.0 | 1.5 1.5 | 15.0 11.0 | ns | 2-6 |
| t _{PZH} | Enable Time G to A _n or B _n | 3.3 5.0 | 2.5 1.5 | 7.0 5.0 | 11.5 8.5 | 1.0 1.0 | 13.0 9.5 | 2.0 1.5 | 12.5 9.0 | ns | 2-7 |
| t _{PZL} | Enable Time G to A _n or B _n | 3.3 5.0 | 2.5 1.5 | 7.5 5.5 | 12.5 9.0 | 1.0 1.0 | 15.5 11.0 | 2.0 1.5 | 14.0 10.0 | ns | 2-8 |
| t _{PHZ} | Disable Time G to A _n or B _n | 3.3 5.0 | 3.0 2.0 | 8.0 6.5 | 12.5 10.0 | 1.0 1.0 | 14.0 11.5 | 2.5 2.0 | 13.5 11.0 | ns | 2-7 |
| t _{PLZ} | Disable Time G to A _n or B _n | 3.3 5.0 | 2.0 1.5 | 7.5 6.0 | 12.0 9.5 | 1.0 1.0 | 13.5 11.0 | 2.0 1.5 | 13.5 10.5 | ns | 2-8 |
| t _{PZH} | Enable Time DIR to A _n or B _n | 3.3 5.0 | 2.0 1.5 | 6.5 5.0 | 11.0 7.5 | 1.0 1.0 | 14.5 10.5 | 1.5 1.0 | 12.0 8.5 | ns | 2-7 |
| t _{PZL} | Enable Time DIR to A _n or B _n | 3.3 5.0 | 2.5 1.5 | 7.0 5.0 | 11.5 8.0 | 1.0 1.0 | 16.0 12.5 | 2.0 1.0 | 13.0 9.0 | ns | 2-8 |
| t _{PHZ} | Disable Time DIR to A _n or B _n | 3.3 5.0 | 2.5 1.5 | 7.5 5.5 | 11.5 9.5 | 1.0 1.0 | 14.5 12.0 | 1.5 1.5 | 12.5 10.0 | ns | 2-7 |
| t _{PLZ} | Disable Time DIR to A _n or B _n | 3.3 5.0 | 1.5 1.5 | 7.5 5.5 | 12.0 9.5 | 1.0 1.0 | 16.5 12.0 | 1.5 1.5 | 13.5 10.5 | ns | 2-8 |

*Voltage Range 3.3 is 3.3V ± 0.3 V Voltage Range 5.0 is 5.0V ± 0.5 V

AC Operating Requirements

| | C 74AC | 446 | 7 | 4AC | 54AC | 74AC | | |
|----------------|---|-------------------|--------------|-------------------|---|--|-------|-------------|
| Symbol | Parameter | V _{CC} * | | + 25°C = 50 pF | $T_A = -55^{\circ}C$ to $+125^{\circ}C$ $C_L = 50 pF$ | $T_A = -40^{\circ}C$ to $+85^{\circ}C$ $C_L = 50 pF$ | Units | Fig. No. |
| | unid ni# xeM | raile: | Тур | gy f | Guaranteed Min | imum | | |
| t _s | Setup Time, HIGH or LOW Bus to Clock | 3.3 5.0 | 2.0 1.5 | 5.0 4.0 | 6.0 4.5 | 5.5 4.5 | ns | 2-9 |
| th | Hold Time, HIGH or LOW Bus to Clock | 3.3 5.0 | -1.5 -0.5 | 0.5 | 1.5 2.0 | 1.0 | ns | 2-9 |
| t _w | Clock Pulse Width HIGH or LOW | 3.3 5.0 | 2.0 2.0 | 3.5 3.5 | 5.0 5.0 | 4.5 3.5 | ns | 2-6 |

^{*}Voltage Range 3.3 is 3.3V ± 0.3 V Voltage Range 5.0 is 5.0V ± 0.5 V

AC Electrical Characteristics

| | TAACT | 101 | Là-C | 74ACT | | 544 | ACT | 74 | ACT | | |
|------------------|--|--------------------------|--|-------|------|------|--------------------------------|------|------------------------|-------|------|
| Symbol | Parameter | V _{CC} * (V) | T _A = +25°C C _L = 50 pF | | | to + | -55°C 125°C 50 pF | to + | -40°C 85°C 50 pF | Units | Fig. |
| | | dM bas | Min | Тур | Max | Min | Max | Min | Max | | |
| t _{PLH} | Propagation Delay Clock to Bus | 5.0 | 6.0 | 12.0 | 14.5 | 5.0 | WO.I | 3.0 | 16.0 | ns | 2-6 |
| t _{PHL} | Propagation Delay Clock to Bus | 5.0 | 6.0 | 12.0 | 14.5 | oa | WO | 3.5 | 16.0 | ns | 2-6 |
| t _{PLH} | Propagation Delay Bus to Bus | 5.0 | 4.5 | 8.5 | 10.5 | 0.8 | | 2.5 | 11.5 | ns | 2-5 |
| t _{PHL} | Propagation Delay Bus to Bus | 5.0 | 5.0 | 8.5 | 10.5 | | | 2.0 | 11.5 | ns | 2-5 |
| ^t PLH | Propagation Delay SBA or SAB to A _n to B _n (w/A _n or B _n HIGH or LOW) | 5.0 | 5.0 | 9.5 | 11.5 | | moter | 2.5 | 12.5 | ns | 2-6 |
| [†] PHL | Propagation Delay SBA or SAB to A _n to B _n (w/A _n or B _n HIGH or LOW) | 5.0 | 5.0 | 9.5 | 11.5 | 900 | isance i Capacitn setton | 2.5 | 12.5 | ns | 2-6 |
| t _{PZH} | Enable Time G to A _n or B _n | 5.0 | 6.0 | 9.0 | 11.0 | | | 1.5 | 12.0 | ns | 2-7 |
| t _{PZL} | Enable Time G to A _n or B _n | 5.0 | 5.0 | 9.0 | 11.0 | | | 3.0 | 12.0 | ns | 2-8 |
| t _{PHZ} | Disable Time G to A _n or B _n | 5.0 | 7.5 | 10.5 | 13.0 | | | 4.5 | 14.5 | ns | 2-7 |
| t _{PLZ} | Disable Time G to A _n or B _n | 5.0 | 5.5 | 10.0 | 12.5 | | | 3.0 | 14.0 | ns | 2-8 |
| t _{PZH} | Enable Time DIR to A _n or B _n | 5.0 | 5.5 | 6.5 | 10.5 | | | 1.5 | 11.5 | ns | 2-7 |
| t _{PZL} | Enable Time DIR to A _n or B _n | 5.0 | 4.0 | 6.5 | 10.5 | | | 3.0 | 11.5 | ns | 2-8 |
| t _{PHZ} | Disable Time DIR to A _n or B _n | 5.0 | 5.5 | 8.5 | 12.5 | | | 4.5 | 13.5 | ns | 2-7 |
| t _{PLZ} | Disable Time DIR to A _n or B _n | 5.0 | 4.0 | 8.5 | 12.5 | | | 3.0 | 13.5 | ns | 2-8 |

^{*}Voltage Range 5.0 is 5.0V \pm 0.5V

AC Operating Requirements

| | T ZAKOT | DAAB | 74 | ACT | 54 | ACT | 74ACT | | |
|----------------|---|-------------------|--|-----|--|-----------|--|-------|-------------|
| Symbol | Parameter | V _{CC} * | T _A = +25°C C _L = 50 pF | | $T_{A} = -55^{\circ}C$ $to + 125^{\circ}C$ $C_{L} = 50 \text{ pF}$ | | T _A = -40°C to +85°C C _L = 50 pF | Units | Fig. No. |
| | xelvi nilvi xelvi | 11/2 | Тур | ay? | Guarai | nteed Min | imum | | |
| ts | Setup Time, HIGH or LOW BUS to Clock | 5.0 | 2.5 | 7.0 | 0.8 | 0.8 | Short 0.8 | ns | 2-9 |
| t _h | Hold Time, HIGH or LOW Bus to Clock | 5.0 | 0 | 2.5 | 0.8 | o.a | 2.5 | ns | 2-9 |
| tw | Clock Pulse Width HIGH or LOW | 5.0 | 4.5 | 7.0 | 4.5 | 03 | 8.0 | ns | 2-6 |

^{*}Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

| Symbol | Parameter | AC/ACT | Units | Conditions | |
|---|----------------------------------|--------|-------|-----------------|--|
| Суппрог | T di dinotoi | Тур | Onito | | |
| C _{IN} | Input Capacitance | 4.5 | pF | $V_{CC} = 5.0V$ | |
| C _{I/O} Input/Output Capacitance | | 15.0 | pF | $V_{CC} = 5.0V$ | |
| C _{PD} | Power Dissipation Capacitance | 60.0 | pF | $V_{CC} = 5.0V$ | |



54AC/74AC648 Octal Transceiver/Register with TRI-STATE® Outputs

General Description

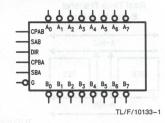
The 'AC648 consists of registered bus transceiver circuits, with outputs, D-type flip-flops and control circuitry providing multiplexed transmission of data directly from the input bus or from the internal storage registers. Data on the A or B bus will be loaded into the respective registers on the LOW-to-HIGH transition of the appropriate clock pin (CPAB or CPBA). The four fundamental data handling functions available are illustrated in *Figures 1* thru 4 (See Page 2).

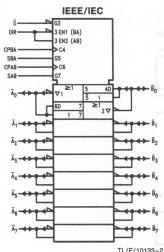
Features

- Independent registers for A and B buses
- Multiplexed real-time and stored data transfers
- **TRI-STATE outputs**
- 300 mil slim dual-in-line package
- Outputs source/sink 24 mA
- Inverted data to output

Ordering Code: See Section 5

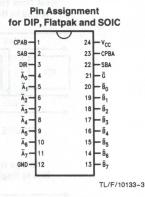
Logic Symbols

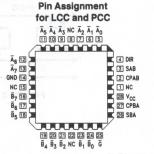




| Standard and the second | | | | | | | | | |
|--|-----------------------------------|--|--|--|--|--|--|--|--|
| Pin Names | Description | | | | | | | | |
| $\overline{A}_0 - \overline{A}_7$ | Data Register A Inputs, | | | | | | | | |
| | Data Register A TRI-STATE Outputs | | | | | | | | |
| $\overline{B}_0 - \overline{B}_7$ | Data Register B Inputs, | | | | | | | | |
| | Data Register B TRI-STATE Outputs | | | | | | | | |
| CPAB, CPBA | Clock Pulse Inputs | | | | | | | | |
| SAB, SBA | Transmit/Receive Inputs | | | | | | | | |
| DIR, G | Output Enable Inputs | | | | | | | | |

Connection Diagrams





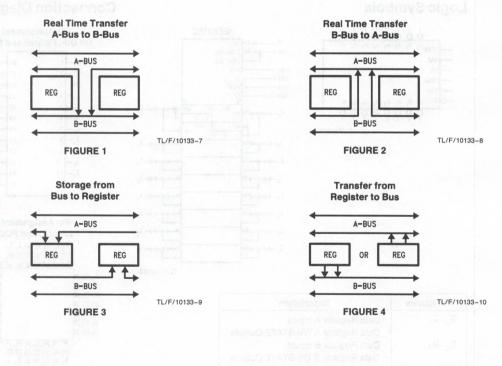
TL/F/10133-4

Function Table

| | Inputs | | | | | Data | 1/0* | Function | |
|---|--------|------|-------|-----|----------|--------------------------------|--------------------------------------|--|--|
| G | DIR | СРАВ | СРВА | SAB | SBA | A ₀ -A ₇ | B ₀ -B ₇ | Tunction | |
| Н | X | HorL | HorL | X | X | | | Isolation | |
| Н | X | _ | X | X | X | Input | Input Input | Clock An Data into A Register | |
| Н | X | X | 5 | X | X | diin a | | Clock B _n Data into B Register | |
| L | Н | X | X | L | X | | | A _n to B _n —Real Time (Transparent Mode) | |
| L | Н | _ | X | L | X | Input | Input | 0 | Clock An Data into A Register |
| L | Н | HorL | X | Н | X | | | Output | A Register to B _n (Stored Mode) |
| L | Н | _ | X | Н | X | d is poli | iscover chants. scultos oroxidado | Clock An Data into A Register and Output to Bn | |
| L | L | X | X | X | TALBA | Tigs aud | nueni sett si | B _n to A _n —Real Time (Transparent Mode) | |
| L | L | X | | X | nis L 0 | Output | A en de | Clock Bn Data into B Register | |
| L | L | X | HorL | X | OF HOS | | Output Input | B Register to An (Stored Mode) | |
| L | L | X | J 100 | X | sh tH ev | el 6 lieu | Lectural Old a | Clock Bn Data into B Register and Output to An | |

^{*}The data output functions may be enabled or disabled by various signals at the G and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the clock inputs.

__ = LOW-to-HIGH Transition

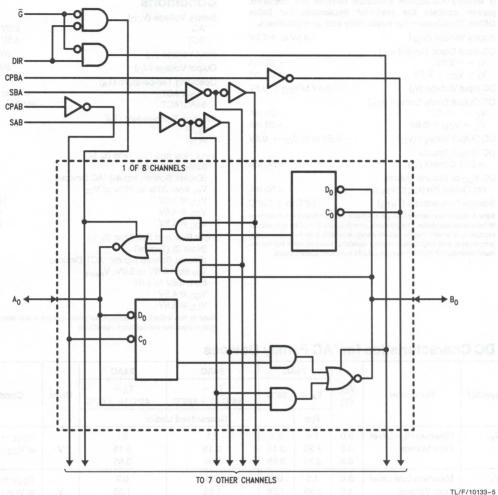


H = HIGH Voltage Level

L = LOW Voltage Level

X = Irrelevant

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Office/ Distributors for available | inty and specimounions. |
|---|---------------------------------|
| Supply Voltage (V _{CC}) | -0.5V to $+7.0V$ |
| DC Input Diode Current (IIK) | |
| $V_1 = -0.5V$ | -20 mA |
| $V_I = V_{CC} + 0.5V$ | + 20 mA |
| DC Input Voltage (V _I) | -0.5 V to $V_{CC} + 0.5$ V |
| DC Output Diode Current (IOK) | |
| $V_{O} = -0.5V$ | -20 mA |
| $V_O = V_{CC} + 0.5V$ | + 20 mA |
| DC Output Voltage (V _O) | -0.5 V to to V $_{CC}$ + 0.5V |
| DC Output Source | |
| or Sink Current (I _O) | ±50 mA |
| DC V _{CC} or Ground Current | |
| per Output Pin (I _{CC} or I _{GND}) | ±50 mA |
| Storage Temperature (T _{STG}) | -65°C to +150°C |
| | |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

Recommended Operating Conditions

| Supply Voltage (V _{CC}) | |
|---|-----------------------|
| 'AC | 2.0V to 6.0V |
| 'ACT | 4.5V to 5.5V |
| Input Voltage (V _I) | 0V to V _{CC} |
| Output Voltage (V _O) | 0V to V _{CC} |
| Operating Temperature (T _A) | |
| 74AC/ACT | -40°C to +85°C |
| 54AC/ACT | -55°C to +125°C |
| Junction Temperature (T,I) | |
| CDIP | 175°C |
| PDIP | 140°C |
| Input Rise and Fall Time (t _r , t _f) (Note 2) (Typical) (Except Schmitt Inputs) 'AC Devices | |
| V _{IN} from 30% to 70% of V _{CC} | |
| V _{CC} @ 3.0V | 150 ns/V |
| V _{CC} @ 4.5V | 40 ns/V |
| V _{CC} @ 5.5V | 25 ns/V |
| Input Rise and Fall Time (t _r , t _f) (Note 2) (Typical) (Except Schmitt Inputs) 'ACT Devices | |
| V _{IN} from 0.8V to 2.0V, V _{meas} | |
| from 0.8V to 2.0V | |
| V _{CC} @ 4.5V | 10 ns/V |
| V _{CC} @ 5.5V | 8 ns/V |

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

| | Parameter | and the same | 74 | AC | 54AC | 74AC | | |
|-----------------|--------------------------------------|------------------------|-------------------------|----------------------|-----------------------------------|---------------------------------|-------|--|
| Symbol | | V _{CC} (V) | T _A = +25°C | | T _A = -55°C to + 125°C | T _A = -40°C to +85°C | Units | Conditions |
| | | | Тур | | Guaranteed L | imits | | |
| V _{IH} | Minimum High Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ |
| V _{IL} | Maximum Low Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ |
| V _{OH} | Minimum High Level Output Voltage | 3.0 4.5 5.5 | 2.99 4.49 5.49 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | V | $I_{OUT} = -50 \mu\text{A}$ |
| | | 3.0 4.5 5.5 | | 2.56 3.86 4.86 | 2.4 3.7 4.7 | 2.46 3.76 4.76 | V | $\begin{tabular}{ll} *V_{\text{IN}} &= V_{\text{IL}} \text{ or } V_{\text{IH}} \\ &- 12 \text{ mA} \\ I_{\text{OH}} &- 24 \text{ mA} \\ &- 24 \text{ mA} \\ \end{tabular}$ |
| V _{OL} | Maximum Low Level Output Voltage | 3.0 4.5 5.5 | 0.002 0.001 0.001 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | ٧ | I _{OUT} = 50 μA |
| | | 3.0 4.5 5.5 | | 0.36 0.36 0.36 | 0.50 0.50 0.50 | 0.44 0.44 0.44 | V | $*V_{IN} = V_{IL} \text{ or } V_{IH}$ 12 mA I_{OL} 24 mA 24 mA |
| I _{IN} | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | ±1.0 | μΑ | $V_{I} = V_{CC}$, GND |

DC Characteristics for 'AC Family Devices (Continued)

| | Parameter | | $T_A = +25^{\circ}C$ $T_A = T_A =$ | | 74AC | | | |
|------------------|-------------------------------------|---------------------|--|------|---------------|---------------------------------|-------|--|
| Symbol | | V _{CC} (V) | | | | T _A = -40°C to +85°C | Units | Conditions |
| | | | Тур | | Guaranteed Li | | | |
| IOLD | †Minimum Dynamic | 5.5 | Seattle r | 1987 | 50 | 75 | mA | V _{OLD} = 1.65V Max |
| I _{OHD} | Output Current | 5.5 | | | -50 | -75 | mA | V _{OHD} = 3.85V Min |
| Icc | Maximum Quiescent Supply Current | 5.5 | | 8.0 | 160.0 | 80.0 | μА | $V_{IN} = V_{CC}$ or GND |
| l _{OZT} | Maximum I/O Leakage Current | 5.5 | | ±0.6 | ±11.0 | ±6.0 | μΑ | V_{I} (OE) = V_{IL} , V_{IH} V_{I} = V_{CC} , GND V_{O} = V_{CC} , GND |

^{*}All outputs loaded; thresholds on input associated with output under test.

Note: $I_{|N}$ and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC} . I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

AC Electrical Characteristics

| | p.a = _{CCV} | | 74AC | | | 54AC | | 74 | AC | 100 N | Fig. |
|------------------|--|--------------------------|------------|--|--------------|---|-----|--|--------------|-------|------|
| Symbol | Parameter | V _{CC} * (V) | | $T_A = +25^{\circ}C$ $C_L = 50 \text{ pF}$ | | $T_A = -55^{\circ}C$ to $+125^{\circ}C$ $C_L = 50 pF$ | | $T_A = -40^{\circ}C$ to $+85^{\circ}C$ $C_L = 50 pF$ | | Units | |
| | | | Min | Тур | Max | Min | Max | Min | Max | 1 | |
| t _{PLH} | Propagation Delay Clock to Bus | 3.3 5.0 | 1.5 1.5 | 10.0 7.0 | 15.5 11.0 | | | 1.5 1.5 | 17.0 12.0 | ns | 2-6 |
| t _{PHL} | Propagation Delay Clock to Bus | 3.3 5.0 | 1.5 1.5 | 8.5 6.0 | 13.5 10.5 | | | 1.5 1.5 | 14.5 11.5 | ns | 2-6 |
| t _{PLH} | Propagation Delay Bus to Bus | 3.3 5.0 | 1.5 1.5 | 6.0 4.0 | 10.0 7.0 | | | 1.5 1.0 | 11.0 7.5 | ns | 2-5 |
| t _{PHL} | Propagation Delay Bus to Bus | 3.3 5.0 | 1.5 1.5 | 5.5 3.5 | 9.0 7.5 | | | 1.5 1.0 | 10.0 8.0 | ns | 2-5 |
| t _{PLH} | Propagation Delay SBA or SAB to A _n or B _n (with A _n or B _n HIGH or LOW) | 3.3 5.0 | 1.5 1.5 | 7.5 5.5 | 12.5 9.0 | | | 1.5 14.0 1.5 10.0 | | ns | 2-6 |
| t _{PHL} | Propagation Delay SBA or SAB to A _n or B _n (with A _n or B _n HIGH or LOW) | 3.3 5.0 | 1.5 1.5 | 7.5 5.5 | 12.5 9.5 | | | 1.5 1.5 | 14.0 10.5 | ns | 2-6 |
| t _{PZH} | Enable Time G to A _n or B _n | 3.3 5.0 | 1.5 1.5 | 6.5 5.0 | 11.0 8.0 | | | 1.0 1.0 | 11.5 9.0 | ns | 2-7 |
| t _{PZL} | Enable Time G to A _n or B _n | 3.3 5.0 | 1.5 1.5 | 7.0 5.0 | 11.0 8.0 | | | 1.0 1.0 | 12.5 9.0 | ns | 2-8 |
| t _{PHZ} | Disable Time G to A _n or B _n | 3.3 5.0 | 1.5 1.5 | 7.5 6.0 | 12.0 10.0 | | | 1.0 1.0 | 13.0 11.0 | ns | 2-7 |
| t _{PLZ} | Disable Time G to A _n or B _n | 3.3 5.0 | 1.5 1.5 | 7.0 5.5 | 11.5 9.0 | | | 1.0 1.0 | 12.5 10.0 | ns | 2-8 |
| t _{PZH} | Enable Time DIR to A _n or B _n | 3.3 5.0 | 1.5 1.5 | 6.0 4.5 | 12.5 9.5 | | | 1.0 1.0 | 14.0 10.5 | ns | 2-7 |
| t _{PZL} | Enable Time DIR to A _n or B _n | 3.3 5.0 | 1.5 1.5 | 6.5 4.5 | 13.0 9.0 | | | 1.5 1.0 | 14.5 10.5 | ns | 2-8 |
| t _{PHZ} | Disable Time DIR to A _n or B _n | 3.3 5.0 | 1.5 1.5 | 7.0 5.5 | 11.5 9.0 | | | 1.0 1.0 | 13.5 10.0 | ns | 2-7 |
| t _{PLZ} | Disable Time DIR to A _n or B _n | 3.3 5.0 | 1.5 1.5 | 7.0 5.0 | 13.5 9.5 | | | 1.5 1.0 | 15.0 10.0 | ns | 2-8 |

*Voltage Range 3.3 is 3.3V ± 0.3 V

Voltage Range 5.0 is 5.0V ±0.5V

[†]Maximum test duration 2.0 ms, one output loaded at a time.

AC Operating Requirements

| | CARC | | 74 | AC | 54AC | 74AC | | |
|----------------|--|-------------------|--|------------|--|--|-------|-------------|
| Symbol | Parameter | V _{CC} * | T _A = +25°C C _L = 50 pF | | T _A = -55°C to + 125°C C _L = 50 pF | $T_A = -40^{\circ}C$ to $+85^{\circ}C$ $C_L = 50 pF$ | Units | Fig. No. |
| | | SAICT No. | Тур | | Guaranteed Min | Guaranteed Minimum | | |
| ts | Setup Time, HIGH or LOW, Bus to Clock | 3.3 5.0 | 2.0 1.5 | 3.0 2.0 | 8 | 3.5 2.0 | ns | 2-9 |
| t _h | Hold Time, HIGH or LOW, Bus to Clock | 3.3 5.0 | -1.5 -0.5 | 0 1.0 | 08 | 0 1.0 | ns | 2-9 |
| tw | Clock Pulse Width HIGH or LOW | 3.3 5.0 | 2.0 2.0 | 3.5 3.0 | | 4.0 3.0 | ns | 2-6 |

^{*}Voltage Range 3.3 is 3.3V ± 0.3 V Voltage Range 5.0 is 5.0V ± 0.5 V

Capacitance

| Symbol | Parameter | AC/ACT | Units | Conditions | |
|------------------|-------------------------------|--------|--------------|-----------------|--|
| Symbol | Falametei | Тур | e no Contact | Conditions | |
| C _{IN} | Input Capacitance | 4.5 | pF | $V_{CC} = 5.0V$ | |
| C _{PD} | Power Dissipation Capacitance | 65.0 | pF | $V_{CC} = 5.0V$ | |
| C _{I/O} | Input/Output Capacitance | 15.0 | pF | $V_{CC} = 5.0V$ | |



54ACT/74ACT657 Octal Bidirectional Transceiver with 8-Bit Parity Generator/Checker and TRI-STATE® Outputs

General Description

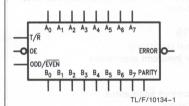
The 'ACT657 contains eight noninverting buffers with TRI-STATE outputs and an 8-bit parity generator/checker, and is intended for bus-oriented applications. The Transmit/Receive (T/\overline{R}) input determines the direction of the data flow through the bidirectional transceivers. Transmit (active-HIGH) enables data from A ports to B ports; Receive (active-LOW) enables data from B ports to A ports. The Output Enable input disables both the A and B ports by placing them in a High Z condition.

The parity generator detects whether an even or odd number of bits on the A port is HIGH, depending on the condition of the ODD/EVEN input, and the ERROR output is LOW if not equal.

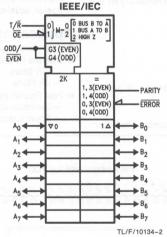
Features

- 300 mil 24-pin Slimline DIP
- TRI-STATE outputs
- 'ACT657 has TTL-compatible inputs

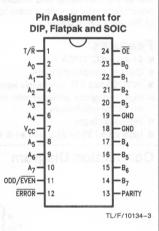
Logic Symbols

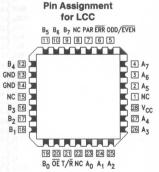


| Pin Names | Description |
|--------------------------------|------------------------|
| A ₀ -A ₇ | Data Inputs |
| | Data Outputs |
| B ₀ -B ₇ | Data Inputs |
| | Data Outputs |
| T/R | Transmit/Receive Input |
| ŌĒ | Enable Input |
| PARITY | Parity Input/Output |
| ODD/EVEN | ODD/EVEN Parity Input |
| ERROR | Error Output |



Connection Diagrams





TL/F/10134-4

ADVANCE INFORMATION



54ACT/74ACT705 Arithmetic Logic Unit for Digital Signal Processing Applications

General Description

The 'ACT705 is a high-speed arithmetic processing integrated circuit which is packaged in an 84-pin leadless chip carrier. It features separate input buses that provide data and instruction codes to a high-speed single-cycle 16-bit ALU and an 8-bit by 8-bit parallel multiplier/accumulator.

The ALU is a 16-bit parallel design which supports sixteen arithmetic and logic functions, as well as carry-in/out and borrow-in/out. The multiplier/accumulator, which offers a full 16-bit product, provides for unsigned, signed, mixed mode and imaginary number multiplication. Product accumulation with sum and difference arithmetic is available in each multiplier operating mode.

The 16-bit results of the ALU and multiplier/accumulator are multiplexed to a single set of TRI-STATE® output buffers. The two ALU and multiplier/accumulator carry-out bits, as well as the 4-bit status field indicating ALU and multiplier/accumulator error conditions make up the remaining six bits of the entire 22-bit output.

Features

- 84-pin, PCC, CPGA
- Outputs source/sink 8 mA
- 'ACT705 has TTL-compatible inputs
- High throughput achieved with high degree of parallelism in the architecture
- Pipelined stages
- High-speed 16-bit ALU and an 8 x 8 complex multiplier

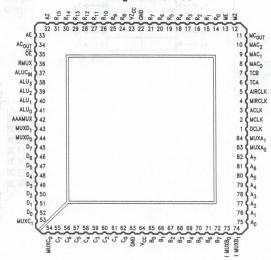
- 16-bit full ALU performs sixteen Boolean and arithmetic functions with carry-in and carry-out
- 8 x 8 parallel multiplier supports unsigned, signed, complex or mixed mode multiplications, produces 16-bit result with carry-out
- Separate data and instruction buses allow instruction fetches in parallel with execution—single cycle operation
- Accepts 8- or 16-bit data and delivers a 16-bit output
- Data register bank configured to accept a combination of 8- or 16-bit data
- Separate clocks for ALU instruction, multiplier instruction, data, ALU accumulator and multiplier accumulator registers
- Clustered clock pins for ease of board design
- 16-bit ALU/accumulator with feedback to ALU input
- Status of accumulator inputs is monitored: conditions monitored include twos complement overflow, underflow or equal-to-zero

Applications

- Voice-band signal processing
- Discrete Fourier transform applications
 - FIR filters
 - IIR filters
- Fast Fourier transform applications
 - Spectrum analysis
 - Speech recognition

Connection Diagram

Pin Assignment for PCC



TL/F/10135-1



54ACT/74ACT715 Programmable Video Sync Generator

General Description

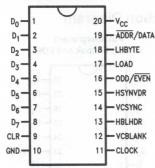
The 'ACT715 is a 20-pin TTL-input compatible device capable of generating Horizontal, Vertical and Composite Sync and Blank signals for televisions and monitors. All pulse widths are completely definable by the user. The device is capable of generating signals for both interlaced and noninterlaced modes of operation. Equalization and serration pulses can be introduced into the Composite Sync signal when needed.

Four additional signals can also be made available when Composite Sync or Blank are used. These signals can be used to generate horizontal and vertical driving pulses, horizontal or vertical gating pulses, cursor position or vertical Interrupt signal.

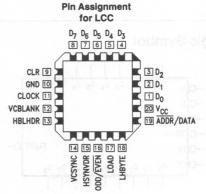
The 'ACT715 makes no assumptions concerning the system that it will be used in. Line rate and field/frame rate are all a function of the values programmed into the data registers, the status register, and the input clock frequency.

Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/10137-1



TL/F/10137-2



54ACT/74ACT725 512 x 9 First In, First Out Memory (FIFO)

General Description

The 512 x 9 FIFO is a first-in, first-out dual port memory capable of asynchronous, simultaneous read and write. Other important features are: expansion capability in both the word depth and bit width, half-full flag capability in the single device mode, empty and full warning flags, ring pointers for zero fall-through time; it is suited for high-speed applications.

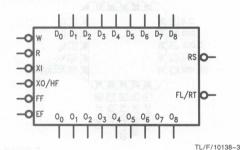
Features

- First-in, first-out dual port memory
- 512 x 9 organization
- Low power consumption
- Asynchronous and simultaneous read and write
- Fully expandable by word depth and/or bit width
- Half-full flag capability in single device mode
- Master/slave multiprocessing applications
- Bidirectional and rate buffer applications
- Empty and full warning flags
- Auto retransmit capability
- Outputs source/sink 8 mA
- 'ACT725 has TTL-compatible inputs
- Pin and functionality compatible with IDT7201

Logic Symbol

Din Names

FL/RT



| Pin Names | | Description | |
|-----------|--------------------------------|-------------------------------|--|
| | D ₀ -D ₈ | Data Inputs | |
| | 00-08 | Data Outputs | |
| | W | Write Enable | |
| | R | Read Enable | |
| 1 | XI | Expansion In | |
| | XO/HF | Expansion Out, Half-Full Flag | |
| | EF | Empty Flag | |
| | FF | Full Flag | |
| | RS | Reset | |

First Load/Retransmit

Connection Diagram

Pin Assignment for DIP, Flatpak and SOIC



TL/F/10138-1



54ACT/74ACT818 8-Bit Diagnostic Register

General Description

The 'ACT818 is a high-speed, general-purpose pipeline register with an on-board diagnostic register for performing serial diagnostics and/or writable control store loading.

The D-to-Y path provides an 8-bit parallel data path pipeline register for normal system operation. The diagnostic register can load parallel data to or from the pipeline register and can output data through the D input port (as in WCS loading).

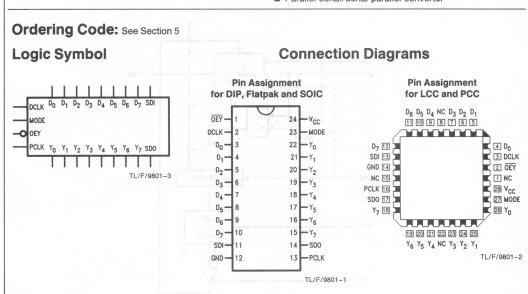
The 8-bit diagnostic register has multiplexer inputs that select parallel inputs from the Y-port or adjacent bits in the diagnostic register to operate as a right-shift-only register. This register can then participate in a serial loop throughout the system where normal data, address, status and control registers are replaced with 'ACT818 diagnostic pipeline registers. The loop can be used to scan in a complete test routine starting point (Data, Address, etc.). Then after a specified number of machine cycles it scans out the results to be inspected for the expected results. WCS loading can be accomplished using the same technique. An instruction word can be serially shifted into the shadow register and written into the WCS RAM by enabling the D output.

Features

- On-line and off-line system diagnostics
- Swaps the contents of diagnostic register and output register
- Diagnostic register and diagnostic testing
- Cascadable for wide control words as used in microprogramming
- Edge-triggered D registers
- Outputs source/sink 24 mA
- 'ACT818 has TTL-compatible inputs
- 'ACT818 is functionally- and pin-compatible to AMD Am29818 and MMI 74S818

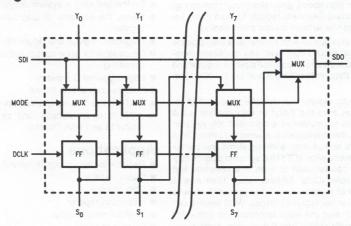
Applications

- Register for microprogram control store
- Status register
- Data register
- Instruction register
- Interrupt mask register
- Pipeline register
- General purpose register
- Parallel-serial/serial-parallel converter



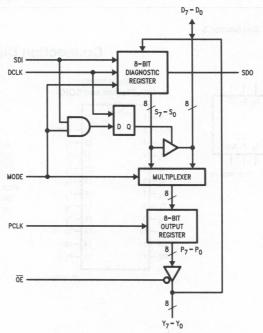
| Pin Names | Description | | |
|--------------------------------|-------------------------|--|--|
| D ₀ -D ₇ | Data Inputs | | |
| SĎI | Serial Data Input | | |
| DCLK | Diagnostics Clock | | |
| MODE | Control Input | | |
| PCLK | Pipeline Register Clock | | |
| OEY | Output Enable Input | | |
| SDO | Serial Data Output | | |
| $Y_0 - Y_7$ | Data Outputs | | |

Diagnostic Register



TL/F/9801-4

Block Diagram



Functional Description

Data transfers into the diagnostic register occur on the LOW-to-HIGH transition of DCLK. Mode and SDI determine what data source will be loaded. The pipeline register is loaded on the LOW-to-HIGH transition of PCLK. Mode selects whether the data source is the data input or the diagnostic state.

nostic register output. Because of the independence of the clock inputs, data can be shifted in the diagnostic register via DCLK and loaded into the pipeline register from the data input via PCLK simultaneously, as long as no setup or hold times are violated. This simultaneous operation is legal.

Function Table

| O'BB of O'Ch Inputs | | | | TOA | Outputs | Operation | |
|---------------------|------|------|------|---------------------|--|--|---|
| SDI | MODE | DCLK | PCLK | SDO | DO Diagnostic Reg. Pipeline Reg. | | Operation |
| × | L | _ | × | S7 | SI <si -="" 1,<br="">SO<sd<sub>I</sd<sub></si> | NA | Serial Shift; D ₇ -D ₀ Disabled |
| Χ | L | Х | _ | S7 | NA | PI <di< td=""><td>Normal Load Pipeline Register</td></di<> | Normal Load Pipeline Register |
| L | Н | | X | hengos of acus n | SI <yi< td=""><td>NA</td><td>Load Diagnostic Register from Y; DI Disabled</td></yi<> | NA | Load Diagnostic Register from Y; DI Disabled |
| x | Н | × | _ | SDI | NA NA | PI <si< td=""><td>Load Pipeline Register from Diagnostic Register</td></si<> | Load Pipeline Register from Diagnostic Register |
| н | Н | ~ | X | H S | Hold Hold | NA | Hold Diagnostic Register; DI Enabled |

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

^{✓ =} LOW-to-HIGH Clock Transition

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Office/Distributors for availability | ty and specifications. |
|--|------------------------------|
| Supply Voltage (V _{CC}) | -0.5V to $+7.0V$ |
| DC Input Diode Current (IIK) | |
| $V_1 = -0.5V$ | -20 mA |
| $V_I = V_{CC} + 0.5V$ | + 20 mA |
| DC Input Voltage (V _I) | $-0.5V$ to $V_{CC} + 0.5V$ |
| DC Output Diode Current (IOK) | |
| $V_{O} = -0.5V$ | -20 mA |
| $V_O = V_{CC} + 0.5V$ | + 20 mA |
| DC Output Voltage (V _O) | -0.5 V to $V_{CC} + 0.5$ V |
| DC Output Source or Sink Current (I _O) | ±50 mA |
| DC V _{CC} or Ground Current per Output Pin (I _{CC} or I _{GND}) | ±50 mA |
| Storage Temperature (T _{STG}) | -65°C to +150°C |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

Recommended Operating Conditions

| Supply Voltage (Vcc) | |
|--|-----------------------|
| 'AC | 2.00 10 6.00 |
| 'ACT | 4.57 10 5.57 |
| Input Voltage (V _I) | 0V to V _{CC} |
| Output Voltage (V _O) | 0V to V _{CC} |
| Operating Temperature (T _A) | |
| 74AC/ACT | -40°C to +85°C |
| 54AC/ACT | -55°C to +125°C |
| Junction Temperature (T _J) | |
| CDIP | 175°C |
| PDIP | 140°C |
| Input Rise and Fall Time (t _r , t _f) | |
| (Note 2) (Typical) | |
| (Except Schmitt Inputs) 'AC Devices V _{IN} from 30% to 70% of V _{CC} | |
| V _{CC} @ 3.0V | 150 ns/V |
| V _{CC} @ 4.5V | 40 ns/V |
| V _{CC} @ 5.5V | 25 ns/V |
| Input Rise and Fall Time (t _r , t _f) | |
| (Note 2) (Typical) | |
| (Except Schmitt Inputs) 'ACT Devices | |
| V _{IN} from 0.8V to 2.0V, V _{meas} from 0.8V to 2.0V | |
| V _{CC} @ 4.5V | 10 ns/V |
| V _{CC} @ 5.5V | 8 ns/V |

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'ACT Family Devices

| Symbol | Parameter | | 74 | ACT | 54ACT | 74ACT | | |
|------------------|---|------------------------|------------------|--------------|----------------------------------|---------------------------------|-------|--|
| | | V _{CC} (V) | T _A = | + 25°C | T _A = -55°C to +125°C | T _A = -40°C to +85°C | Units | Conditions |
| | | | Тур | | Guaranteed Li | mits | | |
| V _{IH} | Minimum High Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 2.0 2.0 | 2.0 2.0 | 2.0 2.0 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ |
| V _{IL} | Maximum Low Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 0.8 0.8 | 0.8 0.8 | 0.8 0.8 | | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ |
| I _{IN} | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±10.0 | ±1.0 | μΑ | $V_{IN} = V_{CC}$ |
| loz | Maximum TRI-STATE Leakage Current | 5.5 | | ±0.5 | ±10.0 | ±5.0 | μΑ | $\overline{OE} = V_{IH}$ $V_{OUT} = 0V, V_{CC}$ |
| Icc | Maximum Quiescent Supply Current | 5.5 | | 1.0 | | | mA | $V_{IN} = V_{CC}$ or GN |
| ГССТ | Maximum Additional I _{CC} /Input | 5.5 | | | 1.6 | 1.5 | mA | $V_{IN} = V_{CC} - 2.1$ $V_{CC} = 5.5$ V |
| V _{OH} | Minimum HIGH Level Output Voltage, Y ₀ -Y ₇ Outputs | 4.5 5.5 | | 3.86 4.86 | 3.70 4.70 | 3.76 4.76 | V | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $I_{OH} = -24 \text{ mA}$ $I_{OH} = -24 \text{ mA}$ |
| | Minimum HIGH Level Output Voltage, D ₀ -D ₇ , SDO Outputs | 4.5 5.5 | | 3.86 4.86 | 3.70 4.70 | 3.76 4.76 | V | $I_{OH} = -8 \text{ mA}$ $I_{OH} = -8 \text{ mA}$ |
| V _{OL} | Maximum LOW Level Output Voltage, Y0-Y7 Outputs | 4.5 5.5 | | 0.36 0.36 | 0.50 0.50 | 0.44 0.44 | V | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $I_{OL} = 24 \text{ mA}$ $I_{OL} = 24 \text{ mA}$ |
| | Maximum LOW Level Output Voltage, D ₀ -D ₇ , SDO Outputs | 4.5 5.5 | | 0.36 0.36 | 0.50 0.50 | 0.44 0.44 | V | I _{OL} = 8 mA I _{OL} = 8 mA |
| I _{OLD} | Minimum Dynamic Output Current, Y ₀ -Y ₇ Outputs | 5.5 | | | 50 | 75 | mA | V _{OLD} = 1.65V M |

DC Characteristics for 'ACT Family Devices (Continued)

| | PARCY | | 74ACT | | 54ACT | 74ACT | | |
|------------------|--|------------------------|------------------|--------|----------------------------------|---------------------------------|-------------------|------------------------------|
| Symbol | Parameter | V _{CC} (V) | T _A = | + 25°C | T _A = -55°C to +125°C | T _A = -40°C to +85°C | Units | Conditions |
| .elf | San | | Тур | | Guaranteed Li | mits | 1007 2015 2280 11 | A COMME |
| I _{OHD} | Minimum Dynamic Output Current, Y ₀ -Y ₇ Outputs | 5.5 | M bael | Ouaran | -50 | -75 | mA | V _{OHD} = 3.85V Min |
| lold | Minimum Dynamic Output Current, D ₀ -D ₇ , SDO Outputs (Note 1) | 5.5 | | | 32 | 32 | mA | V _{OLD} = 5.5V |
| lohd | Minimum Dynamic Output Current, D ₀ -D ₇ , SDO Outputs (Note 1) | 5.5 | | į | -32 | -32 | mA | V _{OHD} = 3.3V |

*All outputs loaded; thresholds on input associated with output under test.

Note 1: Test load 50 pF, 500Ω to ground.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

| Symbol | Parameter | | | 74ACT | | 54/ | ACT | 74 | ACT | - | |
|------------------|-----------------------------------|-------------------|--|-------|------|---|-----|--|------|-------|-------------|
| | | V _{CC} * | T _A = +25°C C _L = 50 pF | | | T _A = -55°C to +125°C C _L = 50 pF | | $T_A = -40^{\circ}C$ to $+85^{\circ}C$ $C_L = 50 pF$ | | Units | Fig. No. |
| 6-5 | en 0.1 | | Min | Тур | Max | Min | Max | Min | Max | | |
| t _{PHL} | Propagation Delay PCLK to Y | 5.0 | 3.0 | 6.0 | 9.0 | 0.5 | 5,0 | 2.5 | 9.5 | ns | 2-5 |
| t _{PLH} | Propagation Delay PCLK to Y | 5.0 | 3.0 | 6.5 | 9.0 | .0- | | 2.5 | 10.0 | ns | 2-5 |
| t _{PHL} | Propagation Delay MODE to SDO | 5.0 | 4.0 | 8.0 | 11.0 | 0.5 | | 3.5 | 12.0 | ns | 2-5 |
| t _{PLH} | Propagation Delay MODE to SDO | 5.0 | 4.0 | 8.0 | 11.5 | | | 4.0 | 12.5 | ns | 2-5 |
| t _{PHL} | Propagation Delay SDI to SDO | 5.0 | 3.5 | 7.5 | 10.5 | 0.8 | 0.0 | 3.0 | 12.0 | ns | 2-5 |
| t _{PLH} | Propagation Delay SDI to SDO | 5.0 | 3.5 | 7.5 | 10.5 | 0.8 | 5.0 | 3.5 | 12.0 | ns | 2-5 |
| t _{PHL} | Propagation Delay DCLK to SDO | 5.0 | 4.5 | 9.0 | 12.5 | 0.8 | 0.0 | 4.0 | 14.0 | ns | 2-5 |
| t _{PLH} | Propagation Delay DCLK to SDO | 5.0 | 4.5 | 9.5 | 13.0 | | | 4.0 | 14.5 | ns | 2-5 |
| t _{PZL} | Output Enable Time | 5.0 | 2.5 | 6.0 | 9.0 | | | 2.5 | 10.0 | ns | 2-8 |
| t _{PLZ} | Output Disable Time OEY to Yn | 5.0 | 1.5 | 5.5 | 8.0 | DANGA | | 1.0 | 9.0 | ns | 2-8 |
| t _{PZL} | Output Enable Time DCLK to Dn | 5.0 | 3.0 | 8.0 | 12.0 | GAL | 1 | 3.0 | 13.5 | ns | 2-8 |
| t _{PLZ} | Output Disable Time DCLK to Dn | 5.0 | 2.0 | 8.5 | 11.0 | - C.R. | nes | 1.5 | 12.0 | ns | 2-8 |
| ^t PZH | Output Enable Time | 5.0 | 3.0 | 8.0 | 10.0 | | | 2.5 | 11.0 | ns | 2-7 |
| t _{PHZ} | Output Disable Time OEY to Yn | 5.0 | 2.5 | 9.0 | 11.0 | | | 2.0 | 11.5 | ns | 2-7 |
| t _{PZH} | Output Enable Time DCLK to Dn | 5.0 | 3.0 | 6.5 | 11.5 | | | 3.0 | 13.0 | ns | 2-7 |
| t _{PHZ} | Output Disable Time DCLK to Dn | 5.0 | 3.0 | 7.5 | 12.0 | | | 2.0 | 13.0 | ns | 2-7 |

*Voltage Range 5.0 is 5.0V \pm 0.5V.

AC Operating Requirements: See Section 2 for Waveforms 10 A 101 and an including the section 2 for Waveforms

| | Parameter | V _{CC} * | 744 | ACT | 54ACT | 74ACT | | |
|------------------|---------------------------------|-------------------|--|------|---|--|---------------------|-------------|
| Symbol | | | $T_A = +25^{\circ}C$ $C_L = 50 \text{ pF}$ | | T _A = -55°C to +125°C C _L = 50 pF | T _A = -40°C to +85°C C _L = 50 pF | Units | Fig. No. |
| 3,85V Mur | E CHOV | | Тур | | Guaranteed Mini | mum | Dumaniwi Dumanio | CH |
| t _s | Setup Time D to PCLK | 5.0 | 1.0 | 4.0 | | 5.0 | ns | 2- |
| t _h | Hold Time D to PCLK | 5.0 | 0.0 | 1.0 | | 1.0 | ns | 2- |
| t _s | Setup Time MODE to PCLK | 5.0 | 2.5 | 4.5 | | 5.5 menu | ns | 2- |
| t _h | Hold Time MODE to PCLK | 5.0 | -1.0 | 0.0 | se sehrup krátop rítke bája | 0.0 | ns | 2- |
| t _s | Setup Time Y to DCLK | 5.0 | 0.5 | 2.5 | .010 25 0.10 | 2.5 | ns | 2- |
| t _h | Hold Time Y to DCLK | 5.0 | 0 | 1.0 | rishes sadhar | 1.5 | ns | 2- |
| t _s | Setup Time MODE to DCLK | 5.0 | 2.0 | 4.0 | E AT | 4.0 | ns | 2- |
| th | Hold Time MODE to DCLK | 5.0 | -0.5 | 1.0 | WT mild | 1.0 | ns | 2- |
| t _s | Setup Time SDI to DCLK | 5.0 | 2.0 | 3.5 | 3.8 0.8 1 | 4.5 | ns | 2- |
| t _h S | Hold Time SDI to DCLK | 5.0 | -0.5 | 1.0 | 0,6 | 1.0 | ns | 2- |
| ts | Setup Time DCLK to PCLK | 5.0 | 6.0 | 9.0 | 0.8 | 10.5 | ns | 2- |
| ts | Setup Time PCLK to DCLK | 5.0 | 6.0 | 11.0 | 3.6 | 11.5 | ns | 2- |
| t _w | Pulse Width PCLK HIGH or LOW | 5.0 | 2.0 | 3.0 | 3.6 | 3.0 | ns | 2- |
| t _w | Pulse Width DCLK HIGH or LOW | 5.0 | 2.0 | 3.0 | 3.8 d.c | 3.0 | ns | 2- |

Note 1: Test load 50 pF, 500Ω to ground. *Voltage range 5.0 is $5.0V \pm 0.5V$.

Capacitance

| Symbol | Parameter | AC/ACT | Units | Conditions | |
|-----------------|-------------------------------|--------|-------|-----------------|--|
| Symbol | Parameter | Тур | 0.8 | | |
| C _{IN} | Input Capacitance | 4.5 | pF | $V_{CC} = 5.0V$ | |
| C _{PD} | Power Dissipation Capacitance | 20 | pF | $V_{CC} = 5.0V$ | |



54AC/74AC821 • 54ACT/74ACT821 10-Bit D Flip-Flop with TRI-STATE® Outputs

General Description

The 'AC/'ACT821 is a 10-bit D flip-flop with TRI-STATE outputs arranged in a broadside pinout.

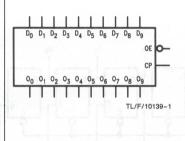
The 'AC/'ACT821 is functionally identical to the AM29821.

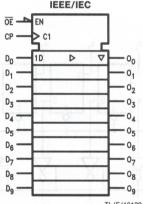
Features

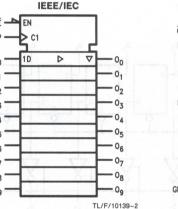
- TRI-STATE outputs for bus interfacing
- Noninverting outputs
- Outputs source/sink 24 mA
- 'ACT821 has TTL-compatible inputs

Ordering Code: See Section 5

Logic Symbols

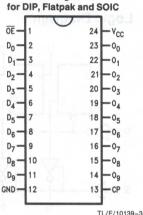






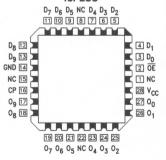
Connection Diagrams

Pin Assignment



Pin Names Description $D_0 - D_9$ **Data Inputs Data Outputs** $O_0 - O_9$ OE Output Enable Input CP Clock Input

Pin Assignment for LCC



TL/F/10139-4

Functional Description

The 'AC/'ACT821 consists of ten D-type edge-triggered flipflops. The buffered Clock (CP) and buffered Output Enable (OE) are common to all flip-flops. The flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH CP transition. With OE LOW the contents of the flip-flops are available at

the outputs. When \overline{OE} is HIGH the outputs go to the high impedance state. Operation of the \overline{OE} input does not affect the state of the flip-flops.

The 'AC/'ACT821 is functionally and pin compatible with the AM29821.

Function Table

| | Inputs | | Internal | Outputs | Function | |
|---------|--------|---|------------------------|---------|-------------|--|
| OE CP D | | D | Q | 0 | al Archolit | |
| Н | _ | L | ine W L aude at | a Z | High Z | |
| Н | _ | Н | Heed 15 | Z | High Z | |
| L | _ | L | L | L | Load | |
| L | | Н | Н | Н | Load | |

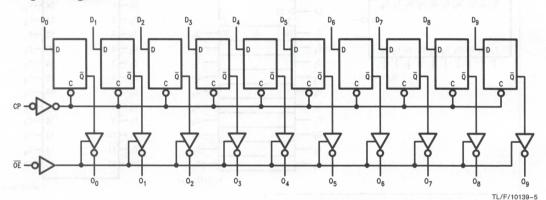
H = HIGH Voltage Level

L = LOW Voltage Level

Z = HIGH Impedance

__ = LOW-to-HIGH Clock Transition

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1) Recommended Operating

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Ciliad, Didilibatoro rei aramai | mity and oppositionations. | |
|---|--|--|
| Supply Voltage (V _{CC}) | -0.5V to +7.0V | |
| DC Input Diode Current (I_{IK}) $V_I = -0.5V$ $V_I = V_{CC} + 0.5V$ | -20 mA +20 mA | |
| DC Input Voltage (V _I) | -0.5 V to $V_{CC} + 0.5$ V | |
| DC Output Diode Current (I_{OK}) $V_O = -0.5V$ $V_O = V_{CC} + 0.5V$ DC Output Voltage (V_O) | -20 mA +20 mA -0.5V to to V _{CC} + 0.5V | |
| DC Output Source or Sink Current (I _O) | ± 50 mA | |
| DC V _{CC} or Ground Current per Output Pin (I _{CC} or I _{GND}) | ±50 mA | |
| Storage Temperature (T _{STG}) | −65°C to +150°C | |
| | | |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

Conditions

| Supply Voltage (V _{CC}) | |
|--|-------------------------|
| 'AC | |
| 'ACT | 4.5V to 5.5V |
| Input Voltage (V _I) | 0V to V _{CC} |
| Output Voltage (V _O) | 0V to V _{CC} |
| Operating Temperature (T _A) | |
| 74AC/ACT | -40°C to +85°C |
| 54AC/ACT | -55°C to +125°C |
| Junction Temperature (T _J) | |
| CDIP | 175°C |
| PDIP | 140°C |
| Input Rise and Fall Time (t _r , t _f) | |
| (Note 2) (Typical) | |
| (Except Schmitt Inputs) 'AC Devices | |
| 111 | TMaxer on text duration |
| - 00 | 150 ns/V |
| V _{CC} @ 4.5V V _{CC} @ 5.5V | 40 ns/V 25 ns/V |
| | |
| Input Rise and Fall Time (t _r , t _f) (Note 2) (Typical) | |
| (Except Schmitt Inputs) 'ACT Devices | |
| V _{IN} from 0.8V to 2.0V, V _{meas} | |
| from 0.8V to 2.0V | |
| V _{CC} @ 4.5V | 10 ns/V |
| V _{CC} @ 5.5V | 8 ns/V |
| Note 2. See individual datasheets for those device | s which differ from the |

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

| | - 00 ^{1/10} | 8.0 | 74. | AC | 54AC | 74AC | 30.81 | lo V Jugai |
|-----------------------------|---|------------------------|-------------------------|----------------------|----------------------|----------------------|-------|---|
| Symbol | Parameter | V _{CC} (V) | | | Units | Conditions | | |
| | $V = M_i V_i$ | | Тур | | Guaranteed L | imits | 1 | |
| V _{IH} | Minimum High Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ |
| VIL HIV 10 J Am AS | Maximum Low Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ |
| VoH | Minimum High Level Output Voltage | 3.0 4.5 5.5 | 2.99 4.49 5.49 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | ٧ | $I_{OUT} = -50 \mu A$ |
| | $V_{ij} = V_{ij}$ | 3.0 4.5 5.5 | | 2.56 3.86 4.86 | 2.4 3.7 4.7 | 2.46 3.76 4.76 | V - | $\label{eq:VIN} \begin{split} ^*\text{V}_{\text{IN}} &= \text{V}_{\text{IL}} \text{ or V}_{\text{IH}} \\ &- 12 \text{ mA} \\ \text{I}_{\text{OH}} &- 24 \text{ mA} \\ &- 24 \text{ mA} \end{split}$ |
| V _{OL} xeM Vea: | Maximum Low Level Output Voltage | 3.0 4.5 5.5 | 0.002 0.001 0.001 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | V | $I_{OUT} = 50 \mu\text{A}$ |
| | VIV = VO | 3.0 4.5 5.5 | | 0.36 0.36 0.36 | 0.50 0.50 0.50 | 0.44 0.44 0.44 | ٧ | $^*V_{IN} = V_{IL} \text{ or } V_{IH}$ 12 mA I_{OL} 24 mA 24 mA |
| I _{IN} | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | ±1.0 | μА | $V_{I} = V_{CC}$, GND |

DC Characteristics for 'AC Family Devices (Continued)

| | | | 74 | AC | 54AC | 74AC | Units | Conditions | |
|------------------|-------------------------------------|---------------------|-------------------------|----------|-----------------------------------|---------------------------------|-------|--|--|
| Symbol | Parameter | V _{CC} (V) | T _A = | + 25°C | T _A = -55°C to + 125°C | T _A = -40°C to +85°C | | | |
| | 49 | | Тур | effoy to | Guaranteed L | imits. | | no shalo lugii ofi | |
| loz | Maximum TRI-STATE® Current | 5.5 | 671 898 81 976 70 | ±0.5 | ±10.0 | ±5.0 | μА | V_{I} (OE) = V_{IL} , V_{IH} $V_{I} = V_{CC}$, GND $V_{O} = V_{CC}$, GND | |
| I _{OLD} | †Minimum Dynamic | 5.5 | Econos: | Tacina | 50 | 75 | mA | V _{OLD} = 1.65V Max | |
| IOHD | Output Current | 5.5 | | sigo | -50 | -75 | mA | V _{OHD} = 3.85V Min | |
| Icc | Maximum Quiescent Supply Current | 5.5 | ip i Cara | 8.0 | 160.0 | 80.0 | μА | $V_{IN} = V_{CC}$ or GND | |

^{*}All outputs loaded; thresholds on input associated with output under test.

DC Characteristics for 'ACT Family Devices

| | Parameter Parameter | (atuan | 74ACT | | 54ACT | 74ACT | Eliando M | CAT to incented bright | |
|------------------|--------------------------------------|------------------------|------------------|--------------|----------------------------------|---------------------------------|-----------|--|--|
| Symbol | | V _{CC} (V) | T _A = | + 25°C | T _A = -55°C to +125°C | T _A = -40°C to +85°C | Units | Conditions | |
| | | | Тур | 8.8 00V | Guaranteed L | imits | | | |
| V _{IH} | Minimum High Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 2.0 2.0 | 2.0 2.0 | 2.0 2.0 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{IL} | Maximum Low Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 0.8 | 0.8 0.8 | 0.8 0.8 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{OH} | Minimum High Level Output Voltage | 4.5 5.5 | 4.49 5.49 | 4.4 5.4 | 4.4 5.4 | 4.4 5.4 | ٧ | $I_{OUT} = -50 \mu\text{A}$ | |
| | - TUO ^V | 4.5 5.5 | artient. | 3.86 4.86 | 3.70 4.70 | 3.76 4.76 | ٧ | $\label{eq:VIN} \begin{split} ^*\text{V}_{\text{IN}} &= \text{V}_{\text{IL}} \text{ or V}_{\text{IH}} \\ &-24 \text{ mA} \\ &-24 \text{ mA} \end{split}$ | |
| V _{OL} | Maximum Low Level Output Voltage | 4.5 5.5 | 0.001 0.001 | 0.1 0.1 | 0.1 0.1 | 0.1 | ٧ | $I_{OUT} = 50 \mu A$ | |
| | -00/10 V | 4.5 5.5 | | 0.36 0.36 | 0.50 0.50 | 0.44 | v | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IN} = V_{IL} \text{ or } V_{IH}$ | |
| I _{IN} | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | 98.4 68.6 ±1.0 | μΑ | $V_I = V_{CC}$, GND | |
| loz | Maximum TRI-STATE® Current | 5.5 | | ±0.5 | ±10.0 | ±5.0 | μΑ | $V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}, GND$ | |
| ГССТ | Maximum I _{CC} /Input | 5.5 | 0.6 | | 1.6 | 1.5 | mA | $V_{\rm I} = V_{\rm CC} - 2.1V$ | |
| I _{OLD} | †Minimum Dynamic Output Current | 5.5 | | | 50 | 75 | mA | V _{OLD} = 1.65V Max | |
| IOHD | | 5.5 | | | -50 | -75 | mA | V _{OHD} = 3.85V Min | |
| Icc | Maximum Quiescent Supply Current | 5.5 | | 8.0 | 160.0 | 80.0 | μΑ | V _{IN} = V _{CC} or GND | |

^{*}All outputs loaded; thresholds on input associated with output under test.

[†]Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{1N} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC} .

I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

[†]Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

| | TOART | | TOARE | 74AC | TOA | 54 | AC | 74 | AC | | |
|------------------|---|--------------------------|------------|---|-------------|-----------|-------------------------|--|--------------------|-------|-------------|
| Symbol | Parameter | V _{CC} * (V) | | _A = +25° C _L = 50 pl | | to + | -55°C 125°C 50 pF | $T_A = -40^{\circ}C$ to $+85^{\circ}C$ $C_L = 50 pF$ | | Units | Fig. No. |
| | Man Man | 1 | Min | Тур | Max | Min | Max | Min | Max | | |
| f _{max} | Maximum Clock Frequency | 3.3 5.0 | 110 120 | 145 160 | Da. | 95 100 | 0.8 | 100 110 | noiD mishi make | MHz | 2-3 |
| t _{PLH} | Propagation Delay CP to O _n | 3.3 5.0 | 3.0 2.0 | 8.0 6.0 | 13.0 9.5 | 1.0 | 16.0 11.5 | 3.0 2.0 | 15.0 10.5 | ns | 2-6 |
| t _{PHL} | Propagation Delay CP to On | 3.3 5.0 | 3.0 2.0 | 8.0 5.5 | 13.0 9.5 | 1.0 | 16.0 11.5 | 3.0 2.0 | 15.0 10.5 | ns | 2-6 |
| ^t PZH | Output Enable Time | 3.3 5.0 | 2.5 1.5 | 6.0 4.5 | 11.0 8.0 | 1.0 | 13.0 10.0 | 2.5 1.5 | 12.0 9.0 | ns | 2-7 |
| t _{PZL} | Output Enable Time | 3.3 5.0 | 2.5 1.5 | 6.5 5.0 | 11.0 8.0 | 1.0 | 13.5 10.0 | 2.5 1.5 | 12.0 9.0 | ns | 2-8 |
| t _{PHZ} | Output Disable Time | 3.3 5.0 | 2.5 1.5 | 6.5 5.0 | 10.5 8.0 | 1.0 | 12.0 10.0 | 2.5 1.5 | 11.0 8.5 | ns | 2-7 |
| t _{PLZ} | Output Disable Time | 3.3 5.0 | 2.5 1.5 | 6.0 4.5 | 10.5 8.0 | 1.0 | 12.0 10.0 | 2.5 1.5 | 11.0 8.5 | ns | 2-8 |

*Voltage Range 3.3 is 3.3V ± 0.3 V Voltage Range 5.0 is 5.0V ± 0.5 V

AC Operating Requirements

| | 200 | | 74/ | AC | 54AC | 74AC | | |
|----------------|---|--------------------------|--|------------|---|--|-------|-------------|
| Symbol | Parameter | V _{CC} * (V) | T _A = +25°C C _L = 50 pF | | $T_A = -55^{\circ}C$ to $+125^{\circ}C$ $C_L = 50 pF$ | T _A = -40°C to +85°C C _L = 50 pF | Units | Fig. No. |
| | CV 16.01 1.02 25000 40 | | Тур | | Guaranteed Min | imum | | |
| ts | Setup Time, HIGH or LOW D _n to CP | 3.3 5.0 | -1.0 -1.0 | 1.5 1.5 | 2.5 2.5 | 1.5 90 d 1.5 | ns | 2-9 |
| t _h | Hold Time, HIGH or LOW D _n to CP | 3.3 5.0 | -1.0 -1.0 | 3.5 3.5 | 4.0 4.0 | 4.0 4.0 | ns | 2-9 |
| t _w | CP Pulse Width HIGH or LOW | 3.3 5.0 | 3.5 2.5 | 5.0 4.0 | 6.0 5.0 | 5.5 4.0 | ns | 2-6 |

*Voltage Range 3.3 is 3.3V \pm 0.3V Voltage Range 5.0 is 5.0V \pm 0.5V

AC Electrical Characteristics

| | TAC | | SAAC | 74ACT | 710.0 | 54A | СТ | 74 | ACT | | |
|------------------|-------------------------------|--------------------------|------|---|-----------|------------|------------|--------------|------------------|-------|-------------|
| Symbol | Parameter | V _{CC} * (V) | | $ \begin{array}{cccccccccccccccccccccccccccccccccccc$ | | to + 125°C | | 5°C to +85°C | | Units | Fig. No. |
| | xalá nilá | X.31 | Min | Тур | Max | Min | Max | Min | Max | | |
| f _{max} | Maximum Clock Frequency | 5.0 | 120 | 150 | 85 0.0 | 85 011 | 0.3 5.0 | 110 | тит Сюс излоч | MHz | 2-3 |
| t _{PLH} | Propagation Delay CP to On | 5.0 | 2.0 | 6.0 | 9.5 | 1.0 | 11.5 | 1.5 | 10.5 | ns | 2-6 |
| t _{PHL} | Propagation Delay CP to On | 5.0 | 2.5 | 6.0 | 9.5 | 1.0 0.8 | 11.5 | 2.0 | 10.5 | ns | 2-6 |
| t _{PZH} | Output Enable Time | 5.0 | 2.5 | 7.0 | 10.5 | 1.0 | 12.5 | 2.0 | 11.5 | ns | 2-7 |
| t _{PZL} | Output Enable Time | 5.0 | 2.5 | 7.0 | 10.5 | 1.0 | 13.0 | 2.0 | 12.0 | ns | 2-8 |
| t _{PHZ} | Output Disable Time | 5.0 | 1.5 | 7.5 0.8 | 12.0 | 1.0 | 13.5 | 1.0 | 13.0 | ns | 2-7 |
| t _{PLZ} | Output Disable Time | 5.0 | 1.5 | 7.0 | 10.5 | 1.0 | 12.5 | 1.0 | 11.5 | ns | 2-8 |

^{*}Voltage Range 5.0 is 5.0V \pm 0.5V

AC Operating Requirements

| | | | 744 | CT | 54ACT | 74ACT | Units | Fig. |
|----------------|--|-------------------|-----------------------------------|--------------------|--|--|-------|------|
| Symbol | Parameter | V _{CC} * | T _A = C _L = | + 25°C 50 pF | T _A = -55°C to + 125°C C _L = 50 pF | $T_A = -40^{\circ}C$ $to +85^{\circ}C$ $C_L = 50 pF$ | | |
| | 70 06 = 10 3 | | Тур | Guaranteed Minimum | | imum | | |
| ts | Setup Time, HIGH or LOW Dn to CP | 5.0 | 2.5 | 2.0 | 4.0 WO | 1 10 Hi 2.5 | ns | 2-9 |
| t _h | Hold Time, HIGH or LOW D _n to CP | 5.0 | -0.5 | 2.0 | 3.0 | 2.5 | ns | 2-9 |
| t _w | CP Pulse Width HIGH or LOW | 5.0 | 3.0 | 4.5 | 6.0 | 5.5 _{// eclus} | ns | 2-6 |

^{*}Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

| Symbol | Parameter | rameter AC/ACT | | Conditions | |
|-----------------|----------------------------------|----------------|-------|------------------------|--|
| Oyillb01 | rarameter | Тур | Units | Conditions | |
| CIN | Input Capacitance | 4.5 | pF | $V_{CC} = 5.0V$ | |
| C _{PD} | Power Dissipation Capacitance | 35.0 | pF | V _{CC} = 5.0V | |



54AC/74AC823 • **54ACT/74ACT823 9-Bit D Flip-Flop**

General Description

The 'ACT823 is a 9-bit buffered register. It features Clock Enable and Clear which are ideal for parity bus interfacing in high performance microprogramming systems. The 'ACT823 offers noninverting outputs and is fully compatible with AMD's Am29823.

Features

- Outputs source/sink 24 mA
- TRI-STATE® outputs for bus interfacing
- Inputs and outputs are on opposite sides
- 'ACT823 has TTL-compatible inputs

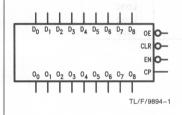
The information for the 'AC823 is Advanced Information only.

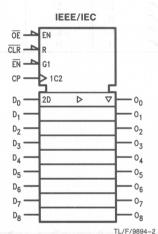
Ordering Code: See Section 5

Logic Symbols

CP

FN





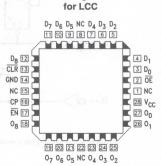
Connection Diagrams



Pin Names Description D0-D8 Data Inputs O0-O8 Data Outputs OE Output Enable CLR Clear

Clock Input

Clock Enable



Pin Assignment

TL/F/9894-4

Functional Description

The 'ACT823 consists of nine D-type edge-triggered flipflops. These have TRI-STATE outputs for bus systems organized with inputs and outputs on opposite sides. The buffered clock (CP) and buffered Output Enable (\overline{OE}) are common to all flip-flops. The flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH CP transition. With \overline{OE} LOW, the contents of the flip-flops are available at the outputs. When \overline{OE} is HIGH, the outputs go to the high impedance state. Operation of the \overline{OE} input does not affect

the state of the flip-flops. In addition to the Clock and Output Enable pins, there are Clear $(\overline{\text{CLR}})$ and Clock Enable $(\overline{\text{EN}})$ pins. These devices are ideal for parity bus interfacing in high performance systems.

When $\overline{\text{CLR}}$ is LOW and $\overline{\text{OE}}$ is LOW, the outputs are LOW. When $\overline{\text{CLR}}$ is HIGH, data can be entered into the flip-flops. When $\overline{\text{EN}}$ is LOW, data on the inputs is transferred to the outputs on the LOW-to-HIGH clock transition. When the $\overline{\text{EN}}$ is HIGH, the outputs do not change state, regardless of the data or clock input transitions.

Function Table

| | action cha | Inputs | s singino 5 | na muqn | Internal | Output | Function |
|-------|------------|--------|-------------|---------|----------------|-----------------|-------------|
| ŌĒ | CLR | EN | СР | D | Q | 0 | T direction |
| Н | X | L | _ | L | ino su (smior) | DEPOT Z PO A RE | High Z |
| Н | X | L | _ | Н | Н | Z | High Z |
| Н | L | X | X | X | L | Z | Clear |
| L | L | X | X | X | L | L | Clear |
| Н | Н | Н | X | X | NC | Z | Hold |
| e Cab | SIGHION | H | X | X | NC | NC | Hold |
| Н | Н | L | _ | L | L | Z | Load |
| Н | H | L | _ | Н | H | Z | Load |
| Jos P | Н | and E | _ | L | L | L | Load |
| L | Н | L | _ | Н | Н | Н -0 | Load |

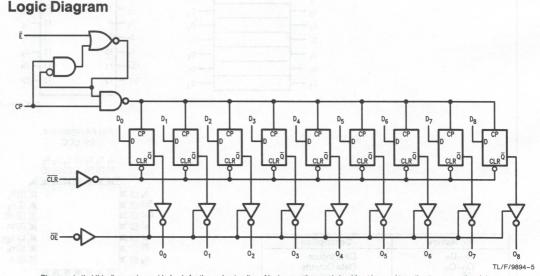
H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Z = High Impedance

= LOW-to-HIGH Transition
NC = No Change



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1) Recommended Operating

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | -,p | |
|--|-------------------|---------------------------|
| Supply Voltage (V _{CC}) | | -0.5V to 7.0V |
| DC Input Diode Current (I_{IK}) $V_I = -0.5V$ | | -20 mA |
| $V_I = V_{CC} + 0.5V$ | | + 20 mA |
| DC Input Voltage (V _I) | -0.5V | to V _{CC} + 0.5V |
| DC Output Diode Current (I_{OK}) $V_{O} = -0.5V$ | | -20 mA |
| $V_O = V_{CC} + 0.5V$ | | + 20 mA |
| DC Output Voltage (VO) | -0.5V | to V _{CC} + 0.5V |
| DC Output Source or Sink Current | (l _O) | ±50 mA |
| DC V _{CC} or Ground Current per Output Pin (I _{CC} or I _{GND}) | | ±50 mA |
| | | |
| Storage Temperature (T _{STG}) | -6 | 5°C to +150°C |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

Recommended Operating Conditions

| Supply Voltage (V _{CC}) | | |
|--|-----------------------------------|--|
| 'AC | 2.0V to 6.0V | |
| 'ACT | 4.5V to 5.5V | |
| Input Voltage (V _I) | 0V to V _{CC} | |
| Output Voltage (V _O) | 0V to V _{CC} | |
| Operating Temperature (TA) | | |
| 74AC/ACT 54AC/ACT | -40°C to +85°C -55°C to +125°C | |
| Junction Temperature (T _J) | | |
| CDIP | 0 or 0 175°C | |
| PDIP | 140°C | |
| Input Rise and Fall Time (t _r , | t _f) O or FLIO | |
| (Note 2) (Typical) (Except Schmitt Inputs) 'A | AC Devices | |
| V _{IN} from 30% to 70% of | | |
| V _{CC} @ 3.0V | 150 ns/V | |
| V _{CC} @ 4.5V | 40 ns/V | |
| V _{CC} @ 5.5V | 25 ns/V | |
| Input Rise and Fall Time (tr, | t _f) | |
| (Note 2) (Typical) | | |
| (Except Schmitt Inputs) 'A | CT Devices | |
| V_{IN} from 0.8V to 2.0V, V_{m} | neas from 0.8V to 2.0V | |
| V _{CC} @ 4.5V | 10 ns/V | |
| V _{CC} @ 5.5V | 8 ns/V | |
| | | |

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Electrical Characteristics

| 34 | CL = 50 pF Units | 908 | 74/ | ACT | 54ACT | 74ACT | 000357 | 19th Act |
|------------------|--|------------------------|------------------|-------------------|-----------------------------------|---------------------------------|-------------------------------|---|
| Symbol | Parameter Parameter | V _{CC} (V) | T _A = | 25°C | T _A = -55°C to + 125°C | T _A = -40°C to +85°C | Units | Conditions |
| | 0.4 | Тур | | Guaranteed Limits | | | 000 | |
| VIH | Minimum High Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 2.0 | 2.0 2.0 | 2.0 2.0 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ |
| VIL | Maximum Low Level Input Voltage | 4.5 4.5 | 1.5 1.5 | 0.8 | 0.8 0.8 | 0.8 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ |
| V _{OH} | Minimum High Level | 4.5 | 4.49 5.49 | 4.4 5.4 | 4.4 5.4 | 4.4 5.4 | ٧ | $I_{OUT} = -50 \mu\text{A}$ |
| | en a | 4.5 | | 3.86 4.86 | 3.70 4.70 | 3.76 4.76 | V ₁ V ₁ | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IOH} = -24 \text{ mA}$ $V_{IOH} = -24 \text{ mA}$ |
| V _{OL} | Maximum Low Level Output Voltage | 4.5 5.5 | 0.001 0.001 | 0.1 0.1 | 0.1 0.1 | 0.1 0.1 | ٧ | I _{OUT} = 50 μA |
| | | 4.5 5.5 | | 0.36 0.36 | 0.50 0.50 | 0.44 0.44 | V | $\begin{tabular}{ll} *V_{IN} &= V_{IL} \mbox{ or } V_{IH} \\ I_{OL} & 24 \mbox{ mA} \\ & 24 \mbox{ mA} \end{tabular}$ |
| I _{IN} | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | ±1.0 | μА | $V_{I} = V_{CC}$, GND |
| loz | Maximum TRI-STATE Current | 5.5 | | ±0.5 | ±10.0 | ±5.0 | μА | $V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}, GND$ |
| ICCT | Maximum I _{CC} /Input | 5.5 | 0.6 | 70 | 1.6 | 1.5 | mA | $V_I = V_{CC} - 2.1V$ |
| I _{OLD} | †Minimum Dynamic | 5.5 | | Bo | 50 | 75 | mA | V _{OLD} = 1.65V Max |
| IOHD | Output Current | 5.5 | | | -50 | -75 | mA | V _{OHD} = 3.85V Min |
| Icc | Maximum Quiescent Supply Current (Note 1) | 5.5 | | 8.0 | 160 | 80 | μΑ | V _{IN} = V _{CC} or GND |

^{*}All outputs loaded; thresholds on input associated with output under test.

[†]Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: I_{CC} limit for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

| | | | DIMONE | 74ACT | 2000 | 54/ | ACT | 74 | ACT | | Maria II |
|------------------|---------------------------------|-------------------|---|-------|------|--|------|--|------|----------|----------|
| Symbol Parameter | | V _{CC} * | T _A = +25°C C _L = 50pF | | | T _A = -55°C to + 125°C C _L = 50 pF | | T _A = -40°C to +85°C C _L = 50 pF | | Units | Fig. |
| | 9 | | Min | Тур | Max | Min | Max | Min | Max | Pan Pugi | |
| f _{max} | Maximum Clock Frequency | 5.0 | 120 | 158 | Acc | 95 | | 109 | Va.0 | MHz | 2-3 |
| t _{PLH} | Propagation Delay CP to On | 5.0 | 1.5 | 5.5 | 9.5 | 1.0 | 12.0 | 1.5 | 10.5 | ns | 2-6 |
| t _{PHL} | Propagation Delay CP to On | 5.0 | 2.0 | 5.5 | 9.5 | 1.0 | 12.0 | 1.5 | 10.5 | ns | 2-6 |
| t _{PHL} | Propagation Delay CLR to On | 5.0 | 2.5 | 8.0 | 13.5 | 1.0 | 18.0 | 2.0 | 15.5 | ns | 2-6 |
| t _{PZH} | Output Enable Time | 5.0 | 1.5 | 6.0 | 10.5 | 1.0 | 11.5 | 1.5 | 11.5 | ns | 2-7 |
| t _{PZL} | Output Enable Time | 5.0 | 2.0 | 6.5 | 11.0 | 1.0 | 12.0 | 1.5 | 12.0 | ns | 2-8 |
| t _{PHZ} | Output Disable Time OE to On | 5.0 | 1.5 | 6.5 | 11.0 | 1.0 | 13.5 | 1.5 | 12.0 | ns | 2-7 |
| t _{PLZ} | Output Disable Time OE to On | 5.0 | 1.5 | 6.0 | 10.5 | 1.0 | 12.0 | 1.5 | 11.5 | ns | 2-8 |

^{*}Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements: See Section 2 for Waveforms

| | times relies to the or course within the | handren a d | 744 | CT | 54ACT | 74ACT | | |
|-----------------------|--|-------------------|-----------------------------------|------|--|--|-------|-----------|
| Symbol | Parameter | V _{CC} * | T _A = C _L = | | T _A = -55°C to + 125°C C _L = 50 pF | T _A = -40°C to +85°C C _L = 50 pF | Units | Fig. |
| | and Laboratory 1 | | Тур | Park | Guaranteed Min | imum | | fearlers. |
| ts | Setup Time, HIGH or LOW D to CP | 5.0 | 0.5 | 2.5 | 4.0 | 2.5 | ns | 2-9 |
| t _h | Hold Time, HIGH or LOW D _n to CP | 5.0 | 0 | 2.5 | 3.0 | 2.5 | ns | 2-9 |
| t _s | Setup Time, HIGH or LOW EN to CP | 5.0 | 0 | 2.0 | 4.0 | 2.5 | ns | 2-9 |
| t _h Au Do- | Hold Time, HIGH or LOW EN to CP | 5.0 | 0 | 1.0 | 3.0 | 1.0 | ns | 2-9 |
| t _w | CP Pulse Width HIGH or LOW | 5.0 | 2.5 | 4.5 | 6.0 | 5.5 | ns | 2-6 |
| t _w | CLR Pulse Width, LOW | 5.0 | 3.0 | 5.5 | 7.0 | 5.5 | ns | 2-6 |
| t _{rec} | CLR to CP Recovery Time | 5.0 | 1.5 | 3.5 | 4.5 | 4.0 | ns | 2-9 |

^{*}Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

| Symbol | Parameter | AC/ACT | Units | Conditions |
|-----------------|----------------------------------|--------|--------|------------------------|
| Symbol | Parameter | Тур | Office | Conditions |
| C _{IN} | Input Capacitance | 4.5 | pF | $V_{CC} = 5.0V$ |
| C _{PD} | Power Dissipation Capacitance | 44 | pF | V _{CC} = 5.0V |

54AC/74AC825 • 54ACT/74ACT825 8-Bit D Flip-Flop

General Description

The 'ACT825 is an 8-bit buffered register. They have Clock Enable and Clear features which are ideal for parity bus interfacing in high performance microprogramming systems. Also included are multiple enables that allow multi-use control of the interface. The 'ACT825 has noninverting outputs and is fully compatible with AMD's Am29825.

Features

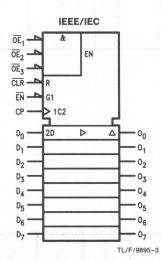
- Outputs source/sink 24 mA
- Inputs and outputs are on opposite sides
- 'ACT825 has TTL-compatible inputs

The information for the 'AC825 is Advanced Information only.

Ordering Code: See Section 5

Logic Symbols

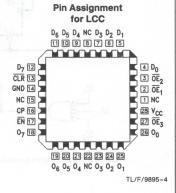
OE₁ D₀ D₁ D₂ D₃ D₄ D₅ D₆ D₇ OE₂ OE₃ CLR CP EN O₀ O₁ O₂ O₃ O₄ O₅ O₆ O₇ TL/F/9895-1





Connection Diagrams

| Pin Names | Description | | | |
|---|----------------|--|--|--|
| D ₀ -D ₇ | Data Inputs | | | |
| 00-07 | Data Outputs | | | |
| \overline{OE}_1 , \overline{OE}_2 , \overline{OE}_3 | Output Enables | | | |
| EN | Clock Enable | | | |
| CLR | Clear | | | |
| CP | Clock Input | | | |



Functional Description

The 'AC/'ACT825 consists of eight D-type edge-triggered flip-flops. These devices have TRI-STATE® outputs for bus systems, organized in a broadside pinning. In addition to the clock and output enable pins, the buffered clock (CP) and buffered Output Enable ($\overline{\text{OE}}$) are common to all flip-flops. The flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH CP transition. With $\overline{\text{OE}}_1$, $\overline{\text{OE}}_2$ and $\overline{\text{OE}}_3$ LOW, the contents of the flip-flops are available at the outputs. When one of $\overline{\text{OE}}_1$, $\overline{\text{OE}}_2$ or $\overline{\text{OE}}_3$ is HIGH, the outputs go to the high impedance state.

Operation of the $\overline{\text{OE}}$ input does not affect the state of the flip-flops. The 'AC/'ACT825 has Clear ($\overline{\text{CLR}}$) and Clock Enable ($\overline{\text{EN}}$) pins. These pins are ideal for parity bus interfacing in high performance systems.

When $\overline{\text{CLR}}$ is LOW and $\overline{\text{OE}}$ is LOW, the outputs are LOW. When $\overline{\text{CLR}}$ is HIGH, data can be entered into the flip-flops. When $\overline{\text{EN}}$ is LOW, data on the inputs is transferred to the outputs on the LOW-to-HIGH clock transition. When $\overline{\text{EN}}$ is HIGH, the outputs do not change state, regardless of the data or clock input transitions.

Function Table

| | | Inputs | | | Internal | Output | Function |
|------|-----|----------------|---|----|-----------------|-------------|----------|
| ŌĒ | CLR | CLR EN CP Dn Q | | Q | 0 | TO A MAN ON | |
| Н | X | L | _ | L | tace no Laments | Z na si | High-Z |
| Н | X | L | _ | Н | Н | Z | High-Z |
| Н | L | Χ | X | X | L | Z | Clear |
| L | L | X | X | X | L | L 3 non | Clear |
| Н | Н | Н | Χ | X | NC | Z | Hold |
| L | Н | Н | X | X | NC | NC | Hold |
| Н | Н | L | _ | L | L | Z | Load |
| H | Н | and L | _ | Н. | Н | Z | Load |
| Logi | Н | and La | _ | L | L | L | Load |
| L | Н | L | _ | Н | Н | н | Load |

H = HIGH Voltage Level

L = LOW Voltage Level

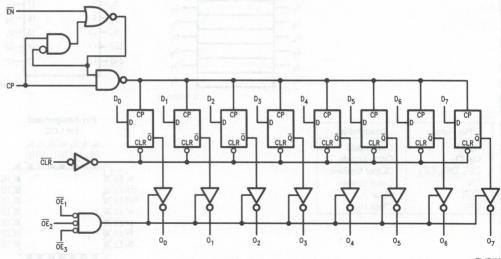
X = Immaterial

Z = High Impedance

= LOW-to-HIGH Transition

NC = No Change

Logic Diagram



TL/F/9895-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Office/Distributors for availability | and specifications. |
|---|------------------------------|
| Supply Voltage (V _{CC}) | -0.5V to 7.0V |
| DC Input Diode Current (I _{IK}) | |
| $V_I = -0.5V$ | -20 mA |
| $V_I = V_{CC} + 0.5V$ | + 20 mA |
| DC Input Voltage (V _I) | -0.5 V to $V_{CC} + 0.5$ V |
| DC Output Diode Current (IOK) | |
| $V_{O} = -0.5V$ | -20 mA |
| $V_O = V_{CC} + 0.5V$ | + 20 mA |
| DC Output Voltage (V _O) | -0.5 V to $V_{CC} + 0.5$ V |
| DC Output Source or Sink Current (IO) | ±50 mA |
| DC V _{CC} or Ground Current | |
| Per Output Pin (Icc or IGND) | ±50 mA |

Storage Temperature (T_{STG}) -65° C to $+150^{\circ}$ C Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

Recommended Operating Conditions

| Ooliditions | |
|---|-----------------------|
| Supply Voltage (V _{CC}) | |
| 'AC | 2.0V to 6.0V |
| 'ACT | 4.5V to 5.5V |
| Input Voltage (V _I) | 0V to V _{CC} |
| Output Voltage (V _O) | 0V to V _{CC} |
| Operating Temperature (T _A) | |
| 74AC/ACT | -40°C to +85°C |
| 54AC/ACT | -55°C to +125°C |
| Junction Temperature (T _J) | |
| CDIP | 175°C |
| PDIP | 140°C |
| Input Rise and Fall Time (tr, tf) | |
| (Note 2) (Typical) | |
| (Except Schmitt Inputs) 'AC Devices | |
| V _{IN} from 30% to 70%, V _{CC} | |
| V _{CC} @ 3.0V | 150 ns/V |
| V _{CC} @ 4.5V | 40 ns/V |
| V _{CC} @ 5.5V | 25 ns/V |
| Input Rise and Fall Time (t _r , t _f) | |
| (Note 2) (Typical) | |
| (Except Schmitt Inputs) 'ACT Devices | |
| V _{IN} from 0.8V to 2.0V, V _{meas} | |
| from 0.8V to 2.0V | |
| V _{CC} @ 4.5V | 10 ns/V |
| V _{CC} @ 5.5V | 8 ns/V |

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Electrical Characteristics

| | runs x rus | | 74ACT | | 54ACT | 74ACT | | | |
|------------------|--|--|------------------|----------------------------------|--------------|---------------------------------|---------|--|--|
| Symbol | Parameter | | T _A = | T _A = -55°C to + 125° | | T _A = -40°C to +85°C | Units | Conditions | |
| | arranesing M. By | (V) 1A 25 0 -55°C to +125°C -40°C to +85°C Typ Guaranteed Limits | | | | | | | |
| V _{IH} | Minimum High Level Input Voltage | | 1.5 1.5 | 2.0 2.0 | 2.0 2.0 | 2.0 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{IL} | Maximum Low Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 0.8 | 0.8 0.8 | 0.8 0.8 | ri ,emi | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{OH} | Minimum High Level | 4.5 5.5 | 4.49 5.49 | 4.4 5.4 | 4.4 5.4 | 4.4 5.4 | V | $I_{OUT} = -50 \mu\text{A}$ | |
| 8-5 | an 0.1 | 4.5 5.5 | | 3.86 4.86 | 3.70 4.70 | 3.76 4.76 | V | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IOH} = -24 \text{ mA}$ $V_{IOH} = -24 \text{ mA}$ | |
| V _{OL} | Maximum Low Level Output Voltage | 4.5 5.5 | 0.001 0.001 | 0.1 0.1 | 0.1 0.1 | 0.1 0.1 | V | I _{OUT} = 50 μA | |
| | 8n 83 | 4.5 5.5 | | 0.36 0.36 | 0.50 0.50 | 0.44 0.44 | V | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = 24 \text{ mA}$ $V_{IOL} = 24 \text{ mA}$ | |
| IIN | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | ±1.0 | μΑ | $V_I = V_{CC}$, GND | |
| loz | Maximum TRI-STATE Current | 5.5 | | ±0.5 | ± 10.0 | ±5.0 | μА | $V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}, GND$ | |
| ICCT | Maximum I _{CC} /Input | 5.5 | 0.6 | | 1.6 | 1.5 | mA | $V_I = V_{CC} - 2.1V$ | |
| I _{OLD} | †Minimum Dynamic | 5.5 | asti | w. | 50 | 75 | mA | V _{OLD} = 1.65V Max | |
| IOHD | Output Current | 5.5 | | | -50 | -75 | mA | V _{OHD} = 3.85V Min | |
| Icc | Maximum Quiescent (Note 1) Supply Current | 5.5 | | 8.0 | 160 | 80 | μΑ | $V_{IN} = V_{CC}$ or GND | |

^{*}All outputs loaded; thresholds on input associated with output under test.

[†]Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: I_{CC} limit for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

| | | | | 74ACT | ,000 | 54/ | ACT | 74/ | ACT | BRAY TELES | E ST | |
|------------------|---|--------------------------|-----|-----------------------|-------------|-----|--|-----|--|------------|--------------------------|------|
| Symbol | Parameter | V _{CC} * (V) | | A = +25° CL = 50 p | | to+ | T _A = -55°C to + 125°C C _L = 50 pF | | $T_A = -40^{\circ}C$ $to +85^{\circ}C$ $C_L = 50 pF$ | | Fig. No. 2-3 2-6 2-6 2-6 | Fig. |
| | 0 | | Min | Тур | Max | Min | Max | Min | Max | ¥8.0 | V | |
| f _{max} | Maximum Clock Frequency | 5.0 | 120 | 158 | Ami Väld | 95 | -0. 5 V | 109 | yd.y (V) ag | MHz | 2-3 | |
| t _{PLH} | Propagation Delay CP to O _n | 5.0 | 1.5 | 5.5 | 9.5 | 1.0 | 11.5 | 1.5 | 10.5 | ns | 2-6 | |
| t _{PHL} | Propagation Delay CP to On | 5.0 | 2.0 | 5.5 | 9.5 | 1.0 | 11.5 | 1.5 | 10.5 | ns | 2-6 | |
| t _{PHL} | Propagation Delay CLR to On | 5.0 | 2.5 | 8.0 | 13.5 | 1.0 | 18.0 | 2.0 | 15.5 | ns | 2-6 | |
| t _{PZH} | Output Enable Time | 5.0 | 1.5 | 6.0 | 10.5 | 1.0 | 11.5 | 1.5 | 11.5 | ns | 2-7 | |
| t _{PZL} | Output Enable Time | 5.0 | 2.0 | 6.5 | 11.0 | 1.0 | 12.5 | 1.5 | 12.0 | ns | 2-8 | |
| t _{PHZ} | Output Disable Time | 5.0 | 1.5 | 6.5 | 11.0 | 1.0 | 13.5 | 1.5 | 12.0 | ns | 2-7 | |
| t _{PLZ} | Output Disable Time | 5.0 | 1.5 | 6.0 | 10.5 | 1.0 | 13.0 | 1.5 | 11.5 | ns | 2-8 | |

^{*}Voltage Range 5.0 is 5.0V ± 0.5 V

AC Operating Requirements: See Section 2 for Waveforms

| | | | 744 | CT | 54ACT 74ACT | | to the | |
|-----------------------|---|----------|--|-----|---|------------|--------|-----|
| Symbol | | | +25°C = 50 pF T _A = -55°C to + 125°C C _L = 50 pF | | $T_A = -40^{\circ}C$ $to + 85^{\circ}C$ $C_L = 50 pF$ | Units | Fig. | |
| | | im I bee | Тур | | Guaranteed Min | imum | | |
| t _s | Setup Time, HIGH or LOW D _n to CP | 5.0 | 0.5 | 2.5 | 4.0 | 2.5 egai | ns | 2-9 |
| t _h | Hold Time, HIGH or LOW D _n to CP | 5.0 | 0 | 2.5 | 3.0 | 2.5 | ns | 2-9 |
| t _s | Setup Time, HIGH or LOW EN to CP | 5.0 | 0 | 2.0 | 4.0 | 2.5 | ns | 2-9 |
| th | Hold Time, HIGH or LOW EN to CP | 5.0 | 0 | 1.0 | 3.0 | 1.0 | ns | 2-9 |
| t _w Asroa | CP Pulse Width HIGH or LOW | 5.0 | 2.5 | 4.5 | 6.0 | 5.5 egazio | ns | 2-6 |
| t _w V o vV | CLR Pulse Width, LOW | 5.0 | 3.0 | 5.5 | 7.0 | 5.5 | ns | 2-6 |
| t _{rec} | CLR to CP Recovery Time | 5.0 | 1.5 | 3.5 | 4.5 | 4.0 | ns | 2-9 |

^{*}Voltage Range 5.0 is 5.0V \pm 0.5V

Capacitance

| Symbol | Parameter | AC/ACT | Units | Conditions | |
|-----------------|----------------------------------|--------|--------|------------------------|--|
| | raiametei | Тур | Office | | |
| CIN | Input Capacitance | 4.5 | pF | $V_{CC} = 5.0V$ | |
| C _{PD} | Power Dissipation Capacitance | 44 | pF | V _{CC} = 5.0V | |



54ACT/74ACT827 10-Bit Buffer/Line Driver with TRI-STATE® Outputs

General Description

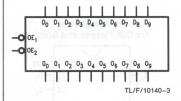
The 'ACT827 10-bit bus buffer provides high performance bus interface buffering for wide data/adress paths or buses carrying parity. The 10-bit buffers have NOR output enables for maximum control flexibility.

The 'ACT827 is functionally- and pin-compatible to AMD's AM29827.

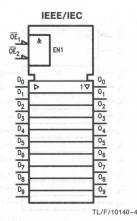
Features

- 'ACT827 has TTL-compatible inputs
- TRI-STATE® Outputs

Logic Symbols

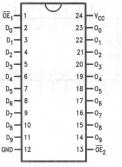


| Pin Names | Description |
|------------------------------------|---------------|
| $\overline{OE}_1, \overline{OE}_2$ | Output Enable |
| D ₀ -D ₇ | Data Inputs |
| 00-07 | Data Outputs |



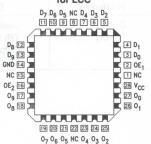
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/10140-1

Pin Assignment for LCC



TL/F/10140-2



54ACT/74ACT841 10-Bit Transparent Latch with TRI-STATE® Outputs

General Description

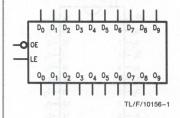
The 'ACT841 bus interface latch is designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity. The 'ACT841 is a 10-bit transparent latch, a 10-bit version of the 'ACT373.

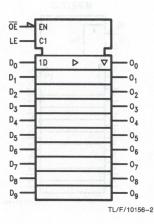
Features

- 'ACT841 has TTL-compatible inputs
- Outputs source/sink 24 mA
- Non-inverting TRI-STATE outputs

Ordering Code: See Section 5

Logic Symbols



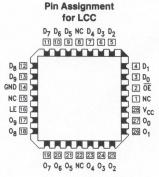


| Pin Names | Description |
|--------------------------------|-------------------|
| D ₀ -D ₉ | Data Inputs |
| 00-09 | TRI-STATE Outputs |
| ŌĒ | Output Enable |
| LE | Latch Enable |

Connection Diagrams



TL/F/10156-3



TL/F/10156-4

Functional Description

The ACT841 consists of ten D-type latches with TRI-STATE outputs. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. This allows asynchronous operation, as the output transition follows the data in transition.

On the LE HIGH-to-LOW transition, the data that meets the setup and hold time is latched. Data appears on the bus when the Output Enable (\overline{OE}) is LOW. When \overline{OE} is HIGH the bus output is in the high impedance state.

Function Table

| DO ALON SO | Inputs | | Inputs | | Internal | Output | Function |
|------------|--------|---|------------------|----------------|-------------|--------|----------|
| ŌĒ | O LE | D | Q | OA.O.O. | runction | | |
| X | X | Х | X | Z | High Z | | |
| Н | Н | L | (L) emissen | Z | High Z | | |
| Н | Н | Н | Н | Z | High Z | | |
| Н | L | X | NC | Z | Latched | | |
| L | Н | L | (4) SAME HERE DO | is early Indus | Transparent | | |
| L | H | Н | H STATE | Н | Transparent | | |
| L | L | X | NC | NC | Latched | | |

H = HIGH Voltage Level

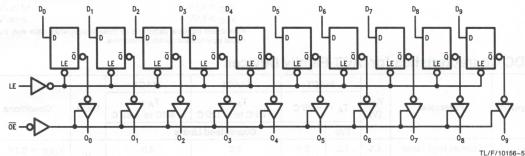
L = LOW Voltage Level

X = Immaterial

Z = High Impedance

NC = No Change

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate progagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Office/ Distributors for availab | omity and specimounions. |
|---|---------------------------------|
| Supply Voltage (V _{CC}) | -0.5V to $+7.0V$ |
| DC Input Diode Current (I _{IK}) | |
| $V_{I} = -0.5V$ | -20 mA |
| $V_I = V_{CC} + 0.5V$ | + 20 mA |
| DC Input Voltage (V _I) | $-0.5V$ to $V_{CC} + 0.5V$ |
| DC Output Diode Current (IOK) | |
| $V_0 = -0.5V$ | -20 mA |
| $V_O = V_{CC} + 0.5V$ | + 20 mA |
| DC Output Voltage (V _O) | -0.5 V to to $V_{CC} + 0.5$ V |
| DC Output Source | |
| or Sink Current (IO) | ±50 mA |
| DC V _{CC} or Ground Current | |
| per Output Pin (I _{CC} or I _{GND}) | ±50 mA |
| Storage Temperature (T _{STG}) | -65°C to +150°C |
| | |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

Recommended Operating Conditions

| Supply Voltage (V _{CC}) | outpate, i ne aparo. Leten Engine (LE) a |
|---|---|
| 'AC | 2.0V to 6.0V |
| 'ACT | 4.5V to 5.5V |
| Input Voltage (V _I) | 0V to V _{CC} |
| Output Voltage (V _O) | 0V to V _{CC} |
| Operating Temperature (T _A) | |
| 74AC/ACT | -40°C to +85°C |
| 54AC/ACT | -55°C to +125°C |
| Junction Temperature (T _{.I}) | |
| CDIP | 175°C |
| PDIP | 140°C |
| | 140 0 |
| Input Rise and Fall Time (t _r , t _f) | |
| (Note 2) (Typical) | |
| (Except Schmitt Inputs) 'AC Devices | |
| V _{IN} from 30% to 70% of V _{CC} | |
| V _{CC} @ 3.0V | 150 ns/V |
| V _{CC} @ 4.5V | 40 ns/V |
| V _{CC} @ 5.5V | 25 ns/V |
| Input Rise and Fall Time (t _r , t _f) | |
| (Note 2) (Typical) | |
| (Except Schmitt Inputs) 'ACT Devices | 3 |
| V _{IN} from 0.8V to 2.0V, V _{meas} | |
| illy | |

V_{CC} @ 5.5V Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

10 ns/V

8 ns/V

from 0.8V to 2.0V V_{CC} @ 4.5V

DC Characteristics for 'ACT Family Devices

| Symbol Parameter | Land make a series | le more a | 74 | ACT | 54ACT | 74ACT | | |
|------------------|--------------------------------------|------------------------|------------------|--------------|----------------------------------|---------------------------------|-------|---|
| | Parameter | V _{CC} (V) | T _A = | + 25°C | T _A = -55°C to +125°C | T _A = -40°C to +85°C | Units | Conditions |
| | | | Тур | alama Barana | Guaranteed Li | mits | | - m (Or 30 |
| V _{IH} | Minimum High Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 2.0 | 2.0 2.0 | 2.0 2.0 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ |
| V _{IL} | Maximum Low Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 0.8 0.8 | 0.8 0.8 | 0.8 0.8 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ |
| V _{OH} | Minimum High Level Output Voltage | 4.5 5.5 | 4.49 5.49 | 4.4 5.4 | 4.4 5.4 | 4.4 5.4 | ٧ | $I_{OUT} = -50 \mu$ A |
| | | 4.5 5.5 | | 3.86 4.86 | 3.70 4.70 | 3.76 4.76 | V | $V_{IN} = V_{IL} \text{ or } V_{I}$ -24 m -24 m |
| V _{OL} | Maximum Low Level Output Voltage | 4.5 5.5 | 0.001 0.001 | 0.1 0.1 | 0.1 0.1 | 0.1 0.1 | V | $I_{OUT} = 50 \mu A$ |
| | | 4.5 5.5 | | 0.36 0.36 | 0.50 0.50 | 0.44 0.44 | V | $V_{IN} = V_{IL} \text{ or } V_{I}$ $I_{OL} \qquad 24 \text{ m}$ 24 m |
| I _{IN} | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | ±1.0 | μА | $V_I = V_{CC}$, GND |
| loz | Maximum TRI-STATE Leakage Current | 5.5 | | ± 0.5 | ±10.0 | ±5.0 | μА | $V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}, GNE$ |
| ICCT | Maximum I _{CC} /Input | 5.5 | 0.6 | | 1.6 | 1.5 | μΑ | $V_{\rm I} = V_{\rm CC} - 2.1$ |

DC Characteristics for 'ACT Family Devices (Continued) Continued Continued

| Symbol | ZAACT | | 74ACT 54ACT VCC (V) TA = +25°C TA = -55°C to +125°C | | 54ACT | 74ACT | | | |
|------------------|-------------------------------------|-----|--|-------|----------------|-------|-------|------------------------------|--|
| | Parameter | | | | | | Units | Conditions | |
| | Fig 08 = 16 | | Тур | 30 17 | Guaranteed Lir | mits | | | |
| I _{OLD} | †Minimum Dynamic | 5.5 | bastqr | naue) | 50 | 75 | mA | V _{OLD} = 1.65V Max | |
| I _{OHD} | Output Current | 5.5 | 0.0 | | -50 | -75 | mA | V _{OHD} = 3.85V Min | |
| Icc | Maximum Quiescent Supply Current | 5.5 | | 8.0 | 160.0 | 80.0 | μА | $V_{IN} = V_{CC}$ or GND | |

^{*}All outputs loaded; thresholds on input associated with output under test.

AC Electrical Characteristics

| enoit | | noo | 74ACT | | 54ACT | | 74ACT | | 1043177 | | |
|------------------|---|-------------------|--|-----|---|-----|--|-----|---------|-------------|-----|
| Symbol | Parameter | V _{CC} * | T _A = +25°C C _L = 50 pF | | $T_A = -55^{\circ}C$ to + 125°C $C_L = 50 \text{ pF}$ | | $T_A = -40$ °C to $+85$ °C $C_L = 50 pF$ | | Units | Fig. No. | |
| | V0.8 = | opV . | Min | Тур | Max | Min | Max | Min | Max | (140 | |
| t _{PLH} | Propagation Delay D _n to O _n | 5.0 | 2.0 | 5.5 | 9.5 | 1.0 | 11.0 | 2.0 | 10.0 | ns | 2-5 |
| t _{PHL} | Propagation Delay D _n to O _n | 5.0 | 2.0 | 5.5 | 9.5 | 1.0 | 11.0 | 2.0 | 10.0 | ns | 2-5 |
| t _{PLH} | Propagation Delay LE to O _n | 5.0 | 2.0 | 5.5 | 9.0 | 1.0 | 11.0 | 2.0 | 10.0 | ns | 2-6 |
| t _{PHL} | Propagation Delay LE to O _n | 5.0 | 2.0 | 5.5 | 9.0 | 1.0 | 11.0 | 2.0 | 10.0 | ns | 2-6 |
| ^t PZH | Output Enable Time OE to On | 5.0 | 2.0 | 5.5 | 9.5 | 1.0 | 11.0 | 2.0 | 10.5 | ns | 2-7 |
| t _{PZL} | Output Enable Time OE to On | 5.0 | 2.0 | 5.5 | 9.5 | 1.0 | 11.0 | 2.0 | 10.5 | ns | 2-8 |
| t _{PHZ} | Output Disable Time OE to On | 5.0 | 2.0 | 6.0 | 10.5 | 1.0 | 12.0 | 2.0 | 11.0 | ns | 2-7 |
| t _{PLZ} | Output Disable Time OE to On | 5.0 | 2.0 | 6.0 | 10.5 | 1.0 | 12.0 | 2.0 | 11.0 | ns | 2-8 |

^{*}Voltage Range 5.0 is 5.0V ±0.5V

[†]Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Operating Requirements

| Symbol | 10.48 | | 744 | CT | 54ACT | 74ACT | | |
|----------------|---|--------------------------|--|-----|--|--|-------|-------------|
| | Parameter | V _{CC} * (V) | T _A = +25°C C _L = 50 pF | | $T_A = -55^{\circ}C$ $to + 125^{\circ}C$ $C_L = 50 pF$ | $T_A = -40^{\circ}C$ to $+85^{\circ}C$ $C_L = 50 pF$ | Units | Fig. No. |
| | ha a salver a service a salver | | Тур | | Guaranteed Mini | imum | ran A | |
| ts | Setup Time, HIGH or LOW D _n to LE | 5.0 | -0.5 | 0.5 | 3.0 | 1.0 | ns | 2-9 |
| t _h | Hold Time, HIGH or LOW D _n to LE | 5.0 | 0.5 | 2.0 | 2.0 | 2.0 | ns | 2-9 |
| t _w | LE Pluse Width, HIGH | 5.0 | 2.0 | 3.5 | 5.0 | 3.5 | ns | 2-6 |

^{*}Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

| Symbol | Parameter | AC/ACT | Units | Conditions |
|-----------------|----------------------------------|--------|-------|---------------------|
| | OM - AT | Тур | Onits | Conditions |
| CIN | Input Capacitance | 4.5 | pF | $V_{\rm CC} = 5.0V$ |
| C _{PD} | Power Dissipation Capacitance | 44 | pF | $V_{CC} = 5.0V$ |



54AC/74AC843 • 54ACT/74ACT843 8-Bit Transparent Latch

General Description

The 'AC/'ACT843 bus interface latch is designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths.

The 'AC/'ACT843 is functionally and pin compatible with AMD's Am29843.

Features

- 'ACT843 has TTL-compatible inputs
- TRI-STATE® outputs for bus interfacing

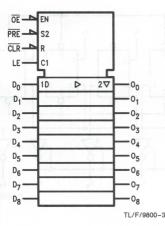
Ordering Code: See Section 5

Logic Symbols

OE DO D1 D2 D3 D4 D5 D6 D7 D8

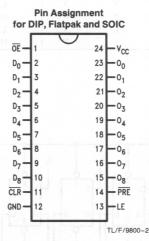
01 02 03 04 05

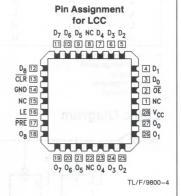
0₆ 0₇ 0₈



| Pin Names | Description | | | | |
|--------------------------------|---------------|--|--|--|--|
| D ₀ -D ₇ | Data Inputs | | | | |
| 00-07 | Data Outputs | | | | |
| ŌĒ | Output Enable | | | | |
| LE | Latch Enable | | | | |
| CLR | Clear | | | | |
| PRE | Preset | | | | |

Connection Diagrams





Functional Description

The 'AC/'ACT843 consists of nine D-type latches with TRI-STATE outputs. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. This allows asynchronous operation, as the output transition follows the data in transition. On the LE HIGH-to-LOW transition, the data that meets the setup times is latched. Data appears on the bus when the Output Enable $\overline{(OE)}$ is LOW. When \overline{OE} is HIGH, the bus output is in the high impedance state. In

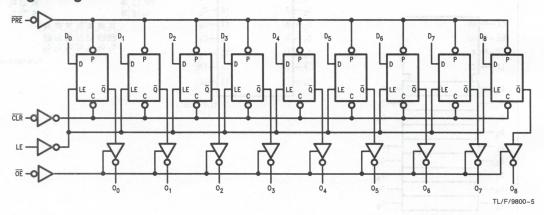
addition to the LE and $\overline{\text{OE}}$ pins, the 'AC/'ACT843 has a Clear ($\overline{\text{CLR}}$) pin and a Preset ($\overline{\text{PRE}}$) pin. These pins are ideal for parity bus interfacing in high performance systems. When $\overline{\text{CLR}}$ is LOW, the outputs are LOW if $\overline{\text{OE}}$ is LOW. When $\overline{\text{CLR}}$ is HIGH, data can be entered into the latch. When $\overline{\text{PRE}}$ is LOW, the outputs are HIGH if $\overline{\text{OE}}$ is LOW. Preset overrides $\overline{\text{CLR}}$.

Function Tables

| | TIDIE INDUS | | WATER FOR | | Internal | Outputs | Function | |
|---------|------------------|----------|-----------|---------|-----------------|---------------------|---------------------|--|
| CLR | PRE | ŌĒ | LE | D | a stab Quinte i | tata vi O for | antice solvent base | |
| Н | Н | Н | Н | Litting | siduagmes mg b | to vilent z and all | High Z | |
| Н | Н | Н | Н | Н | Н | Z | High Z | |
| Н | Н | Н | L | X | NC | Z | Latched | |
| Н | Н | L | Н | L | L en | book a Labori | Transparent | |
| Н | Н | L | Н | Н | Н | Н | Transparent | |
| Н | H | naidi mm | Walna | X | NC | NC | Latched | |
| Н | L | L | X | Χ | Н | н | Preset | |
| L | Н | L | X | X | L | L | Clear | |
| L insin | mgiang ni9 | L | X | X | Н | Н | Preset | |
| L | H | Н | of be pu | X | L L | Z | Clear/High Z | |
| Н | er an tan Egy ég | Н | L | X | Н | Z | Preset/High Z | |

- H = HIGH Voltage Level
- L = LOW Voltage Level
- X = Immaterial
- Z = High Impedance
- NC = No Change

Logic Diagram



Absolute Maximum Ratings (Note 1) Recommended Operating

If Military/Aerospace specified devices are required. please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| -0.5V to $+7.0V$ |
|------------------------------|
| |
| -20 mA |
| + 20 mA |
| -0.5 V to $V_{CC} + 0.5$ V |
| |
| -20 mA |
| + 20 mA |
| -0.5 V to $V_{CC} + 0.5$ V |
| |
| ±50 mA |
| |
| ±50 mA |
| -65°C to +150°C |
| |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

Conditions

| Supply Voltage (V _{CC}) | |
|--|-----------------------|
| 'AC | |
| 'ACT | 4.5V to 5.5V |
| Input Voltage (V _I) | 0V to V _{CC} |
| Output Voltage (V _O) | 0V to V _{CC} |
| Operating Temperature (T _A) | |
| 74AC/ACT | -40°C to +85°C |
| 54AC/ACT | -55°C to +125°C |
| Junction Temperature (T,J) | |
| CDIP | 175°C |
| PDIP | 140°C |
| Input Rise and Fall Time (t _r , t _f) | |
| (Note 2) (Typical) | |
| (Except Schmitt Inputs) 'AC Devices | |
| V _{IN} from 30% to 70% of V _{CC} | |
| V _{CC} @ 3.0V | 150 ns/V |
| V _{CC} @ 4.5V | 40 ns/V |
| V _{CC} @ 5.5V | 25 ns/V |
| Input Rise and Fall Time (t _r , t _f) | |
| (Note 2) (Typical) | |
| (Except Schmitt Inputs) 'ACT Devices | |
| V _{IN} from 0.8V to 2.0V, V _{meas} from 0.8V to 2.0V | |
| V _{CC} @ 4.5V | 10 ns/V |
| V _{CC} @ 5.5V | 8 ns/V |

Note 2: See Individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Electrical Characteristics for 'AC Family Devices

| | Tuo! V | 4.3 | 74 | AC | 54AC | 74AC | ou ngiH | ruminav i ingV |
|-----------------|--------------------------------------|------------------------|-------------------------|----------------------|--------------------------------------|---------------------------------|---------|--|
| Symbol | Parameter | V _{CC} (V) | T _A = | + 25°C | T _A = -55°C to + 125°C | T _A = -40°C to +85°C | Units | Conditions |
| | recol V | 187 | Тур | 0 | Guaranteed L | imits | | |
| VIH | Minimum High Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ |
| VIL | Maximum Low Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ |
| V _{OH} | Minimum High Level Output Voltage | 3.0 4.5 5.5 | 2.99 4.49 5.49 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | in V | $I_{OUT} = -50 \mu\text{A}$ |
| | 0V = V Am | 3.0 4.5 5.5 | | 2.56 3.86 4.86 | 2.4 3.7 4.7 | 2.46 3.76 4.76 | ٧ | $\label{eq:VIN} \begin{split} *V_{IN} &= V_{IL} or V_{IH} \\ &- 12 mA \\ I_{OH} &- 24 mA \\ &- 24 mA \end{split}$ |
| V _{OL} | Maximum Low Level Output Voltage | 3.0 4.5 5.5 | 0.002 0.001 0.001 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | ٧ | I _{OUT} = 50 μA |
| | 016 to | 3.0 4.5 5.5 | | 0.36 0.36 0.36 | 0.50 0.50 0.50 | 0.44 0.44 0.44 | V | $*V_{IN} = V_{IL} \text{ or } V_{IH}$ 12 mA I_{OL} 24 mA 24 mA |
| I _{IN} | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | ±1.0 | μΑ | $V_{I} = V_{CC}$, GND |

DC Electrical Characteristics for 'AC Family Devices (Continued)

| | | | 74 | AC | 54AC | 74AC | gs eng alf arti | georga vysomen o Teorga ovensko |
|------------------|--------------------------------------|---------------------|---|------------|----------------------------------|---------------------------------|--------------------|--|
| Symbol | Parameter | V _{CC} (V) | T _A = +25°C | | T _A = -55°C to +125°C | T _A = -40°C to +85°C | Units | Conditions |
| | /0 | | Тур | Jie v augi | Guaranteed L | imits | ad then | vO aborû runnî 00 |
| loz | Maximum TRI-STATE Leakage Current | 5.5 | Nage (V _C Temperati CT | ±0.5 | ±10.0 | ±5.0 | μА | V_{I} (OE) = V_{IL} , V_{IH} V_{I} = V_{CC} , GND V_{O} = V_{CC} , GND |
| I _{OLD} | †Minimum Dynamic | 5.5 | - 10 | MOAPE | 50 | 75 | mA | V _{OLD} = 1.65V Max |
| IOHD | Output Current | 5.5 | TS INC. THE | 9,00 | -50 | -75 | mA | V _{OHD} = 3.85V Min |
| Icc | Maximum Quiescent Supply Current | 5.5 | laR brita | 8.0 | 160.0 | 80.0 | μА | $V_{IN} = V_{CC}$ or GND |

^{*}All outputs loaded; thresholds on input associated with output under test.

Note: $I_{|N|}$ and $I_{|CC|}$ @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V $V_{|CC|}$. $I_{|CC|}$ for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Electrical Characteristics for 'ACT Family Devices

| | | | 744 | СТ | 54ACT | 74ACT | physic at | CAS to noticing briefly | |
|-----------------|--------------------------------------|------------------------|------------------|--------------|-----------------------------------|---------------------------------|-----------|---|--|
| Symbol | Parameter | V _{CC} (V) | T _A = | + 25°C | T _A = -55°C to + 125°C | T _A = -40°C to +85°C | Units | Conditions | |
| V\an 01 | | | Тур | A P coV | Guaranteed Li | mits | | | |
| V _{IH} | Minimum High Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 2.0 2.0 | 2.0 2.0 | 2.0 2.0 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{IL} | Maximum Low Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 0.8 0.8 | 0.8 0.8 | 0.8 0.8 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{OH} | Minimum High Level Output Voltage | 4.5 5.5 | 4.49 5.49 | 4.4 5.4 | 4.4 5.4 | 4.4 5.4 | ٧ | $I_{OUT} = -50 \mu\text{A}$ | |
| | ero Units Cons | 4.5 5.5 | ros — csiro, | 3.86 4.86 | 3.70 4.70 | 3.76 4.76 | V | $\label{eq:VIN} \begin{array}{ll} *V_{\text{IN}} = V_{\text{IL}} \text{or} V_{\text{IH}} \\ -24 \text{mA} \\ -24 \text{mA} \end{array}$ | |
| V _{OL} | Maximum Low Level Output Voltage | 4.5 5.5 | 0.001 0.001 | 0.1 0.1 | 0.1 0.1 | 0.1 0.1 | ٧ | I _{OUT} = 50 μA | |
| | =. 100V 50 V × Vcc | 4.5 5.5 | | 0.36 0.36 | 0.50 0.50 | 0.44 0.44 | V el | $\begin{tabular}{ll} *V_{IN} &= V_{IL} \text{ or } V_{IH} \\ I_{OL} & 24 \text{ mA} \\ 24 \text{ mA} \\ \end{tabular}$ | |
| I _{IN} | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 0.5 | 68.3 ±1.0 | μА | $V_I = V_{CC}$, GND | |
| loz | Maximum TRI-STATE Leakage Current | 5.5 | | ±0.5 | ±10.0 | ±5.0 | μА | $V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}, GND$ | |
| ГССТ | Maximum I _{CC} /Input | 5.5 | 0.6 | | 1.6 | 1.5 | mA | $V_{\rm I} = V_{\rm CC} - 2.1V$ | |
| IOLD | †Minimum Dynamic | 5.5 | | | 50 | 75 | mA | V _{OLD} = 1.65V Max | |
| IOHD | Output Current | 5.5 | | | -50 | -75 | mA | V _{OHD} = 3.85V Min | |
| Icc | Maximum Quiescent Supply Current | 5.5 | | 8.0 | 160.0 | 80.0 | μА | V _{IN} = V _{CC} or GND | |

^{*}All outputs loaded; thresholds on input associated with output under test.

Note: ICC for 54ACT @ 25°C is identical to 74ACT @ 25°C.

[†]Maximum test duration 2.0 ms, one output loaded at a time.

[†]Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics

| | 7480 | DAL | 8 | 74AC | | 54 | AC | 74/ | AC | | | |
|------------------|---|------------|--------------------------|--|--------------|------------|--------------|-------------------------|--|------|-------|------------|
| Symbol | Parameter | | V _{CC} * (V) | T _A = +25°C C _L = 50 pF | | | to + | −55°C 125°C 50 pF | T _A = to + C _L = | 85°C | Units | Fig No. |
| | 67916 | miniM bea | Min | Тур | Max | Min | Max | Min | Max | | | |
| t _{PLH} | Propagation Delay D _n to O _n | 3.3 5.0 | 3.5 2.0 | 6.5 4.5 | 12.0 8.5 | 1.0 1.0 | 14.0 10.0 | 2.5 1.5 | 13.0 9.0 | ns | 2- | |
| t _{PHL} | Propagation Delay D _n to O _n | 3.3 5.0 | 4.0 2.5 | 7.0 5.0 | 12.0 8.5 | 1.0 1.0 | 14.0 10.0 | 3.0 1.5 | 13.0 9.0 | ns | 2- | |
| t _{PLH} | Propagation Delay LE to O _n | 3.3 5.0 | 3.5 2.0 | 6.5 4.5 | 12.0 8.5 | 1.0 1.0 | 14.0 10.0 | 2.5 1.5 | 13.0 9.0 | ns | 2-0 | |
| t _{PHL} | Propagation Delay LE to On | 3.3 5.0 | 4.0 2.5 | 7.0 5.0 | 12.0 8.5 | 1.0 1.0 | 14.0 10.0 | 3.0 1.5 | 13.0 9.0 | ns | 2- | |
| t _{PLH} | Propagation Delay PRE to On | 3.3 5.0 | 5.5 3.5 | 8.5 6.0 | 19.0 13.0 | 1.0 1.0 | 23.5 16.0 | 4.5 2.5 | 21.5 14.5 | ns | 2- | |
| t _{PHL} | Propagation Delay CLR to On | 3.3 5.0 | 7.5 5.0 | 11.0 7.5 | 21.5 15.0 | 1.0 1.0 | 26.5 19.0 | 6.0 4.0 | 24.0 17.0 | ns | 2- | |
| ^t PZH | Output Enable Time OE to On | 3.3 5.0 | 3.5 2.0 | 6.0 4.5 | 11.0 8.0 | 1.0 1.0 | 13.0 10.0 | 3.0 1.5 | 12.0 9.0 | ns | 2- | |
| t _{PZL} | Output Enable Time OE to On | 3.3 5.0 | 4.0 2.0 | 6.5 5.0 | 11.0 8.0 | 1.0 1.0 | 13.0 10.0 | 2.5 1.5 | 12.0 9.0 | ns | 2- | |
| t _{PHZ} | Output Disable Time OE to On | 3.3 5.0 | 4.0 3.0 | 6.5 5.0 | 10.5 8.0 | 1.0 1.0 | 12.0 9.0 | 3.5 2.5 | 11.0 8.5 | ns | 2- | |
| t _{PLZ} | Output Disable Time OE to On | 3.3 5.0 | 3.0 2.0 | 6.0 4.5 | 10.5 8.0 | 1.0 1.0 | 12.0 9.0 | 2.5 1.5 | 11.0 8.5 | ns | 2- | |
| t _{PHL} | Propagation Delay PRE to On | 3.3 5.0 | 4.5 3.0 | 7.0 5.0 | 12.5 9.0 | 1.0 1.0 | 15.0 10.5 | 3.5 2.0 | 13.5 9.5 | ns | 2- | |
| t _{PLH} | Propagation Delay CLR to On | 3.3 5.0 | 4.5 3.0 | 7.0 5.0 | 12.5 9.0 | 1.0 1.0 | 15.0 10.5 | 3.5 2.0 | 13.5 9.5 | ns | 2- | |

^{*}Voltage Range 3.3 is 3.3V ± 0.3 V

^{*}Voltage Range 5.0 is 5.0V ± 0.5 V

AC Operating Requirements

| | 7480 | CARC | 7. | 4AC | 54AC | 74AC | | |
|------------------|---|-------------------|------------|-------------------|---|--|-------|------|
| Symbol | Parameter | V _{CC} * | | + 25°C = 50 pF | $T_A = -55^{\circ}C$ to + 125°C $C_L = 50 pF$ | $T_A = -40^{\circ}C$ to $+85^{\circ}C$ $C_L = 50 pF$ | Units | Fig. |
| | xaM ciM xak | 11186 | Тур | gyT | Guaranteed Minin | num | | |
| ts | Setup Time, HIGH or LOW D _n to LE | 3.3 5.0 | 0 -0.5 | 3.0 1.5 | 3.5 2.0 | 3.5 2.0 | ns | 2-9 |
| t _h | Hold Time, HIGH or LOW | 3.3 5.0 | -0.5 | 2.0 2.5 | 2.0 2.5 | 2.0 2.5 | ns | 2-9 |
| t _w | LE Pulse Width, HIGH | 3.3 5.0 | 1.5 1.5 | 3.0 3.0 | 3.5 3.0 | 3.0 | ns | 2-6 |
| t _w | PRE Pulse Width, LOW | 3.3 5.0 | 5.0 3.0 | 12.0 8.5 | 16.0 11.0 | 14.5 10.0 | ns | 2-6 |
| tw | CLR Pulse Width, LOW | 3.3 5.0 | 5.5 4.0 | 14.0 10.0 | 18.5 13.0 | 16.5 12.0 | ns | 2-6 |
| t _{rec} | PRE Recovery Time | 3.3 5.0 | 1.0 | 3.0 1.5 | 3.5 1.5 | 3.0 1.5 | ns | 2-9 |
| t _{rec} | CLR Recovery Time | 3.3 5.0 | 0 -0.5 | 1.5 0.5 | 2.5 | 0.5 | ns | 2-9 |

^{*}Voltage Range 3.3 is 3.3V ±0.3V

^{*}Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics

| | | unitike n.O. | | 74ACT | TOAY | 54/ | ACT | 74A | СТ | ledan | 23 |
|------------------|---|-------------------|-----|-------|------|--|------|--|------|-------|------|
| Symbol Parameter | Parameter | V _{CC} * | | | | $T_A = -55^{\circ}C$ $to + 125^{\circ}C$ $C_L = 50 pF$ | | $T_A = -40^{\circ}C$ $to +85^{\circ}C$ $C_L = 50 pF$ | | Units | Fig. |
| | - V | 1.d = 00V | Min | Тур | Max | Min | Max | Min | Max | G* | |
| ^t PLH | Propagation Delay D _n to O _n | 5.0 | 2.5 | 5.5 | 9.5 | 1.0 | 11.0 | 2.0 | 10.0 | ns | 2-5 |
| t _{PHL} | Propagation Delay D _n to O _n | 5.0 | 2.5 | 5.5 | 9.5 | 1.0 | 11.0 | 2.0 | 10.0 | ns | 2-5 |
| t _{PLH} | Propagation Delay LE to O _n | 5.0 | 2.5 | 5.5 | 9.0 | 1.0 | 11.0 | 2.0 | 10.0 | ns | 2-6 |
| t _{PHL} | Propagation Delay LE to O _n | 5.0 | 2.5 | 5.5 | 9.0 | 1.0 | 11.0 | 2.0 | 10.0 | ns | 2-6 |
| t _{PLH} | Propagation Delay PRE to On | 5.0 | 2.5 | 6.5 | 14.0 | 1.0 | 17.5 | 2.0 | 16.0 | ns | 2-6 |
| t _{PHL} | Propagation Delay CLR to On | 5.0 | 2.5 | 7.5 | 15.5 | 1.0 | 19.0 | 2.0 | 17.5 | ns | 2-6 |
| t _{PZH} | Output Enable Time | 5.0 | 2.5 | 5.5 | 9.5 | 1.0 | 11.0 | 2.0 | 10.5 | ns | 2-7 |
| t _{PZL} | Output Enable Time OE to On | 5.0 | 2.5 | 5.5 | 9.5 | 1.0 | 11.0 | 2.0 | 10.5 | ns | 2-8 |
| t _{PHZ} | Output Disable Time OE to On | 5.0 | 2.5 | 6.0 | 10.5 | 1.0 | 12.0 | 2.0 | 11.0 | ns | 2-7 |
| t _{PLZ} | Output Disable Time OE to On | 5.0 | 2.5 | 6.0 | 10.5 | 1.0 | 12.0 | 2.0 | 11.0 | ns | 2-8 |
| t _{PHL} | Propagation Delay PRE to On | 5.0 | 2.5 | 6.0 | 10.5 | 1.0 | 12.5 | 2.0 | 11.0 | ns | 2-6 |
| t _{PLH} | Propagation Delay CLR to On | 5.0 | 2.5 | 5.5 | 9.5 | 1.0 | 11.5 | 2.0 | 10.5 | ns | 2-6 |

^{*}Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

| | | | 7 | 4ACT | 54ACT | 74ACT | | |
|------------------|---|-------------------|------------------------|--------------------|---|--|-------|------|
| Symbol | Parameter | V _{CC} * | | = +25°C = 50 pF | $T_A = -55^{\circ}C$ to + 125°C $C_L = 50 pF$ | $T_{A} = -40^{\circ} C$ to $+85^{\circ} C$ $C_{L} = 50 \text{ pF}$ | Units | Fig. |
| | | | Typ Guaranteed Minimum | | | | | |
| t _s | Setup Time, HIGH or LOW D _n to LE | 5.0 | -0.5 | 0.5 | 1.0 | 1.0 | ns | 2-9 |
| t _h | Hold Time, HIGH or LOW D _n to LE | 5.0 | 0.5 | 2.0 | 2.0 | 2.0 | ns | 2-9 |
| t _w | LE Pulse Width, HIGH | 5.0 | 2.0 | 3.5 | 3.5 | 3.5 | ns | 2-6 |
| t _w | PRE Pulse Width, LOW | 5.0 | 5.0 | 8.5 | 11.0 | 10.0 | ns | 2-6 |
| t _w | CLR Pulse Width, LOW | 5.0 | 5.5 | 9.5 | 12.5 | 11.0 | ns | 2-6 |
| t _{rec} | PRE Recovery Time | 5.0 | 0.5 | 2.0 | 2.0 | 2.0 | ns | 2-9 |
| t _{rec} | CLR Recovery Time | 5.0 | -0.5 | 1.0 | 1.0 | 1.0 | ns | 2-9 |

^{*}Voltage Range 5.0 is 5.0V \pm 0.5V

Capacitance

| Symbol | Parameter | AC/ACT | Units | Conditions | |
|-----------------|----------------------------------|---------|-------|-----------------|--|
| | 0.48 = 41 0.48 | Тур | Oille | | |
| CIN | Input Capacitance | 4.5 | pF | $V_{CC} = 5.0V$ | |
| C _{PD} | Power Dissipation Capacitance | 44 x 14 | pF | $V_{CC} = 5.0V$ | |

MY.



54AC/74AC845 • 54ACT/74ACT845 8-Bit Transparent Latch with TRI-STATE® Outputs

General Description

Features

The 'AC/'ACT845 bus interface latch is designed to eliminate the extra packages required to buffer existing latches and provide easy expansion through multiple $\overline{\text{OE}}$ controls.

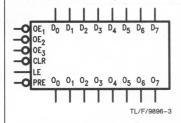
The 'AC/'ACT845 is functionally and pin compatible with AMD's Am29845.

■ 'ACT845 has TTL-compatible inputs

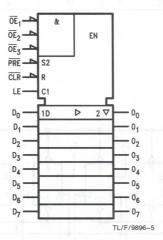
The information for the 'AC845 is Advanced Information only.

Ordering Code: See Section 5

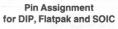
Logic Symbols

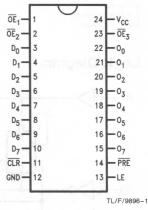


| Pin Names | Description |
|----------------------------------|----------------|
| D ₀ -D ₇ | Data Inputs |
| O ₀ -O ₇ | Data Outputs |
| OE ₁ -OE ₃ | Output Enables |
| LE | Latch Enable |
| CLR | Clear |
| PRE | Preset |

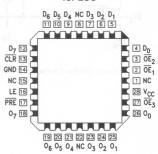


Connection Diagrams





Pin Assignment for LCC



TL/F/9896-2

Functional Description

The 'ACT845 consists of eight D latches with TRI-STATE outputs. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. This allows asynchronous operation as the output transition follows the data in transition.

On the LE HIGH-to-LOW transition, the data that meets the setup times is latched Data appears on the bus when the Output Enables $(\overline{OE}_1, \overline{OE}_2, \overline{OE}_3)$ are LOW. When any one of $\overline{OE}_1, \overline{OE}_2$ or \overline{OE}_3 is HIGH, the bus output is in the high impedance state.

Function Table

| | | Inputs | | | Internal | Output | Function |
|-----|-----|-----------------|----|--------|-------------|-------------|---------------|
| CLR | PRE | OE n | LE | D | Q | 0 | nollgin |
| Н | Н | H | Н | L CENT | -A E L mile | Z | High Z |
| Н | Н | Н | Н | Н | Н | Z | High Z |
| Н | Н | Н | L | X | NC | Z | Latched |
| H | Н | L | Н | L | L | ouscules ma | Transparent |
| Н | H | L | Н | Н | Н | Н | Transparent |
| Н | Н | L | L | X | NC | NC | Latched |
| Н | L | L | X | X | Н | Н | Preset |
| L | Н | L | X | X | L | L | Clear |
| L | L | L | X | X | Н | н | Preset |
| L | Н | Н | L | X | L | Z | Clear/High Z |
| Н | L | Н | L | X | Н | Z | Preset/High 2 |

H = HIGH Voltage Level

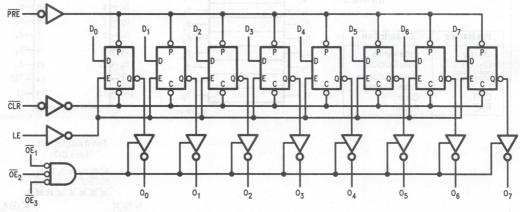
L = LOW Voltage Level

X = Immaterial

Z = High Impedance

NC = No Change

Logic Diagram



TL/F/9896-4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

10 ns/V

8 ns/V

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Office, Distributors to | avanabi | nty and op | ecincations. |
|------------------------------------|--|------------|------------------------|
| Supply Voltage (V _{CC}) | | t of _ | -0.5V to +7.0V |
| DC Input Diode Current | t (I _{IK}) | | |
| $V_{I} = -0.5V$ | | | -20 mA |
| $V_I = V_{CC} + 0.5V$ | | | + 20 mA |
| DC Input Voltage (V _I) | | -0.5 | V to $V_{CC} + 0.5V$ |
| DC Output Diode Curre | nt (I _{OK}) | | |
| $V_0 = -0.5V$ | | | -20 mA |
| $V_O = V_{CC} + 0.5V$ | | | + 20 mA |
| DC Output Valtage (V-) | and the second s | -0.51 | /to \/ +0 5\/ |

DC Output Voltage (V_O) -0.5V to V_{CC} +0.5V DC Output Source or Sink Current (I_O) ± 50 mA

DC V_{CC} or Ground Current

Per Output Pin (I_{CC} or I_{GND}) ±50 mA
Storage Temerature (T_{STG}) -65°C to +150°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (Vcc)

| 'AC | 2.0V to 6.0V |
|---|------------------------|
| 'ACT | 4.5V to 5.5V |
| Input Voltage (V _I) | 0V to V _{CC} |
| Output Voltage (VO) | 0V to V _{CC} |
| Operating Temperature (T _A) | |
| 74ACT | -40°C to +85°C |
| 54ACT | -55°C to +125°C |
| Junction Temperature (T _J) | |
| CDIP | 175°C |
| PDIP | 140°C |
| Input Rise and Fall Time | |
| (Note 2) (Typical) (Except Schmitt Inputs) (t _r , t _f) | leyt Propagation Delay |

V_{IN} from 0.8V to 2.0V, V_{meas} from 0.8V to 2.0V

V_{CC} @ 5.5V

Note 2: Individual data sheets for those devices which differ from the typical input rise and fall times noted here.

DC Electrical Characteristics for 'ACT Family Devices

| | | 74ACT T _A = 25°C | | 54ACT | 74ACT | | Tolde | Conditions | |
|------------------|--------------------------------------|-----------------------------|--------------|----------------------------------|---------------------------------|--------------|-----------------|--|--|
| Symbol | Parameter | | | T _A = -55°C to +125°C | T _A = -40°C to +85°C | Units (V) | v _{cc} | | |
| 5-5 | 1.8 an 0.11 | Тур | | Guaranteed Li | mits | . Banti | 81088 | Chiput Chiput D | |
| V _{IH} | Minimum High Level Input Voltage | 1.5 1.5 | 2.0 2.0 | 2.0 2.0 | 2.0 2.0 | V | 4.5 5.5 | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{IL} | Maximum Low Level Input Voltage | 1.5 1.5 | 0.8 0.8 | 0.8 0.8 | 0.8 | ٧ | 4.5 5.5 | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{OH} | Minimum High Level | 4.49 5.49 | 4.4 5.4 | 4.4 5.4 | 4.4 5.4 | ٧ | 4.5 5.5 | $I_{OUT} = -50 \mu\text{A}$ | |
| | 16.5 ns 5.4 | 0.8 | 3.86 4.86 | 3.70 4.70 | 3.76 4.76 | V | 4.5 5.5 | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IOH} = -24 \text{ mA}$ $V_{IOH} = -24 \text{ mA}$ | |
| V _{OL} | Maximum Low Level Output Voltage | 0.001 0.001 | 0.1 0.1 | 0.1 0.1 | 0.1 0.1 | ٧ | 4.5 5.5 | $I_{OUT} = 50 \mu A$ | |
| | | | 0.36 0.36 | 0.50 0.50 | 0.44 0.44 | ٧ | 4.5 5.5 | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ | |
| I _{IN} | Maximum Input Leakage Current | | ±0.1 | ±1.0 | ±1.0 | μА | 5.5 | $V_I = V_{CC}$, GND | |
| loz | Maximum TRI-STATE Leakage Current | | ±0.5 | ± 10.0 | ±5.0 | μА | 5.5 | $V_{I} = V_{IL}, V_{IH}$ $V_{O} = V_{CC}, GND$ | |
| Ісст | Maximum I _{CC} /Input | 0.6 | | 1.6 | 1.5 | mA | 5.5 | $V_I = V_{CC} - 2.1V$ | |
| lold | †Minimum Dynamic | | | 50 | 75 | mA | 5.5 | V _{OLD} = 1.65V Max | |
| I _{OHD} | Output Current | | | -50 | -75 | mA | 5.5 | V _{OHD} = 3.85V Min | |
| Icc | Maximum Quiescent Supply Current | | 8.0 | 160 | 80 | μΑ | 5.5 | V _{IN} = V _{CC} or Ground (Note 1) | |

^{*}All outputs loaded; thresholds on input associated with output under test.

Note 1: I_{CC} limit for 54ACT @ 25°C is identical to 74ACT @ 25°C.

[†]Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics: See Section 2 or Waveforms and Load Configurations

| | | | 74ACT | noo | 54/ | ACT | 74/ | ACT | 10801016 1011 1011 | ann ea | ifi 1. osales |
|------------------|---|--|-------|--|-------------------|--|-----|-------|-----------------------|-------------|------------------|
| Symbol | Parameter | T _A = +25°C C _L = 50 pF | | T _A = -55°C to + 125°C C _L = 50 pF | | T _A = -40°C to +85°C C _L = 50 pF | | Units | V _{CC} * | Fig. No. | |
| | 0 | Min | Тур | Max | Min | Max | Min | Max | V | a.o == | N. |
| t _{PLH} | Propagation Delay D _n to O _n | 2.0 | 5.5 | 9.5 | V3.0 | _{OO} V at V | 2.0 | 10.0 | ns | 5.0 | 2-5 |
| t _{PHL} | Propagation Delay D _n to O _n | 2.0 | 5.5 | 9.5 | Am 05 | | 2.0 | 10.0 | ns | 5.0 | 2-5 |
| t _{PLH} | Propagation Delay LE to O _n | 2.0 | 5.5 | 9.0 | VBLG Aun Gr | - 55V of Vi 7 | 2.0 | 10.0 | ns | 5.0 | 2-6 |
| t _{PHL} | Propagation Delay LE to O _n | 2.0 | 5.5 | 9.0 | Am 0 | | 2.0 | 10.0 | ns | 5.0 | 2-6 |
| t _{PLH} | Propagation Delay PRE to On | 2.0 | 6.5 | 14.0 | oceana localis | Holling bindy Jam od bindy | 2.0 | 16.0 | ns | 5.0 | 2-6 |
| t _{PHL} | Propagation Delay CLR to On | 2.0 | 7.5 | 15.5 | on dealers | yon area fan enclassifings | 2.0 | 17.5 | ns | 5.0 | 2-6 |
| ^t PZH | Output Enable Time OE to On | 2.0 | 5.5 | 9.5 | TOA | 101.00 | 2.0 | 10.5 | ns | 5.0 | 2-7 |
| t _{PZL} | Output Enable Time | 2.0 | 5.5 | 9.5 | CARS EAT | 0.8 | 2.0 | 10.5 | ns | 5.0 | 2-8 |
| t _{PHZ} | Output Disable Time OE to On | 2.0 | 6.0 | 10.5 | erego o c | 0.0 | 2.0 | 11.0 | ns | 5.0 | 2-7 |
| t _{PLZ} | Output Disable Time OE to On | 2.0 | 6.0 | 10.5 | 80 | 0.S 8.0 | 2.0 | 11.0 | ns | 5.0 | 2-8 |
| t _{PHL} | Propagation Delay PRE to On | 2.0 | 6.0 | 10.5 | 8.0 | 0.8 | 2.0 | 11.0 | ns | 5.0 | 2-6 |
| t _{PLH} | Propagation Delay CLR to On | 2.0 | 5.5 | 9.5 | 07.0 | 3.56 | 2.0 | 10.5 | ns | 5.0 | 2-0 |

^{*}Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements: See Section 2 for Waveforms

| | | 74ACT | | 54ACT | 74ACT | | | |
|------------------|---|--|------------------------|---|--|-------|-------------------|------|
| Symbol | Parameter | T _A = +25°C C _L = 50 pF | | $T_A = -55^{\circ}C$ to $+125^{\circ}C$ $C_L = 50 pF$ | T _A = -40°C to +85°C C _L = 50 pF | Units | V _{CC} * | Fig. |
| | | | Typ Guaranteed Minimum | | | | Pot | k at |
| ts | Setup Time, HIGH or LOW D _n to LE | -0.5 | 0.5 | | 1.0 | ns | 5.0 | 2-9 |
| t _h | Hold Time, HIGH or LOW | 0.5 | 2.0 | 16 bit paral- and digital signal con | 2.0 | ns | 5.0 | 2-9 |
| t _w | LE Pulse Width, HIGH | 2.0 | 3.5 | as beensyds | 3.5 | ns | 5.0 | 2-6 |
| tw | PRE Pulse Width, LOW | 5.0 | 8.5 | O(t) | 10.0 | ns | 5.0 | 2-6 |
| t _w | CLR Pulse Width, LOW | 5.5 | 9.5 | aceinent for the | 11.0 | ns | 5.0 | 2-6 |
| t _{rec} | PRE Recovery Time | 0.5 | 2.0 | all legic for such a special T | bash 2.0 Aliw s | ns | 5.0 | 2-9 |
| t _{rec} | CLR Recovery Time | 0 | 1.0 | - B° | 1.0 | ns | 5.0 | 2-9 |

^{*}Voltage Range 5.0 is 5.0V ± 0.5 V

Capacitance of the solid section of the solid secti

| Symbol | Parameter | 54/74ACT | Units | Conditions | |
|-----------------|-------------------------------|-------------------|------------|-----------------|--|
| | raiameter | ng CSE Typ CS 1 | tormos 23T | | |
| C _{IN} | Input Capacitance | 4.5 | W pF | $V_{CC} = 5.0V$ | |
| C _{PD} | Power Dissipation Capacitance | T and 3 44 TOA' m | pF | $V_{CC} = 5.0V$ | |



54ACT/74ACT1016 16 x 16 Parallel Multiplier

General Description

The 'ACT1016 is a high-speed, low power 16 x 16-bit parallel multiplier that is ideally suited for real-time digital signal processing applications. Fabricated using advanced FACT™ technology, the 'ACT1016 offers a very low power alternative and exceptional performance.

The 'ACT1016 is a pin and functional replacement for TRW's MPY016H; the 'ACT1016 operates from a single $V_{\rm CC}$ supply and is compatible with standard TTL logic levels

The architecture of the 'ACT1016 features one 16-bit port dedicated to the X input registers (controlled by CLKX), one 16-bit I/O port used for loading the Y input registers (controlled by CLKY) and for displaying the Least Significant Product (LSP), and one 16-bit output port multiplexed between displaying the Least Significant Product (LSP) and the Most Significant Product (MSP). The I/O port direction is controlled by \overline{OEL} and the output port TRI-STATE® control is controlled by \overline{OEP} . The result is registered if FT is LOW (controlled by CLKL for the LSP and CLKM for the MSP) and unregistered if FT is held HIGH.

Twos complement, unsigned magnitude and mixed mode multiplications are possible through the two's complement X

and Y mode controls, X_M and Y_M , respectively. These mode controls are registered, controlled by the input clocks CLKX and CLKY.

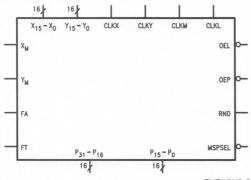
Result rounding is controlled by the registered RND signal (controlled by both CLKX and CLKY). Selection of one of the two rounding modes is determined by the FA signal.

Features

- 16 x 16 parallel multiplier
- Selectable rounding modes
- Twos complement, unsigned magnitude and mixed mode multiplication
- Pin and functionally compatible with TRW MPY016H
- Provides low voltage, high-speed operation
- Single V_{CC} supply
- ±2000V ESD protection
- Outputs source/sink 8 mA
- TRI-STATE outputs
- 'ACT1016 has TTL-compatible inputs

Ordering Code: See Section 5

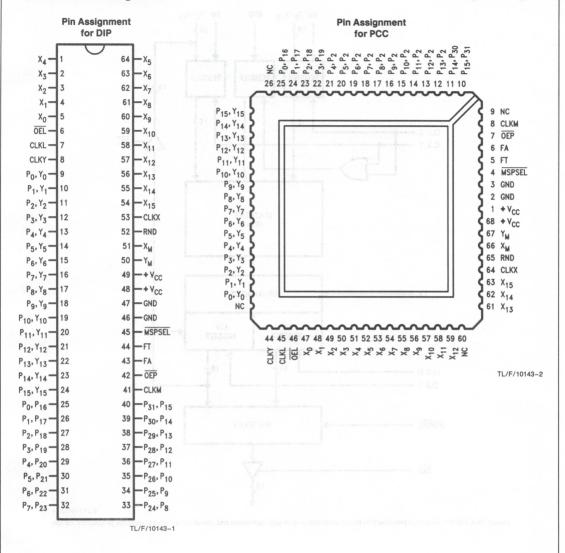
Logic Symbol



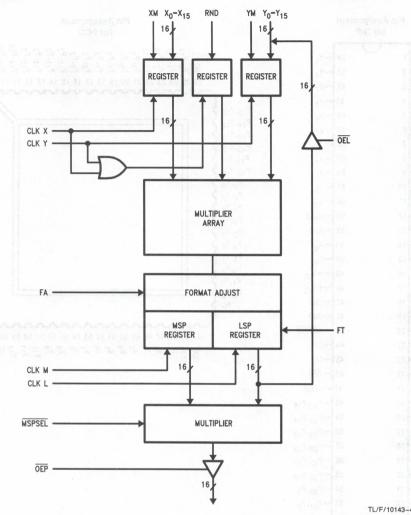
TL/F/10143-3

| Pin Names | Description |
|----------------------------------|-------------------------------|
| X ₁₅ -X ₀ | Multiplicand Data Inputs |
| Y ₁₅ -Y ₀ | Multiplier Data Inputs |
| CLKX, CLKY | Input Clocks |
| CLKM | Input Clock, MSP |
| CLKL | Input Clock, LSP |
| X _M , Y _M | Mode Control Inputs |
| FA | Format Adjust Control |
| FT | Format Transparent Control |
| OEL | TRI-STATE Enable, LSP Routing |
| OEP | TRI-STATE Enable, Product |
| | Output Port |
| RND | Round Control, MSP |
| MSPSEL | MSP Select |
| P ₃₁ -P ₁₆ | MSP Outputs |
| P ₁₅ -P ₀ | LSP Outputs |

Connection Diagrams



Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

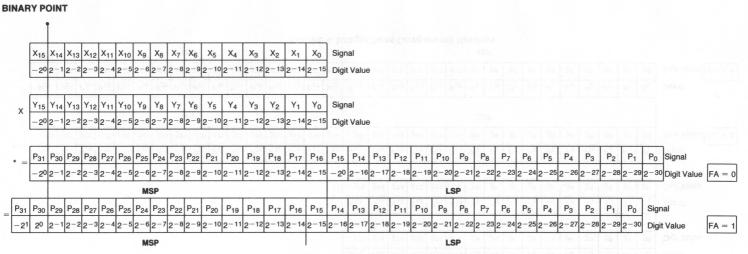


FIGURE 1. Fractional Twos Complement Notation

BINARY POINT

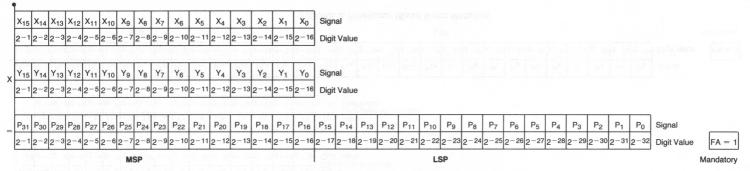


FIGURE 2. Fractional Unsigned Magnitude Notation

^{*}In this format an overflow occurs in the attempted multiplication of the two complement number 1000 ... 0 with 1000.00 yielding an erroneous product of -1 in the fraction case and -230 in the integer case.

4-316

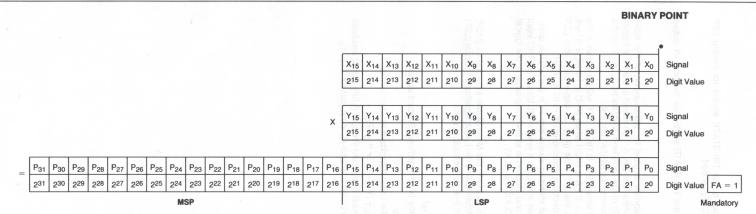


FIGURE 5. Integer Unsigned Magnitude Notation

BINARY POINT

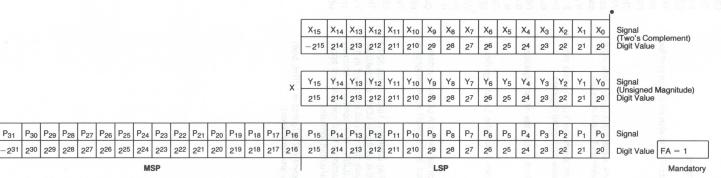


FIGURE 6. Integer Mixed Mode Notation

*In this format an overflow occurs in the attempted multiplication of the two's complement number 1000 . . . 0 with 1000.00 yielding an erroneous product of -1 in the fraction case and -230 in the integer case.

Signal Descriptions

Inputs

 $X_{IN}(X_{15}-X_0)$

Sixteen multiplicand data inputs.

YIN (Y15-Y0)

Sixteen multiplier data inputs. This is also an output port for $P_{15}-P_{0}$.

Input Clocks

CLKX

The rising edge of this clock loads the X_{15} - X_0 data input register along with the X mode and round registers.

CLKY

The rising edge of this clock loads the Y_{15} - Y_0 data input register along with the Y mode and round registers.

CLKM

The rising edge of this clock loads the Most Significant Product (MSP) register.

CLKI

The rising edge of this clock loads the Least Significant Product (LSP) register.

Controls

XM, YM

Mode control inputs for each data word. A LOW input designates an unsigned data input, and a HIGH input designates twos complement.

FA

When the Format Adjust (FA) Control is HIGH, a full 32-bit product is selected. When this control is LOW, a left-shifted 31-bit product is selected with the sign bit replicated in the Least Significant Product (LSP). This control is normally HIGH except for certain fractional twos complement applications (see multiplier input/output formats).

FT

When the Format Transparent (FT) Control is HIGH, both the MSP and LSP registers are transparent.

OEL

The $\overline{\text{OEL}}$ input is the TRI-STATE enable for routing LSP through YIN/LSPOUT port.

OEF

The $\overline{\text{OEP}}$ is the TRI-STATE enable for the product output port.

RND

The Round control is used for the rounding of the MSP. When this control is HIGH, A '1' is added to the Most Significant Bit (MSB) of the LSP. Note that this bit depends on the state of the format adjust (FA) control.

If FA is LOW when RND is HIGH, a '1' will be added to the 2^{-16} bit (P₁₄). If FA is HIGH when RND is HIGH, a '1' will be added to the 2^{-15} bit (P₁₅). In either case, the LSP output will reflect this addition when RND is HIGH.

Note also that rounding always occurs in the positive direction which may introduce a systematic bias. The RND input is registered and clocked in at the rising edge of the logical OR of both CLKX and CLKY.

MPSEL

When MPSEL is LOW, the Most Significant Product (MSP) is selected. When HIGH, the Least Significant Product (LSP) is available at the product output port.

Outputs

MSP (P31-P16)

The MSP is the Most Significant Product output.

LSP (P₁₅-P₀)

The LSP is the Least Significant Product output.

Y₁₅₋₀/LSP_{OUT} (Y₁₅-Y₀ or P₁₅-P₀)

This is the Least Significant Product (LSP) output available when \overline{OEL} is LOW. It is also an input port for $Y_{15}-Y_0$.

Absolute Maximum Ratings*

| Supply Voltage (V _{CC}) | -0.5V to +7.0V |
|--|---|
| DC Input Diode Current (I_{IK}) $V_I = 0.5$ | ≎ 88 - 67 9 - 20 mA |
| $V_1 = V_{CC} + 0.5$ | + 20 mA |
| DC Input Voltage (V _I) | $-0.5V$ to $V_{CC} + 0.5V$ |
| DC Output Diode Current (I _{OK}) V _O = 0.5V V _O = V _{CC} + 0.5V DC Input Voltage (V _O) DC Output Source or Sink | -20 mA +20 mA -0.5V to V _{CC} + 0.5V |
| Current; per Output Pin | ±15 mA |
| DC V _{CC} or Ground Current per Output Pin (I _{CC}) or (I _{GND}) | ±20 mA |
| Storage Temperature (T _{STG}) | -65°C to +150°C |
| | |

^{*}Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Recommended Operating Conditions

| Supply Voltage (V _{CC}) (Unless Otherwise Specified) | 4.5V to 5.5V |
|---|-----------------------------------|
| Input Voltage (V _I) | 0V to V _{CC} |
| Output Voltage (V _O) | 0V to V _{CC} |
| Operating Temperature (T _A) 74ACT 54ACT | -40°C to +85°C -55°C to +125°C |
| (except for Schmitt Inputs) | |
| V _{IN} | 0.8V to 2.0V |
| V _{CC} @ 4.5V | 0.8V to 2.0V 10 ns |
| Vcc @ 5.5V | 8 ns |

DC Characteristics over Operating Temperature Range (unless otherwise specified)

| Symbol | Parameter | 74ACT | | 74ACT Units | | Conditions |
|-------------------|----------------------------------|--------------|--------------|-------------|--------|---|
| Symbol | raidilletei | Тур | Guarant | eed Limit | Office | VOLING HOW MINING WAR AND THE |
| IN sed ess | Maximum Input Leakage Current | bereine | ±0.1 | ±1.0 | μА | $V_{CC} = Max, V_{IN} = V_{CC}, GND$ |
| loz | Maximum TRI-STATE Current | C S to digit | ±0.5 | ±5.0 | μΑ | High Z, V _{CC} = Max, V _{OUT} = V _{CC} , GND |
| Icca | Supply Current, Quiescent | 0.5 | 2.0 | 10.0 | mA | $V_{CC} = Max, V_{IN} = 0 V$ TSL, TSM, TSX = Max |
| ICCD | Supply Current, 12.4 MHz Loaded | 300 | | 325 | mA | V _{CC} = Max, f = 12.4 MHz Test Load: See Note 1 |
| ICCD | Supply Current, 20 MHz Loaded | 325 | | 350 | mA | V _{CC} = Max, f = 20 MHz Test Load: See Note 1 |
| V _{OH} * | Minimum HIGH Level Output | 4.49 | 4.4 | 4.4 | V | $V_{IN} = V_{IL}$ or V_{IH} , $I_{OUT} = -50 \mu A$, $V_{CC} = 4.5 V$ |
| | | 5.49 | 5.4 | 5.4 | | $V_{IN} = V_{IL}$ or V_{IH} , $I_{OUT} = -50 \mu A$, $V_{CC} = 5.5 V$ |
| | | La Samuelana | 3.86 | 3.76 | V | $I_{OH} = -8 \text{ mA}, V_{CC} = 4.5 \text{V}$ |
| | | | 4.86 | 4.76 | В | $I_{OH} = -8 \text{ mA}, V_{CC} = 5.5V$ |
| V _{OL} * | Maximum HIGH Level Output | 0.001 | 0.1 | 0.1 | V | $V_{IN} = V_{IL}$ or V_{IH} , $I_{OUT} = 50 \mu A$, $V_{CC} = 4.5 V$ |
| | | 0.001 | 0.1 | 0.1 | V | $V_{IN} = V_{IL}$ or V_{IH} , $I_{OUT} = 50 \mu A$, $V_{CC} = 5.5 V$ |
| | | V0 | 0.45 | 0.50 | V | $I_{OL} = 8 \text{ mA, } V_{CC} = 4.5 \text{V}$ |
| | NUF/10149-6 | a ed vam | 0.45 | 0.50 | В | $I_{OL} = 8 \text{ mA}, V_{CC} = 5.5 \text{V}$ |
| I _{OLD} | Minimum Dynamic Output Current | \$177 | T tright bri | 32 | mA | V _{CC} = 5.5V, V _{OLD} = 2.2V Max (Note 2) |
| I _{OHD} | Minimum Dynamic Output Current | | | -32 | mA | V _{CC} = 5.5V, V _{OHD} = 3.3V Min (Note 2) |
| Ісст | Maximum I _{CC} /Input | 0.6 | | 1.5 | mA | $V_{IN} = V_{CC} - 2.1V$ |

Note 1: Test Load 50 pF, 500Ω to Ground.

Note 2: Only one output loaded at one time, maximum duration of test 2 ms.

*All outputs loaded.

AC Characteristics

| | 有数的线 | 74ACT | | | (00)/81 | igenov viocina Sonostania | |
|--------------------|--|--------------------|-----------------------|-------|---------------|--------------------------------------|-------------------------------|
| | Parameter Samana Ca | Middec Reint II | T _A = -40° | Units | Fig. | | |
| Dov. of Vo | (V) sost | 101 | 6-65 | 101 | 6-55 | 0.0 | No. |
| oov or Vo | (_O V) epstlo | Min | Max | Min | Max | Ge (V _E) de Ourront I | atlov fugal 00 Januario oc |
| t _{MUC} | Unclocked Multiply Time | ESATEQQ CARS | 80.0 | | 65.0 | ns | 2-3, -9 |
| t _{MC} | Clocked Multiply Time | DANG | 65.0 | | 55.0 | ns | 2-3, -9, -10 |
| t _{PDSEL} | MSPSEL to Product Out | 1.5 | 13.0 | 1.5 | 13.0 | ns | 2-3, -9 |
| t _{PDP} | Output Clock to P | 1.5 | 20.0 | 1.5 | 20.0 | ns | 2-3, -9 |
| t _{PDY} | Output Clock to Y | 1.5 | 20.0 | 1.5 | 20.0 | ns | 2-3, -9 |
| t _{ENA} | TRI-STATE Enable Time (Note 2) | 1.5 | 10.0 | 1.5 | 10.0 | ns | 2-3, -8 |
| t _{DIS} | TRI-STATE Disable Time (Note 2) | 1.5 | 12.5 | 1.5 | 12.5 | ns | 2-3, -8 |
| ^t HCL | Clock LOW Hold Time CLKXY Relative to CLKML (Note 1) | 0 | 488 833 63 | 0 | a water ruse. | ns | 2-3, -9, -10 |
| ts | Setup Time X, Y, RND | 5.5 | 10 1 5110 | 5.5 | GVO.E. | ns | 2-3, -7, -9 |
| t _h | Hold Time X, Y, RND | 1.0 | 104 | 1.0 | jed: | ns | 2-3, -7, -9 |
| t _W | Clock Pulse Width HIGH or LOW | 3.5 | asinematic | 3.5 | | ns | 2-3, -9 |

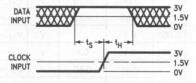
Note 1: To ensure that the correct product is entered in the output registers, new data may not be entered into the registers before the output registers have been clocked.

Note 2: Transition is measured to ±500 mV from steady state voltage with loading specified in Figure 2-3.

Capacitance

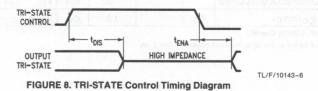
| Symbol Parameter | | Max | Units | Conditions | |
|------------------|--------------------|-----|-------|-----------------------|--|
| C _{IN} | Input Capacitance | 7.0 | pF | $V_{IN} = 0V$ | |
| C _{OUT} | Output Capacitance | 5.0 | pF | V _{OUT} = 0V | |

Timing Diagrams



Note: Diagram shown for HIGH data only. Output transition may be opposite sense.

FIGURE 7. Setup and Hold Time



TL/F/10143-5

Timing Diagrams (Continued)

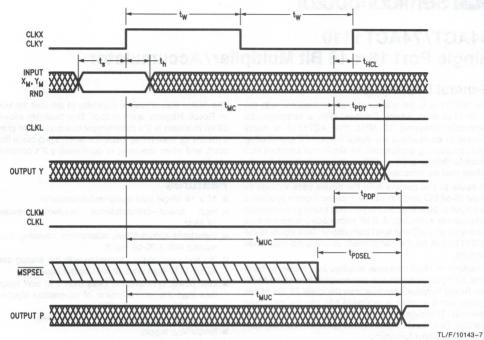


FIGURE 9. '1016 Timing Diagram

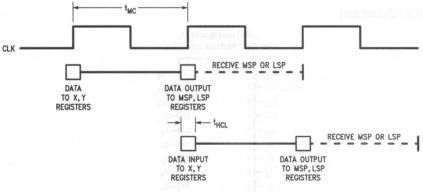


FIGURE 10. Simplified Timing Diagram—Typical Application

TL/F/10143-8

ADVANCE INFORMATION



54ACT/74ACT1110 Single Port 16 x 16 Bit Multiplier/Accumulator

General Description

The 'ACT1110 is pin and functionally compatible with the ADSP-1110 from Analog Devices. With a computational bandwidth exceeding 12 MHz, the 'ACT1110 is highly adapted to applications like digital filters, FFT's, and other signal processing applications. Its single bus structure also allows for the use of 28-pin DIP packages which significantly reduce cost as compared to existing 3-port multipliers.

All inputs to and outputs from the device pass through its single 16-bit I/O port. An internal pipeline register enables a new input to be loaded as the previous multiply/accumulate instruction is executed. A 6-bit microcoded word controls the device with I/O and MAC instructions. Data inputs to the 'ACT1110 can be 2's complement or unsigned magnitude numbers

A multiply or MAC operation requires two cycles to complete. Multiplier products are accumulated in a 40-bit Multiplier Result Register. Overflow from the lower 32 bits of this register into the upper 8 extended bits can be monitored externally. The outputs can be saturated to full scale upon overflow. Two round control inputs implement rounding consistent with output formatting.

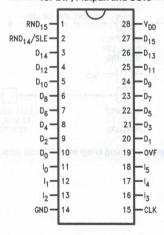
The device also offers the capability to left-shift the Multiplier Result Register upon output. This flexibility allows full 32-bit precision in 2's complement multiply. It also provides a means for maximizing resolution when using block floating point, and when upscaling or downscaling 2's complement results.

Features

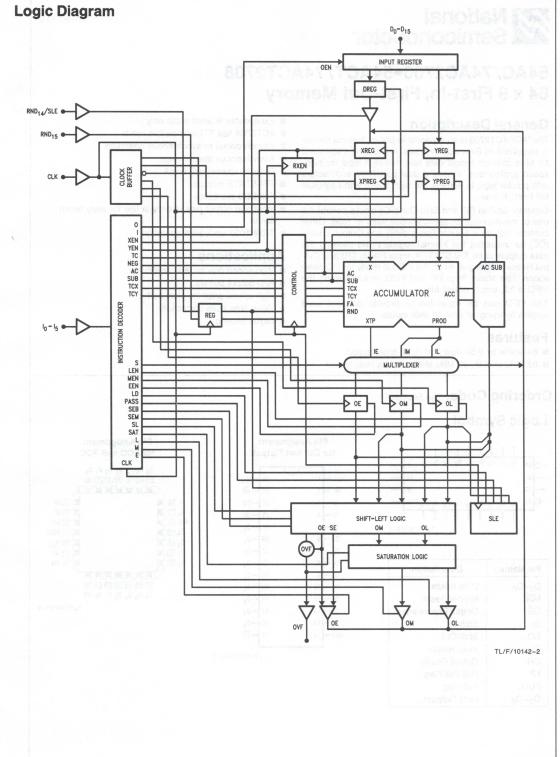
- 16 x 16 Single port multiplier/accumulator
- High speed—computational bandwidth exceeding 12 MHz
- Selectable accumulation, subtraction, rounding and preloading with a 35-bit result
- Pin and functionally compatible with the analog devices ADSP-1110 high drive (8 mA) output capability
- Low power consumption (less than 250 mW typical) less than 7% of the power of compatible bipolar and 14% of the power of NMOS designs
- Inputs and outputs directly TTL-compatible
- Single V_{CC} supply
- ±2000V ESD protection

Connection Diagram

Pin Assignment for DIP, Flatpak and SOIC



TL/F/10142-1





54AC/74AC2708 • 54ACT/74ACT2708 64 x 9 First-In, First-Out Memory

General Description

The 'AC/'ACT2708 is an expandable first-in, first-out memory organized as 64 words by 9 bits. An 85 MHz shift-in and 60 MHz shift-out typical data rate makes it ideal for highspeed applications. It uses a dual port RAM architecture with pointer logic to achieve the high speed with negligible fall-through time.

Separate Shift-In (SI) and Shift-Out (SO) clocks control the use of synchronous or asynchronous write or read. Other controls include a Master Reset (MR) and Output Enable (OE) for initializing the internal registers and allowing the data outputs to be TRI-STATE®. Input Ready (IR) and Output Ready (OR) signal when the FIFO is ready for I/O operations. The status flags HF and FULL indicate when the FIFO is full, empty or half full.

The FIFO can be expanded to provide different word lengths by trying off unused data inputs.

Features

- 64-words by 9-bit dual port RAM organization
- 85 MHz shift-in, 60 MHz shift-out data rate, typical

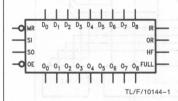
- Expandable in word width only
- ACT2708 has TTL-compatible inputs
- Asynchronous or synchronous operation
- Asynchronous master reset
- Outputs source/sink 8 mA
- TRI-STATE outputs
- Full ESD protection
- Input and output pins directly in line for easy board layout
- TRW 1030 work-alike operation

Applications

- High-speed disk or tape controllers
- A/D output buffers
- High-speed graphics pixel buffer
- Video time base correction
- Digital filtering

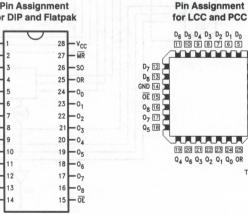
Ordering Code: See Section 5

Logic Symbol



| Pin Names | Description | | |
|--------------------------------|---------------------|--|--|
| D ₀ -D ₈ | Data Inputs | | |
| MR | Master Reset | | |
| ŌĒ | Output Enable Input | | |
| SI | Shift-In | | |
| SO | Shift-Out | | |
| IR | Input Ready | | |
| OR | Output Ready | | |
| HF | Half Full Flag | | |
| FULL | Full Flag | | |
| 00-08 | Data Outputs | | |





TL/F/10144-2

4 SI

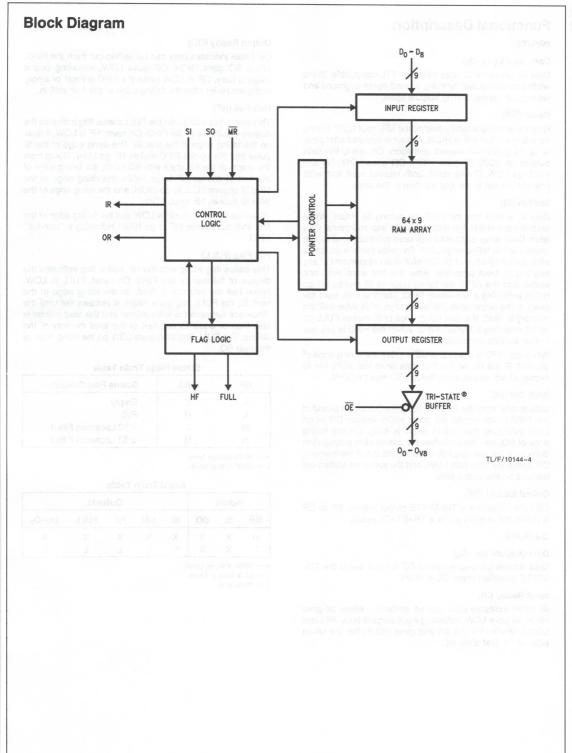
3 IR

2 HF

1 FULL 28 V_{CC} 27 MR 1 FULL

26 SO

TL/F/10144-3



Functional Description

NPUTS

Data Inputs (D₀-D₈)

Data inputs for 9-bit wide data are TTL-compatible. Word width can be reduced by trying unused inputs to ground and leaving the corresponding outputs open.

Reset (MR)

Reset is accomplished by pulsing the $\overline{\text{MR}}$ input LOW. During normal operation $\overline{\text{MR}}$ is HIGH. A reset is required after power up to guarantee correct operation. On reset, the data outputs go LOW, IR goes HIGH, OR goes LOW, FH and FULL go LOW. During reset, both internal read and write pointers are set to the first location in the array.

Shift-In (SI)

Data is written into the FIFO by pulsing SI HIGH. When Shift-In goes HIGH, the data is loaded into an internal data latch. Data setup and hold times need to be adhered to with respect to the falling edge of SI. The write cycle is complete after the falling edge of SI. The shift-in is independent of any ongoing shift-out operation. After the first word has been written into the FIFO, the falling edge of SI makes HF go HIGH, indicating a non-empty FIFO. The first data word appears at the output after the falling edge of SI. After half the memory is filled, the next rising edge of SI makes FULL go HIGH indicating a half-full FIFO. When the FIFO is full, any further shift-ins are disabled.

When the FIFO is empty and \overline{OE} is LOW, the falling edge of the first SI will cause the first data word just shifted-in to appear at the output, even though SO may be LOW.

Shift-Out (SO)

Data is read from the FIFO by the Shift-Out signal provided the FIFO is not empty. SO going HIGH causes OR to go LOW indicating that output stage is busy. On the falling edge of SO, new data reaches the output after propagation delay t_D. If the last data has been shifted-out of the memory, OR continues to remain LOW, and the last word shifted-out remains on the output pins.

Output Enable (OE)

OE LOW enables the TRI-STATE output buffers. When OE is HIGH, the outputs are in a TRI-STATE mode.

OUTPUTS

Data Outputs (O₀-O₈)

Data outputs are enabled when \overline{OE} is LOW and in the TRI-STATE condition when \overline{OE} is HIGH.

Input Ready (IR)

IR HIGH indicates data can be shifted-in. When SI goes HIGH, IR goes LOW, indicating input stage is busy. IR stays LOW when the FIFO is full and goes HIGH after the falling edge of the first shift-out.

Output Ready (OR)

OR HIGH indicates data can be shifted-out from the FIFO. When SO goes HIGH, OR goes LOW, indicating output stage is busy. OR is LOW when the FIFO is reset or empty and goes HIGH after the falling edge of the first shift-in.

Half-Full (HF)

This status flag along with the FULL status flag indicates the degree of fullness of the FIFO. On reset, HF is LOW; it rises on the falling edge of the first SI. The rising edge of the SI pulse that fills up the FIFO makes HF go LOW. Going from the empty to the full state with SO LOW, the falling edge of the first SI causes HF to go HIGH, the rising edge of the 33rd SI causes FULL to go HIGH, and the rising edge of the 64th SI causes HF to go LOW.

When the FIFO is full, HF is LOW and the falling edge of the first shift-out causes HF to go HIGH indicating a "non-full" FIFO.

Full Flag (FULL)

This status flag along with the HF status flag indicates the degree of fullness of the FIFO. On reset, FULL is LOW. When half the memory is filled, on the rising edge of the next SI, the FULL flag goes HIGH. It remains set until the difference between the write pointer and the read pointer is less than or equal to one-half of the total memory of the device. The FULL flag then goes LOW on the rising edge of the next SO.

Status Flags Truth Table

| Н | F FULL | Status Flag Condition | | |
|-----|---------|-----------------------|--|--|
| L | TINA SH | Empty | | |
| L | . н | Full | | |
| H | l L | <32 Locations Filled | | |
| н н | | ≥32 Locations Filled | | |

H = HIGH Voltage Level

L = LOW Voltage Level

Reset Truth Table

| Inputs | | | Outputs | | | | |
|--------|----|----|---------|----|----|------|-------|
| MR | SI | so | IR | OR | HF | FULL | 00-08 |
| Н | X | X | X | Х | X | X | X |
| L | X | X | Н | L | L | L | L |

H = HIGH Voltage Level

L = LOW Voltage Level

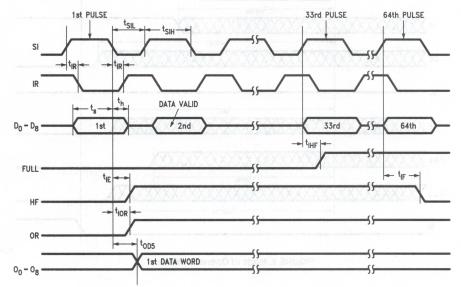
X = Immaterial

Functional Description (Continued)

MODES OF OPERATION

Mode 1: Shift in Sequence for FIFO Empty to Full Sequence of Operation

- Input Ready is initially HIGH; HF and FULL flags are LOW. The FIFO is empty and prepared for valid data. OR is LOW indicating that the FIFO is not yet ready to output data.
- 2. Shift-In is set HIGH, and data is loaded into the FIFO. Data has to be settled $t_{\rm S}$ before the falling edge of SI and held $t_{\rm h}$ after.
- Input Ready (IR) goes LOW propagation delay t_{IR} after SI goes HIGH: input stage is busy.
- 4. Shift-In is set LOW; IR goes HIGH indicating the FIFO is ready for additional data. Data just shifted-in arrives at output propagation delay t_{OD5} after SI falls. OR goes HIGH propagation delay t_{IOR} after SI goes LOW, indicating the FIFO has valid data on its outputs. HF goes HIGH propagation delay t_{IE} after SI falls, indicating the FIFO is no longer empty.
- 5. The process is repeated through the 64th data word. On the rising edge of the 33rd SI, FULL flag goes HIGH propagation delay t_{IHF} after SI, indicating a half-full FIFO. HF goes LOW propagation delay t_{IF} after the rising edge of the 64th pulse indicating that the FIFO is full. Any further shift-ins are disabled.



TL/F/10144-5

Note: SO and $\overline{\text{OE}}$ are LOW; $\overline{\text{MR}}$ is HIGH.

FIGURE 1. Modes of Operation Mode 1

Functional Description (Continued)

Mode 2: Master Reset

Sequence of Operation

- Input and Output Ready, HF and FULL can be in any state before the reset sequence with Master Reset (MR) HIGH.
- Master Reset goes LOW and clears the FIFO, setting up all essential internal states. Master Reset must be LOW pulse width t_{MRW} before rising again.
- 3. Master Reset rises.

- 4. IR rises (if not HIGH already) to indicate ready to write state recovery time t_{MRIRH} after the falling edge of MR. Both HF and FULL will go LOW indicating an empty FIFO, occurring recovery times t_{MRE} and t_{MRO} respectively after the falling edge of MR. OR falls recovery time t_{MRORL} after MR falls. Data at outputs goes LOW recovery time t_{MRONL} after MR goes LOW.
- Shift-In can be taken HIGH after a minimum recovery time t_{MRSIH} after MR goes HIGH.

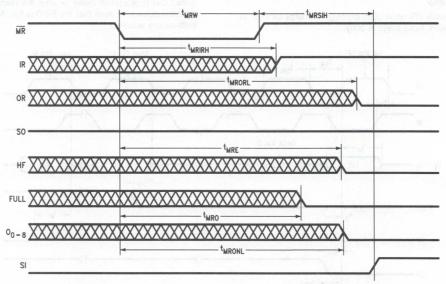


FIGURE 2. Mode of Operation Mode 2

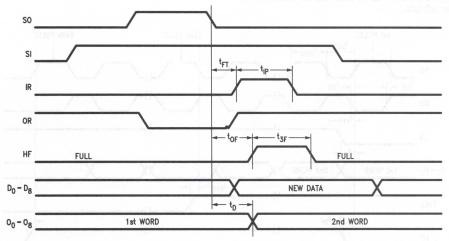
TL/F/10144-6

Functional Description (Continued)

Mode 3: With FIFO Full, Shift-In is Held HIGH in Anticipation of an Empty Location

Sequence of Operation

- The FIFO is initially full and Shift-In goes HIGH. OR is initially HIGH. Shift-Out is LOW. IR is LOW.
- Shift-Out is pulsed HIGH, Shift-Out pulse propagates and the first data word is latched on the rising edge of SO. OR falls on this edge. On the falling edge of SO, the second data word appears after propagation delay t_D. New data is written into the FIFO after SO goes LOW.
- Input Ready goes HIGH one fall-through time, t_{FT}, after the falling edge of SO. Also, HF goes HIGH one t_{OF} after SO falls, indicating that the FIFO is no longer full.
- IR returns LOW pulse width t_{IP} after rising and shifting new data in. Also, HF returns LOW pulse width t_{3F} after rising, indicating the FIFO is once more full.
- 5. Shift-In is brought LOW to complete the shift-in process and maintain normal operation



TL/F/10144-7

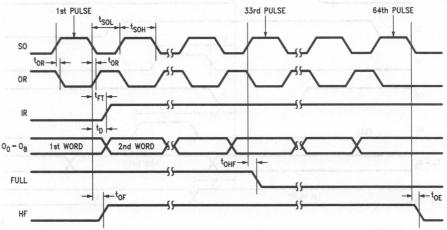
Note: MR and FULL are HIGH; OE is LOW.

FIGURE 3. Modes of Operation Mode 3

Functional Description (Continued)

Mode 4: Shift-Out Sequence, FIFO Full to Empty Sequence of Operation

- FIFO is initially full and OR is HIGH, indicating valid data is at the output. IR is LOW.
- 2. SO goes HIGH, resulting in OR going LOW one propagation delay, $t_{\rm OR}$, after SO rises. OR LOW indicates output stage is busy.
- SO goes LOW, new data reaches output one propagation delay, t_D, after SO falls; OR goes HIGH one propagation delay, t_{OR}, after SO falls and HF rises one propagation delay, t_{OF}, after SO falls. IR rises one fall-through time, t_{FT}, after SO falls.
- 4. Repeat process through the 64th SO pulse. FULL flag goes LOW one propagation delay, t_{OHF}, after the rising edge of 33rd SO, indicating that the FIFO is less than half full. On the falling edge of the 64th SO, HF goes LOW one propagation delay, t_{OE}, after SO, indicating the FIFO is empty. The SO pulse may rise and fall again with an attempt to unload an empty FIFO. This results in no change in the data on the outputs as the 64th word stays latched.



Note: SI and OE are LOW; MR is HIGH; D0-D8 are immaterial.

FIGURE 4. Modes of Operation Mode 4

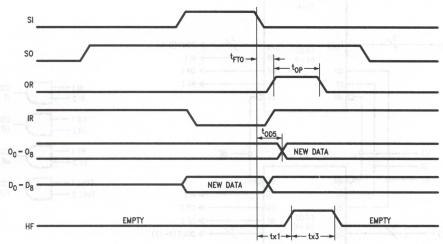
TL/F/10144-8

Functional Description (Continued)

Mode 5: With FIFO Empty, Shift-Out is Held HIGH in Anticipation of Data

Sequence of Operation

- 1. FIFO is initially empty; Shift-Out goes HIGH.
- Shift-In pulse loads data into the FIFO and IR falls. HF rises propagation delay t_{X1} after the falling edge of SI.
- 3. OR rises a fall-through time of $t_{\mbox{FTO}}$ after the falling edge of Shift-In, indicating that new data is ready to be output.
- Data arrives at output one propagation delay, t_{OD5}, after the falling edge of Shift-In.
- OR goes LOW pulse width t_{OP} after rising and HF goes LOW pulse width t_{X3} after rising, indicating that the FIFO is empty once more.
- 6. Shift-Out goes LOW, necessary to complete the Shift-Out process.



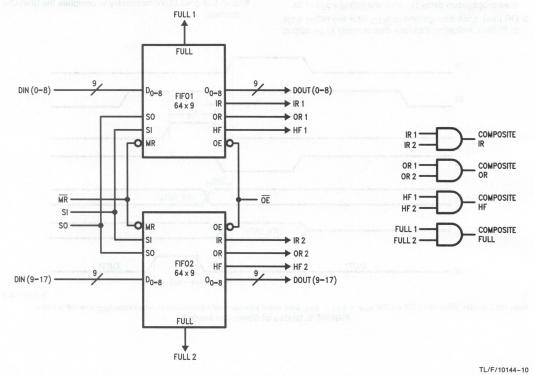
TL/F/10144-9

Note: FULL is LOW; $\overline{\text{MR}}$ is HIGH; $\overline{\text{OE}}$ is LOW; $t_{DOF} = t_{FTO} - t_{OD5}$. Data output transition—valid data arrives at output stage t_{DOF} after OR is HIGH. FIGURE 5. Modes of Operation Mode 5

FIFO Expansion

Word Width Expansion

Word width can be increased by connecting the corresponding input control signals of multiple devices. Flags can be monitored to obtain a composite signal by ANDing the corresponding flags.



Note: AND the corresponding flags to obtain a composite signal.

FIGURE 6. Word Width Expansion—64 x 18 FIFO

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required. please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (VCC) -0.5V to +7.0VDC Input Diode Current (IIK) $V_1 = -0.5V$ -20 mA $V_I = V_{CC} + 0.5V$ +20 mA

DC Input Voltage (V_I) DC Output Diode Current (IOK)

 $V_0 = -0.5V$ -20 mA $V_O = V_{CC} + 0.5V$ +20 mA DC Output Voltage (VO) -0.5V to $V_{CC} + 0.5V$

-0.5V to $V_{CC} + 0.5V$

+32 mA

DC Output Source or Sink Current (Io)

DC Vcc or Ground Current per Output Pin (ICC or IGND) ±32 mA Storage Temperature (TSTG) -65°C to +150°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC}) 'AC 2.0V to 6.0V 'ACT 4.5V to 5.5V Input Voltage (V_I) OV to Vcc Output Voltage (Vo) OV to Vcc Operating Temperature (T_A) 74AC/ACT -40°C to +85°C 54AC/ACT -55°C to +125°C Junction Temperature (T_{.1}) CDIP 175°C PDIP 140°C Input Rise and Fall Time (tr, tf)

(Note 2) (Typical) (Except Schmitt Inputs)

V_{IN} from 0.8V to 2.0V, V_{meas} from 0.8V to 2.0V

V_{CC} @ 4.5V 10 ns/V Vcc. @ 5.5V 8 ns/V Note 2: See individual datasheets for those devices which differ from the

typical input rise and fall times noted here.

DC Characteristics for 'AC Family Device

| | 0.3 | (8 + 6) | 74 | AC | 54AC | 74AC | | | |
|-----------------|--------------------------------------|---------------------|-------------------------|----------------------|-------------------------------------|-----------------------------------|----------|---|--|
| Symbol | Parameter | V _{CC} (V) | T _A = | 25°C | T _A = -55°C to +125°C | T _A = -40° to +85°C | Units | Conditions | |
| Vr.0 | on Vac | 0.8 | Тур | 2 | Guaranteed Li | eed Limits | | | |
| V _{IH} | Minimum High Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | 2.1 3.15 3.85 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| V _{IL} | Maximum Low Level Input Voltage | 3.0 4.5 5.5 | 1.5 2.25 2.75 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | 0.9 1.35 1.65 | ٧ | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| Voн | Minimum High Level Output Voltage | 3.0 4.5 5.5 | 2.99 4.49 5.49 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | 2.9 4.4 5.4 | ٧ | $I_{OUT} = -50 \mu\text{A}$ | |
| Am 8 Am 8 | 30) V | 3.0 4.5 5.5 | 0. | 2.56 3.86 4.86 | 2.4 3.7 4.7 | 2.46 3.76 4.76 | V | $V_{IN} = V_{IL} \text{ or } V_{IH} - 12 \text{ m/s}$ $V_{IOH} - 24 \text{ m/s}$ $V_{IOH} - 24 \text{ m/s}$ | |
| V _{OL} | Maximum Low Level Output Voltage | 3.0 4.5 5.5 | 0.002 0.001 0.001 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | V | $I_{OUT} = 50 \mu A$ | |
| V88.5 | V = V Am | 3.0 4.5 5.5 | | 0.36 0.36 0.36 | 0.50 0.50 0.50 | 0.44 0.44 0.44 | V | $^*V_{IN} = V_{IL} \text{ or } V_{IH}$ 12 mA $^I_{OL}$ 24 mA 24 mA | |
| I _{IN} | Maximum Input Leakage Current | 5.5 | 0 | ±0.1 | ±1.0 | ±1.0 | μΑ | $V_I = V_{CC} GND$ | |
| loz | Maximum TRI-STATE Leakage Current | 5.5 | | ±0.5 | ±10.0 | ±5.0 | Sahoo Is | $V_{I}(OE) = V_{IL}, V_{IH}$ $V_{I} = V_{CC}, GND$ $V_{O} = V_{CC}, GND$ | |

DC Characteristics for 'AC Family Device (Continued) and the state of
| | | 68 | 74. | AC | 54AC | 74AC | notale a | uj jaranga sasak Papatawa kamina u |
|------------------|-------------------------------------|---------------------|-----------------------|--------|-------------------------------------|-----------------------------------|----------|---------------------------------------|
| Symbol | Parameter | V _{CC} (V) | T _A = 25°C | | T _A = -55°C to +125°C | T _A = -40° to +85°C | Units | Conditions |
| goV of VC | | 4 | Тур | Vaudat | Guaranteed L | imits | (SH) to | DC Light Diode June |
| lold | †Minimum Dynamic | 5.5 | LenatioV | Dayout | 32 | 32 | mA | V _{OLD} = 1.65V Max |
| I _{OHD} | Output Current | 5.5 | TO A C | DAKY | -32 | c1 V0-32 | mA | V _{OHD} = 3.85V Min |
| Icc | Maximum Quiescent Supply Current | 5.5 | 10AN sqmeTic | 8.0 | 160 | 80 | μА | $V_{IN} = V_{CC}$ or GND |
| ICCD | Supply Current 20 MHz Loaded | 5.5 | 125 | 150 | V8.0 ± osl | 150 | mA | f = 20 MHz (Note 4) |

^{*}All outputs loaded; thresholds on input associated with output under test.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC} . I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

Note 4: Test load 50 pF, 500Ω to ground.

DC Electrical Characteristics for 'ACT Family Devices

| | Tan bend | | 544 | ACT | 54ACT | 74ACT | | |
|--------------------------------|-------------------------------------|---------------------|------------------|--------------|-------------------------------------|--|--------------------|--|
| Symbol | Parameter | V _{CC} (V) | T _A = | 25°C | T _A = -55°C to +125°C | $T_A = -40^{\circ}$ to $+85^{\circ}$ C | Units | Conditions |
| | 518 | | Тур | 7 | Guaranteed Li | mits | | |
| V _{IH} | Minimum High Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 2.0 | 2.0 2.0 | 2.0 2.0 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ |
| VIL | Maximum Low Level Input Voltage | 4.5 5.5 | 1.5 1.5 | 0.8 | 0.8 0.8 | 0.8 | n High Lev Nade | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ |
| V _{OH} | Minimum High Level | 4.5 5.5 | 4.49 5.49 | 4.4 5.4 | 5.4 | 4.4 5.4 | V | $I_{OUT} = -50 \mu\text{A}$ |
| V1.0 | poVie V | 4.5 5.5 | 3 | 3.86 4.86 | 3.70 4.70 | 3.76 4.76 | V sold or | $\begin{tabular}{ll} *V_{IN} = V_{IL} \mbox{ or } V_{IH} \\ I_{OH} & -8 \mbox{ mA} \\ & -8 \mbox{ mA} \end{tabular}$ |
| V _{OL} | Maximum Low Level Output Voltage | 4.5 5.5 | 0.001 0.001 | 0.1 | 0.1 | 0.1 0.1 | V | $I_{OUT} = 50 \mu A$ |
| HIV TO HIV Am Sil Am Sil | HOLE V | 4.5 5.5 | | 0.32 | 0.40 85.0.40 | 0.37 0.37 | v | $^*V_{IN} = V_{IL} \text{ or } V_{IH}$ I_{OL} 8 mA 8 mA |
| I _{IN} | Maximum Input | 5.5 | | ±0.1 | +1.0 | ±1.0 | μА | $V_I = V_{CC}$, GND |
| loz | Maximum TRI-STATE Current | 5.5 | | ±0.5 | n±10.0 | ±5.0 | μΑ | $V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}, GND$ |
| ГССТ | Maximum I _{CC} /Input | 5.5 | 0.6 | 1.0 | 1.6 | 1.5 | mA | $V_I = V_{CC} - 2.1V$ |
| lold | †Maximum Dynamic | 5.5 | | 1.0 | 32 | 32 | mA | V _{OLD} = 1.65V |
| I _{OHD} | Output Current | 5.5 | 0 | 0 | -32 | -32 | mA | V _{OHD} = 3.85V |
| Icc | Maximum Quiescent Supply Current | 5.5 | 9 | 8.0 | 160 | 80 | μΑ | V _{IN} = V _{CC} or GND |
| ICCD | Supply Current 20 MHz Loaded | 5.5 | 125 | 150 | | 150 | mA | f = 20 MHz (Note 4) |

^{*}All outputs loaded; thresholds on input associated with output under test.

When $\overline{\rm MR}$ is low with SO High, I_{CC} > 1.5 mA.

Note 4: Test load 50 pF, 500Ω to ground.

[†]Maximum test duration 20 ms, one output loaded at a time.

[†]Maximum test duration 2.0 ms, one output loaded at a time.

Notes: I_{CC} limit for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Characteristics

| Symbol | ZAAC | DANE | | 74AC | DARK | 5 | 4AC | 74 | AC | | Fig. |
|-------------------------------------|--|----------------------|--------------|------------------|--------------|--------------|------------------------------|--------------|------------------------|-------|------|
| Symbol | Parameter | *V _{CC} (V) | | = + 25 L = 50 | | to - | - 55°C - 125°C = 50 pF | to + | −40°C 85°C 50 pF | Units | |
| | essa niña xe | i i | Min | Тур | Max | Min | Max | Min | Max | | |
| t _{PLH} | Propagation Delay, t _{IR} SI to IR | 3.3 5.0 | 2.5 1.5 | 8.5 5.5 | 16.5 11.5 | 4.0 | 8 8 6,0 | 2.0 1.0 | 18.5 12.5 | ns | 2-6 |
| t _{PHL} | Propagation Delay, t _{IR} SI to IR | 3.3 5.0 | 2.5 1.5 | 7.0 5.0 | 14.0 | 7.6 | 8.8 8.0 | 2.0 | 16.0 11.0 | ns | 2-6 |
| ^t PLH | Propagation Delay, t _{IHF} SI to > HF | 3.3 5.0 | 4.5 3.0 | 12.0 | 23.5 15.5 | 7.5 | s.9 5.0 | 4.5 3.0 | 27.0 18.0 | ns | 2-6 |
| t _{PHL} | Propagation Delay, t _{IF} SI to Full Condition | 3.3 5.0 | 5.0 3.5 | 11.5 | 22.0 15.0 | 4.0 | 8.8 0.8 | 5.0 3.5 | 25.0 17.0 | ns | 2-6 |
| t _{PLH} | Propagation Delay, t _{IE} SI to Not Empty | 3.3 5.0 | 4.5 3.0 | 11.5 8.0 | 23.5 15.5 | 0.A 0.6 | 6.0 (0.8 | 4.5 3.0 | 26.5 17.5 | ns | 2-6 |
| ^t PLH | Propagation Delay, t _{IOR} SI to OR | 3.3 5.0 | 4.5 3.0 | 13.5 | 30.5 20.0 | 0.67 | 8.8 0.6 | 4.5 3.0 | 34.5 23.0 | ns | 2-6 |
| t _{PLH} | Propagation Delay t _{MRIRH} | 3.3 5.0 | 3.5 2.5 | 10.5 7.5 | 21.5 14.5 | 0.81 0.81 | 8.8 0.8 | 3.5 2.0 | 23.5 16.0 | ns | 2-6 |
| t _{PHL} | Propagation Delay, t _{MRORL} | 3.3 5.0 | 7.5 6.0 | 18.5 12.0 | 35.5 23.0 | 6.5 5.0 | 3.3 5.0 | 7.5 6.0 | 41.0 26.5 | ns | 2-6 |
| t _{PHL} | Propagation Delay t _{MRO} | 3.3 5.0 | 4.0 2.5 | 9.0 6.5 | 18.0 | 2.5 | 8.0 0.8 | 4.0 2.0 | 21.5 15.0 | ns | 2-6 |
| t _{PHL} | Propagation Delay t _{MRE} | 3.3 5.0 | 8.5 7.0 | 20.0 13.5 | 39.5 26.0 | 2.0 | 8.8 0.a | 8.5 el | 44.5 29.5 | ns | 2-6 |
| t _{PHL} | Propagation Delay, t _{MRONL} | 3.3 5.0 | 3.5 2.0 | 9.5 7.0 | 19.5 14.0 | 2.5 | 6.8 | 3.5 2.0 | 21.5 15.5 | ns | 2-6 |
| tw | IR Pulse Width, t _{IP} | 3.3 5.0 | 17.0 15.0 | 37.5 22.0 | 69.0 40.5 | 2.0 | 8.8 0.8 | 17.0 at 14.5 | 79.5 48.0 | ns | 2-6 |
| tw | HF Pulse Width t _{3F} | 3.3 5.0 | 18.0 16.0 | 40.0 23.0 | 71.5 42.0 | 0.26 0.00 | 3.8 5.0 | 18.0 15.5 | 84.0 50.5 | ns | 2-0 |
| t _{PLH} | Propagation Delay, t _D SO to Data Out | 3.3 5.0 | 7.0 5.5 | 20.5 13.5 | 41.5 26.0 | 28.0 | 3.3 | 7.0 5.0 | 47.5 31.0 | ns | 2-0 |
| t _{PHL} | Propagation Delay, t _D SO to Data Out | 3.3 5.0 | 7.0 5.5 | 22.5 14.5 | 43.5 28.0 | | | 7.0 5.5 | 50.5 32.5 | ns | 2-0 |
| t _{PHL} | Propagation Delay, t _{OHF} SO to < HF | 3.3 5.0 | 4.0 2.5 | 9.0 6.5 | 17.5 12.0 | | | 4.0 2.0 | 20.5 14.0 | ns | 2-0 |
| t _{PLH} | Propagation Delay, t _{OF} SO to Not Full | 3.3 5.0 | 5.5 4.0 | 14.5 10.0 | 29.0 19.0 | | | 5.5 4.0 | 33.0 22.0 | ns | 2-0 |
| t _{PLH} , t _{PHL} | Propagation Delay, t _{OR} SO to OR | 3.3 5.0 | 3.0 2.0 | 8.5 5.5 | 17.0 12.0 | | | 3.0 1.5 | 19.5 13.0 | ns | 2-0 |

^{*}Voltage Range 3.3 is 3.3V ± 0.3V

^{*}Voltage Range 5.0 is 5.0V \pm 0.5V

AC Characteristics (Continued)

| | 7480 | OANG | | 74AC | OFSI | 54 | AC | 74 | AC | | |
|------------------|---|----------------------|--------------|---------------|--------------|--------------------|-------------------------|--|--------------------|-------|------|
| Symbol | Parameter | *V _{CC} (V) | 4.14 | \ = +28 | | to + | −55°C 125°C 50 pF | T _A = to + C _L = | 85°C | Units | Fig. |
| | eth nite | telf | Min | Тур | Max | Min | Max | Min | Max | | |
| t _{PHL} | Propagation Delay, t _{OE} SO to Empty | 3.3 5.0 | 4.0 2.5 | 10.5 7.0 | 20.5 14.0 | 85 8 87 0 | 18 10 | 3.5 2.0 | 23.5 16.0 | ns | 2-6 |
| t _{PLH} | Propagation Delay, t _{OD5} SI to New Data Out | 3.3 5.0 | 7.5 6.0 | 22.5 15.5 | 44.5 30.0 | 8.9 8 6.1 0 | 3. | 7.0 5.5 | 53.5 35.0 | ns | 2-6 |
| t _{PHL} | Propagation Delay, t _{OD5} SI to New Data Out | 3.3 5.0 | 7.5 6.0 | 21.5 14.5 | 42.0 28.5 | 8 8 8 0 6 6 | | 7.0 5.5 | 48.5 33.0 | ns | 2-6 |
| t _{PLH} | Propagation Delay, t _{X1} SI to HF | 3.3 5.0 | 4.0 2.5 | 11.5 8.0 | 23.0 15.5 | 0.3 1 8 0.5 0 | | 3.5 2.0 | 26.0 17.5 | ns | 2-6 |
| t _{PLH} | Fall-Thourgh Time, t _{FTO} | 3.3 5.0 | 4.0 3.0 | 15.5 10.5 | 30.5 20.0 | 8.4 8 0.6 0 | .£ | 4.0 2.5 | 34.5 23.0 | ns | 2-5 |
| tw | OR Pulse Width, t _{OP} | 3.3 5.0 | 13.0 10.0 | 23.5 13.5 | 42.0 25.5 | 3 4.5 0 3.0 | .c | 12.0 9.0 | 48.5 29.5 | ns | 2-6 |
| tw | HF Pulse Width, t _{x3} | 3.3 5.0 | 15.0 12.0 | 27.0 16.0 | 49.5 30.0 | 3,5 3,5 0 | 8 | 14.0 11.0 | 57.0 34.5 | ns | 2-6 |
| t _{PLH} | Fall-Through Time, t _{FT} SO to IR | 3.3 5.0 | 6.5 5.0 | 19.0 12.5 | 37.0 24.0 | 8.7 E | S LEC | 6.0 4.5 | 42.5 27.5 | ns | 2-5 |
| t _{PZL} | Output Enable OE to On | 3.3 5.0 | 2.5 1.5 | 7.0 5.0 | 14.0 10.0 | 6 5 C | 8 18 | 2.0 1.0 | 16.0 11.0 | ns | 2-8 |
| t _{PLZ} | Output Disable OE to On | 3.3 5.0 | 2.0 1.0 | 4.5 3.5 | 9.0 7.0 | 8 8.5 0 7.6 | .8 .3 | 1.5 1.0 | 9.5 7.5 | ns | 2-8 |
| ^t PZH | Output Enable OE to On | 3.3 5.0 | 2.5 1.5 | 7.5 5.5 | 16.5 11.5 | 8.8 8 0 8 0 | .6. July .2. | 2.0 1.0 | 18.5 13.0 | ns | 2-7 |
| t _{PHZ} | Output Disable OE to On | 3.3 5.0 | 2.0 | 6.5 5.0 | 13.0 10.0 | 0 150 | 3, | 1.5 | 13.5 11.0 | ns | 2- |
| f _{SI} | Maximum SI Clock Frequency | 3.3 5.0 | 35.0 60.0 | 8.1% 0.88 | 0.0A 0.63 | 0.87 8 uar 0 | 8 | 30.0 50.0 | Pulse Wil | MHz | 2-3 |
| fso | Maximum SO Clock Frequency | 3.3 5.0 | 25.0 45.0 | 8.11A 0.88 | 20.5 | 0 7 0 | 3 | 20.0 35.0 | pagation Sala C | MHz | 2- |

^{*}Voltage Range 3.3 is 3.3V ± 0.3V

^{*}Voltage Range 5.0 is 5.0V \pm 0.5V

AC Characteristics (Continued)

| | ZAACT | TOANS | | 74ACT | | 5 | 4ACT | 74 | ACT | | |
|-------------------------------------|--|----------------------|------|--|------|------|-------------------------------|--|------|-------|------|
| Symbol | Parameter | *V _{CC} (V) | | T _A = +25°C C _L = 50 pF | | | = -55°C + 125°C = 50 pF | $T_A = -40^{\circ}C$ $to +85^{\circ}C$ $C_L = 50 pF$ | | Units | Fig. |
| | xsM nilit xs | A 1 | Min | Тур | Max | Min | Max | Min | Max | | |
| t _{PLH} | Propagation Delay, t _{IR} SI to IR | 5.0 | 2.0 | 6.5 | 11.0 | 3.8 | 0.3 | 1.5 | 12.5 | ns | 2-6 |
| t _{PHL} | Propagation Delay, t _{IR} SI to IR | 5.0 | 2.0 | 6.5 | 11.0 | 7.0 | 0.8 | 1.5 | 12.0 | ns | 2-6 |
| t _{PLH} | Propagation Delay, t _{IHF} SI to > HF | 5.0 | 4.0 | 10.5 | 17.0 | 0.8 | 0.8 | 4.0 | 19.5 | ns | 2-6 |
| t _{PHL} | Propagation Delay, t _{IF} SI to Full Condition | 5.0 | 4.5 | 10.5 | 16.5 | 3.8 | 0.8 | 4.5 | 19.5 | ns | 2-6 |
| ^t PLH | Propagation Delay, t _{IE} SI to Not Empty | 5.0 | 4.0 | 10.0 | 15.5 | a.s | 5.0 | 4.0 | 17.5 | ns | 2-6 |
| tpLH 8 | Propagation Delay, t _{IOR} | 5.0 | 4.0 | 13.5 | 16.5 | 3.Sr | 5.0 | 4.0 | 19.0 | ns | 2-6 |
| ^t PLH | Propagation Delay t _{MRIRH} | 5.0 | 3.0 | 8.5 | 13.5 | 0.0 | 0.6 | 3.0 | 15.5 | ns | 2-6 |
| t _{PHL} | Propagation Delay, t _{MRORL} | 5.0 | 7.0 | 16.5 | 25.5 | 0.8 | 5,0 | 7.0 | 29.0 | ns | 2-6 |
| tPHL 8-8 | Propagation Delay, t _{MRO} | 5.0 | 3.5 | 9.0 | 14.0 | ä.i | 0.8 | 3.5 | 16.0 | ns | 2-6 |
| t _{PHL} | Propagation Delay, t _{MRE} | 5.0 | 8.0 | 17.5 | 27.5 | 0.5 | 0 ê | 8.0 | 30.5 | ns | 2-6 |
| ^t PHL | Propagation Delay, t _{MRONL} | 5.0 | 3.0 | 9.0 | 15.0 | a. | 0.3 | 3.0 | 17.0 | ns | 2-6 |
| tw | IR Pulse Width, t _{IP} | 5.0 | 16.5 | 28.0 | 43.0 | | | 16.5 | 51.5 | ns | 2-6 |
| t _W | HF Pulse Width, t _{3F} | 5.0 | 17.5 | 30.0 | 46.5 | 55 | 0.8 | 17.5 | 56.0 | ns | 2-6 |
| ^t PLH | Propagation Delay, t _D SO to Data Out | 5.0 | 6.5 | 18.5 | 27.0 | 88 | 5.0 | 6.5 | 31.0 | ns | 2-6 |
| t _{PHL} | Propagation Delay, t _D SO to Data Out | 5.0 | 6.5 | 18.5 | 29.5 | | | 6.5 | 34.5 | ns | 2-6 |
| ^t PHL | Propagation Delay, t _{OHF} SO to < HF | 5.0 | 3.5 | 8.5 | 13.5 | | | 3.5 | 15.5 | ns | 2-6 |
| t _{PLH} | Propagation Delay, t _{OF} SO to Not Full | 5.0 | 5.0 | 12.5 | 19.5 | | | 5.0 | 22.0 | ns | 2-6 |
| t _{PLH} , t _{PHL} | Propagation Delay, t _{OR} | 5.0 | 2.5 | 7.0 | 11.5 | | | 2.5 | 13.5 | ns | 2-6 |

^{*}Voltage Range 5.0 is 5.0V ± 0.5V

AC Characteristics (Continued)

| | TOACT | 7044 | | 74ACT | TOAKT | 544 | ACT | 74/ | ACT | | |
|------------------|---|----------------------|------|---------|-------|-----------|-------------------------|---|---------------------------|-------|------|
| Symbol | Parameter | *V _{CC} (V) | | \ = +28 | | to + | −55°C 125°C 50 pF | $T_A = -40^{\circ}C$ to +85°C $C_L = 50 \text{ pF}$ | | Units | Fig. |
| | xelf eW | ushi. | Min | Тур | Max | Min | Max | Min | Max | | |
| t _{PHL} | Propagation Delay, t _{OE} SO to Empty | 5.0 | 3.5 | 9.5 | 15.5 | 0.2 | 3 | 3.0 | 17.5 | ns | 2-6 |
| t _{PLH} | Propagation Delay, t _{OD5} SI to New Data Out | 5.0 | 7.0 | 19.0 | 30.5 | 0.5 | 2 | 6.0 | 35.5 | ns | 2-6 |
| t _{PHL} | Propagation Delay, t _{OD5} SI to New Data Out | 5.0 | 7.0 | 19.0 | 29.5 | 0.4 | | 6.0 | 34.5 | ns | 2-6 |
| t _{PLH} | Propagation Delay, t _{X1} SI to HF | 5.0 | 3.5 | 10.0 | 16.0 | a.a c | | 2.5 | 18.0 | ns | 2-6 |
| t _{PLH} | Fall-Through Time, t _{FTO} SI to OR | 5.0 | 3.5 | 13.5 | 21.0 | 0.1. | .3 | 1.5 | 24.0 | ns | 2-5 |
| t _W | OR Pulse Width, t _{OP} | 5.0 | 12.5 | 17.0 | 26.0 | | | 12.5 | 30.5 | ns | 2-6 |
| t _W | HF Pulse Width, t _{X3} | 5.0 | 14.5 | 20.5 | 30.5 | | | 14.5 | 36.5 | ns | 2-6 |
| t _{PLH} | Fall-Through Times, t _{FT} SO to IR | 5.0 | 6.0 | 15.0 | 23.5 | 0.8 | | 2.5 | 28.0 | ns | 2-5 |
| t _{PZL} | Output Enable OE to On | 5.0 | 2.0 | 6.5 | 11.0 | 0.7 7.0 | 3 1 18Y | 1.5 | 12.0 | ns | 2-8 |
| t _{PLZ} | Output Disable OE to On | 5.0 | 1.5 | 5.0 | 8.5 | 3.6 | a C | 1.5 | 9.5 | ns | 2-8 |
| t _{PZH} | Output Enable OE to On | 5.0 | 2.0 | 7.0 | 12.0 | 0.8 | | 1.5 | 13.0 | ns | 2-7 |
| t _{PHZ} | Output Disable OE to On | 5.0 | 1.5 | 7.0 | 12.0 | 0.8 | E JANC | 1.5 | 13.0 | ns | 2-7 |
| f _{SI} | Maximum SI Clock Frequency | 5.0 | 55 | 85 | 0.85 | | 3 | 45 | Pulse Wid Pulse Wid | MHz | 2-3 |
| f _{SO} | Maximum SO Clock Frequency | 5.0 | 42 | 60 | 18.5 | 3.3 0 | .3 | 35 | l nortagaga O stači oz | MHz | 2-3 |

^{*}Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

| | | | 74 | AC | 54AC | 74AC | | 100 |
|--------------------|---|-------------------------|-----------------------------------|--------------|---|--|-------|-------------|
| Symbol | Parameter | *V _{CC} (V) | T _A = C _L = | | $T_A = -55^{\circ}C$ to $+125^{\circ}C$ $C_L = 50 \text{ pF}$ | $T_A = -40^{\circ}C$ to $+85^{\circ}C$ $C_L = 50 \text{ pF}$ | Units | Fig. No. |
| | | | Тур | 163 | Guaranteed Mir | imum | 3 000 | |
| t _W (H) | SI Pulse Width, t _{SIH} | 3.3 5.0 | 9.0 5.5 | 16.5 10.5 | | 20.5 12.5 | ns | 2-6 |
| t _W (L) | SI Pulse Width, t _{SIL} | 3.3 5.0 | 8.5 6.5 | 16.0 12.0 | e tip-hops. The or nd the Taguency | 19.5 14.5 | ns | 2-6 |
| ts | Setup Time, HIGH or LO(W, D _n to SI | 3.3 5.0 | -2.0 -1.5 | 1.0 1.0 | ng one. The state a going edge of the d agree-hips | 1.0 1.0 | ns | 2-9 |
| t _H | Hold Time, HIGH or LOW, D _n to SI | 3.3 | 1.0 1.0 | 5.5 4.0 | occur nimulizmenus retors, decados ou | 6.0 4.5 | ns | 2-9 |
| t _W | MR Pulse Width, t _{MRW} | 3.3 5.0 | 13.0 8.5 | 26.0 16.0 | ever vall bla. sea Inglises amos tot A | 30.5 20.0 | ns | 2-6 |
| t _{rec} | Recovery Time, t _{MRSIH} | 3.3 5.0 | 4.5 3.0 | 8.0 6.0 | | 9.5 7.0 | ns | 2-9 |
| t _W (H) | SO Pulse Width, t _{SOH} | 3.3 5.0 | 4.0 2.5 | 7.5 5.5 | and the | 8.5 6.5 | ns | 2-6 |
| t _W (L) | SO Pulse Width, t _{SOL} | 3.3 5.0 | 10.0 6.0 | 18.0 12.0 | , 0 , 0 | 21.0 14.0 | ns | 2-6 |

^{*}Voltage Range 3.3 is 3.3V \pm 0.3V

AC Operating Requirements

| | H-m/ B | 5 -040 | 74/ | ACT | 54ACT | 74ACT | Units | Fig. |
|--------------------|--|-------------------------|------|-----------------|---|--|-------|------|
| Symbol | Parameter | *V _{CC} (V) | | + 25°C 50 pF | $T_A = -55^{\circ}C$ to $+125^{\circ}C$ $C_L = 50 pF$ | $T_A = -40^{\circ}C$ $to +85^{\circ}C$ $C_L = 50 pF$ | | |
| | | | Тур | | Guaranteed Mi | secusió | giS. | |
| t _W (H) | SI Pulse Width, t _{SIH} | 5.0 | 3.5 | 6.5 | iugn | 7.5 | ns | 2-6 |
| t _W (L) | SI Pulse Width, t _{SIL} | 5.0 | 6.0 | 10.0 | recent toteshi s | 12.0 | ns | 2-6 |
| ts | Setup Time, HIGH or LOW, D _n to SI | 5.0 | 1.0 | 3.5 | | 4.5 | ns | 2-9 |
| t _H | Hold Time, HIGH or LOW, D _n to SI | 5.0 | 1.5 | 3.5 | | 4.5 | ns | 2-9 |
| t _W | MR Pulse Width, t _{MRW} | 5.0 | 13.0 | 20.0 | | 24.5 | ns | 2-6 |
| t _{rec} | Recovery Time, t _{MRSIH} | 5.0 | 4.5 | 7.5 | | 8.5 | ns | 2-9 |
| t _W (H) | SO Pulse Width, t _{SOH} | 5.0 | 7.5 | 6.5 | | 8.0 | ns | 2-6 |
| t _W (L) | SO Pulse Width, t _{SOL} | 5.0 | 9.0 | 14.0 | | 17.0 | ns | 2-6 |

^{*}Voltage Range 5.0 is 5.0V ± 0.5V

Capacitance

| Symbol | Symbol Parameter Cin Input Capacitance | AC/ACT | Units | Conditions |
|-----------------|---|--------|-------|-----------------|
| Symbol | T di dillotto | Тур | Onito | Contactions |
| C _{IN} | Input Capacitance | 4.5 | pF | $V_{CC} = 5.0V$ |

^{*}Voltage Range 5.0 is 5.0V \pm 0.5V



ADVANCE INFORMATION

54AC/74AC4024 7-Stage Binary Ripple Counter

General Description

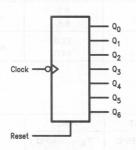
The 'AC4024 consists of 7 master-slave flip-flops. The output of each flip-flop feeds the next and the frequency at each output is half that of the preceding one. The state of the counter advances on the negative going edge of the Clock input. Reset is asynchronous and active-high.

State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and may have to be gated with the Clock of the 'AC4024 for some designs.

Features

- Outputs directly interface to CMOS, NMOS, and TTL
- Operating voltage range: 2V to 6V
- Low input current: 1 μA
- High noise immunity characteristic of CMOS devices
- Pin and functional compatible to MC1424
- Outputs source/sink 24 mA

Logic Symbol

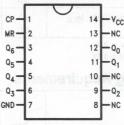


TL/F/10145-1

| Pin Names | Description |
|--------------------------------|---------------------------|
| CP | Clock Pulse Input |
| MR | Asynchronous Master Reset |
| Q ₀ -Q ₆ | Flip-Flop Outputs |

Connection Diagram

Pin Assignment for DIP, Flatpack and SOIC



TL/F/10145-2

NC = No Connection



stretoni il nottosi

Ordering Information and Physical Demansions Bookshalf Dainbulors

Section 5
Ordering Information/
Physical Dimensions



Section 5 Contents

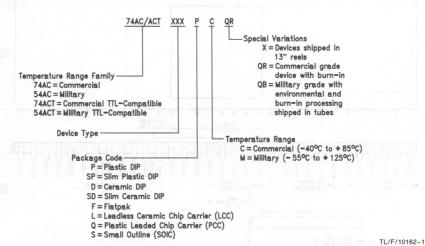
| Ordering Information and Physical Dimensions | 5-3 |
|--|-----|
| Bookshelf | |
| Distributors | |

Section 5 Ordering Information/ Physical Dimensions



Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

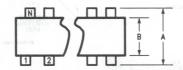


For most current packaging information, contact Product Marketing.

JEDEC-EIAJ Small Outline Package Comparison

| | Dim | 14 Pin | | 16 Pin | | 20 Pin | | 24 Pin | |
|-------|-------------|-----------------|-----------------|-----------------|-----------------|-----------------|------------------|-----------------|------------------|
| | | Min | Max | Min | Max | Min | Max | Min | Max |
| JEDEC | А | 0.228 (5.80) | 0.245 (6.20) | 0.228 (5.80) | 0.245 (6.20) | 0.393 (10.0) | 0.420 (10.65) | 0.393 (10.0) | 0.420 (10.65) |
| | B (4-0) 8 1 | 0.149 (3.80) | 0.158 (4.00) | 0.149 (3.80) | 0.158 (4.00) | 0.291 (7.40) | 0.300 (7.60) | 0.291 (7.40) | 0.300 (7.60) |
| EIAJ | А | 0.300 (7.62) | 0.350 (8.89) | 0.300 (7.62) | 0.350 (8.89) | 0.300 (7.62) | 0.350 (8.89) | 0.300 (7.62) | 0.350 (8.89) |
| | В | 0.198 (5.02) | 0.245 (6.22) | 0.198 (5.02) | 0.245 (6.22) | 0.198 (5.02) | 0.245 (6.22) | 0.198 (5.02) | 0.245 (6.22) |

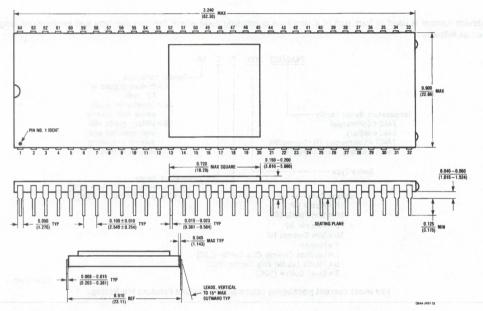
Units: Inch (mm)



TL/F/10162-2

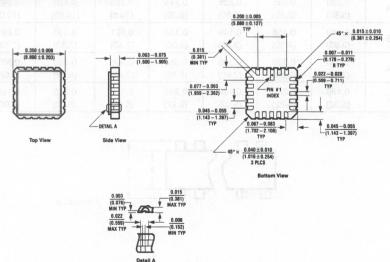


64 Lead Side Brazed Ceramic Dual-In-Line Package (D) NS Package Number D64A

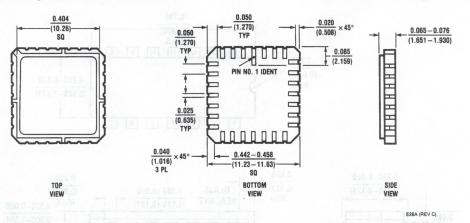


Note: FACT™ Product Shipped WITHOUT Protective Silicon "Bumpers".

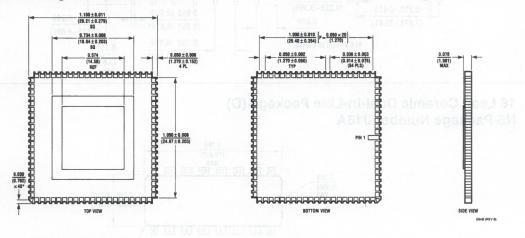
20 Terminal Ceramic Leadless Chip Carrier (L) NS Package Number E20A

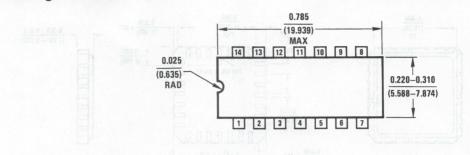


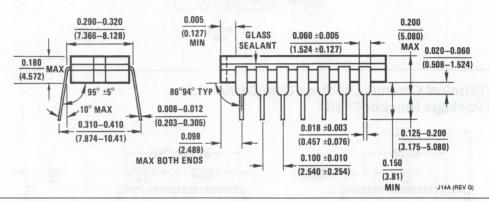
28 Terminal Ceramic Leadless Chip Carrier (L) and an include an action of the Carrier (L) and ac



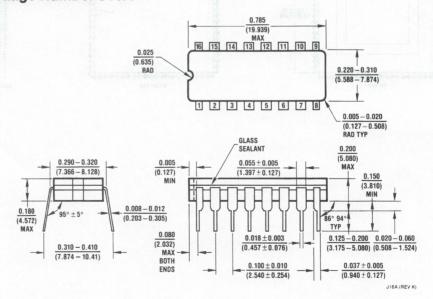
84 Terminal Ceramic Leadless Chip Carrier (L) NS Package Number E84B

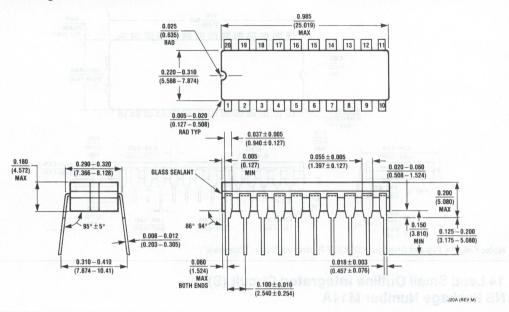




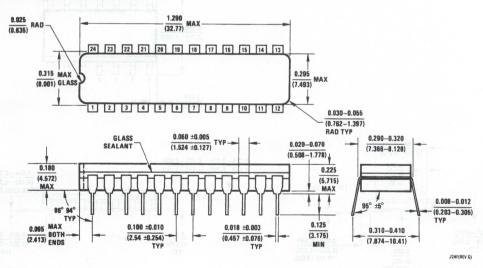


16 Lead Ceramic Dual-In-Line Package (D) NS Package Number J16A

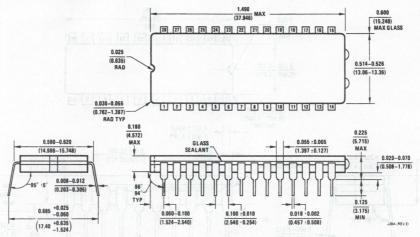




24 Lead Slim (0.300" Wide) Ceramic Dual-In-Line Package (SD) NS Package Number J24F

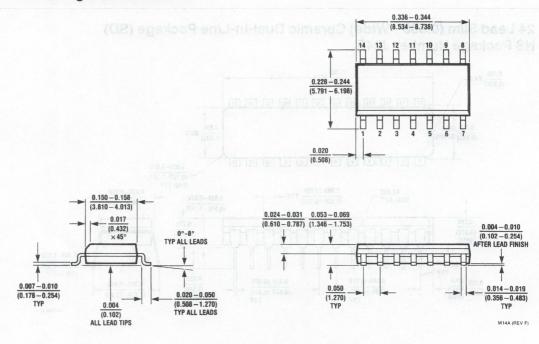


28 Lead Ceramic Dual-In-Line Package (D) Seriod Lead Colored C

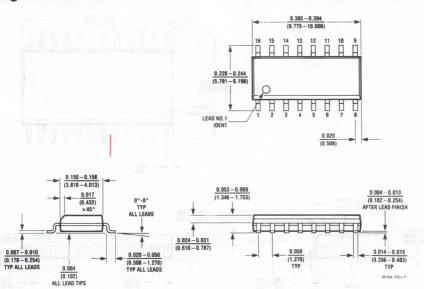


Note: FACTTM Product Shipped WITHOUT Protective Silicon "Bumpers".

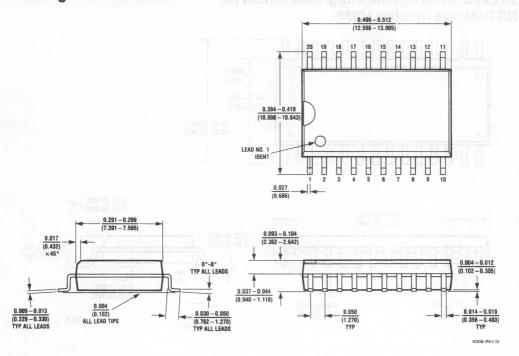
14 Lead Small Outline Integrated Circuit (S) NS Package Number M14A



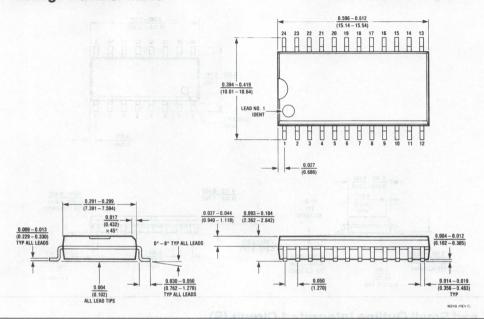
16 Lead Small Outline Integrated Circuit (S) personal entitled lisms besut as NS Package Number M16A



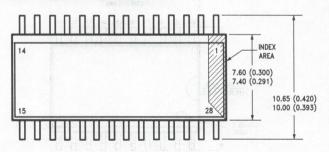
20 Lead Small Outline Integrated Circuit (S) NS Package Number M20B

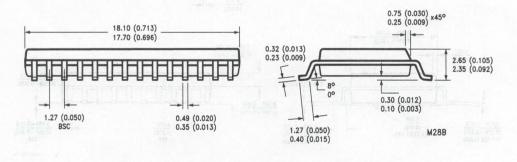


24 Lead Small Outline Integrated Circuit (S) Sergeral Scale (S) NS Package Number M24B

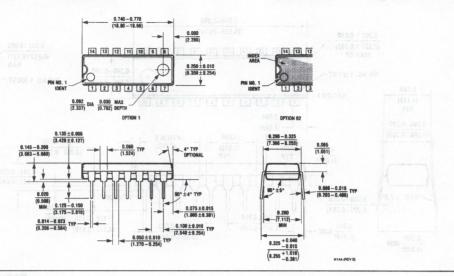


28 Lead Small Outline Integrated Circuit (S) NS Package Number M28B

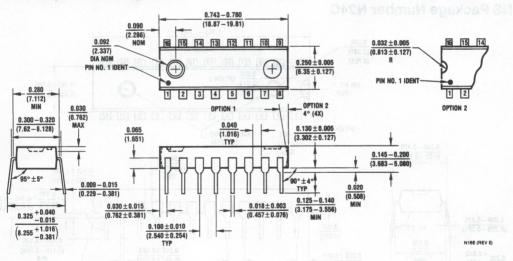




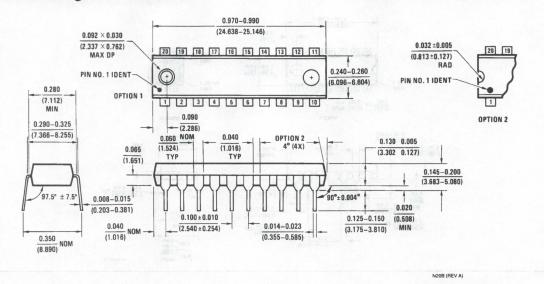
14 Lead Plastic Dual-In-Line Package (P) SNOS I and Include Date I do NS Package Number N14A GOS/A redmuk epskips I 2/A



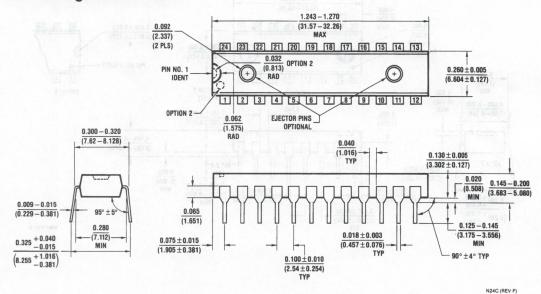
16 Lead Plastic Dual-In-Line Package (P) NS Package Number N16E



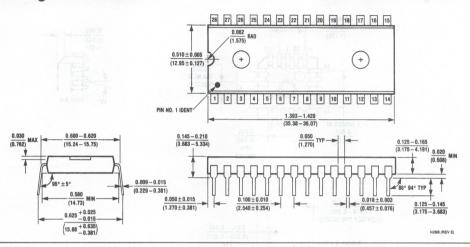
20 Lead Plastic Dual-In-Line Package (P) A STATE OF THE S



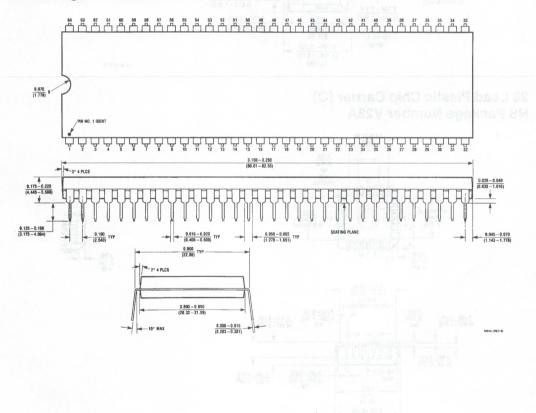
24 Lead Plastic Slim (0.300" Wide) Dual-In-Line Package (SP) NS Package Number N24C



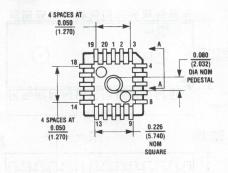
28 Lead Plastic Dual-In-Line Package (P) NS Package Number N28B



64 Lead Plastic Dual In-Line Package (P) NS Package Number N64A

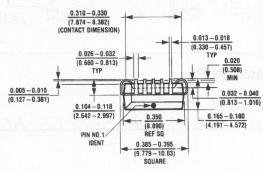


20 Lead Plastic Chip Carrier (Q) NS Package Number V20A

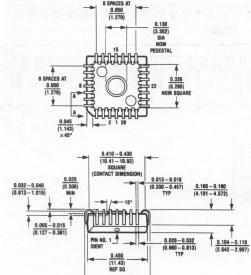




V20A (REV J)



28 Lead Plastic Chip Carrier (Q) NS Package Number V28A

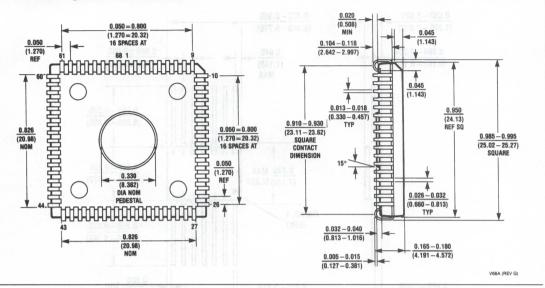


0.485 - 0.495 (12.32 - 12.57) SQUARE

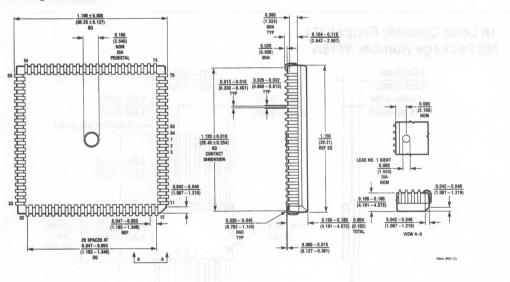


V28A (REV G)

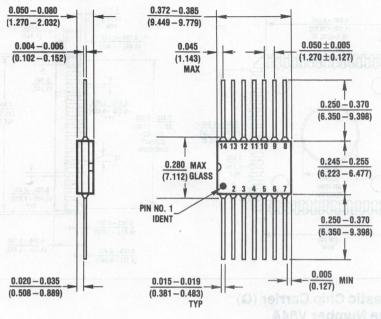
68 Lead Plastic Chip Carrier (Q) NS Package Number V68A



84 Lead Plastic Chip Carrier (Q) NS Package Number V84A

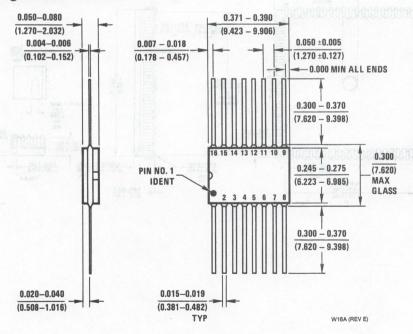


14 Lead Ceramic Flatpak (F) NS Package Number W14B

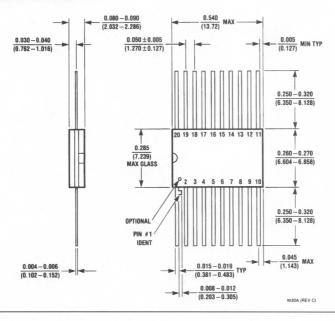


W14B (REV D)

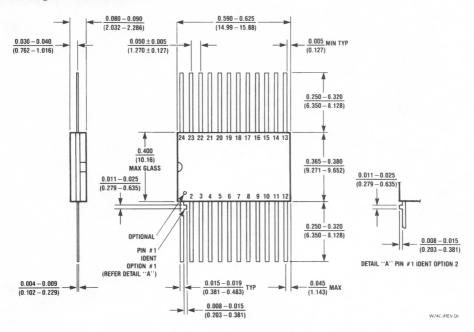
16 Lead Ceramic Flatpak (F) NS Package Number W16A



20 Lead Ceramic Flatpak (F) NS Package Number W20A

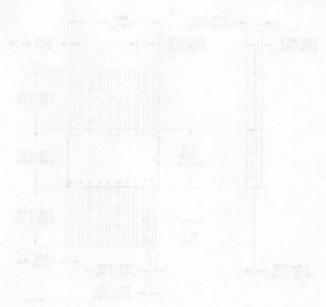


24 Lead Ceramic Flatpak (F) NS Package Number W24C

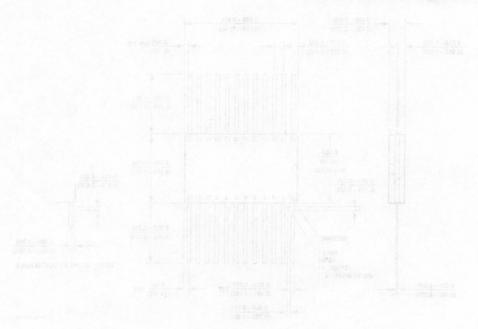


NOTES

20 Lead Caramio Fiatpak (F) NS Package Number W20A



24 Lead Caramio Flatpaik (F) NS Package Number W24C







Bookshelf of Technical Support Information

Mational Semiconductor Corporation recognizes the need to keep you informed about the availability of current technical literature.

This bookshelf is a compilation of books that are cummitly available. The listing that follows shows the publication year and section on reints for each book.

Please contact your local resional sales office for possible complignentary copies. A listi<mark>ng of sales offices f</mark>ollows this buokshell.

We are inferested in your comments on our fechalical liferature and your suggestions for improvement

Plant a send them to

Technipat Communications Best, M/S 16300 2800 Semigenductor Drive P.O. Box 65080

Santa Chara, CA 95052-8090

ALS/AS LOGIC DATABOOK-1987

Introduction to Bigolat Logic . Advanced Low Power Schottky . Advanced Schottky

ASIC DESIGN MANUAL/CATE ARRAYS & STANDARD CELLS-1987

SBIMMS) Functions * Perpresa Functions * USI/VESF unctions * Design Guidelines * Packaging

CHOS LOGIO DATABOOK-1988

CMCS AG Switching Test Circuits and Timing Waveforms • CMOS Approation Notes • MM54HC/MM74HC MM54HCT/MM74HCT • CD4XXX • MM54CX/XX/MM74CXXX • SWiace Mount

DATA COMMUNICATION/LAN/UART DATABOOK-Rev. 1-1988

LAN JECE 202.3 « Aligh Speed Seast/18M Data Communications « ISON Components » UARTS Moderns » Transmission Line Drivers/Flaceivers

DISCRIFF SERCOMBILITORS PRODUCTS DATABOOK-1988

Selection Guido and Cruss Reference Guides « Diodes » Brodler NPN Transistors

Sipolar PNP Transistors » JFET Transistors « Surface Mount Products » Pro-Stetitor Series

Consumer Sence » Power Components » Transistor Datasheets » Process Oberacteristics

SAPILLMOORGUAR THIRROLMEN HARD

Oynamic Mannory Control * Emer Detection end Connection * Microprocessor Applications for the DEP MAY MOATTY AND CASTOR * Microprocessor Applications for the TVR4274 / 21 A 1224

- 830 : ...- 910 0 M A TAR - 910 1 F F

Family Overview 9 F109K Datasheets + 176 Datasheets + 10K and 100K Memory Datasheets
Design Guide • Chout Basics + Logic Design + Transmission Lins Concepts • System Considerations
Power Distribution and Thannet Considerations • Testing Techniques • Quarity Assumnce and Refiguility

Odsenption and Family Characteristics * Ratings, Shoulipations and Wevetoms:
Design Considerations * 54AQ/74AQ/XXX * 54AQ/7774AQ/7XXXX

FAST® ADVANCED SCHOTTOLTILLOGIC DATABOOK-1988

Directi Characteristics - Hellings, Specifications and Waveforms + Design Considerations + S4F774F30X



Bookshelf of Technical Support Information

National Semiconductor Corporation recognizes the need to keep you informed about the availability of current technical literature.

This bookshelf is a compilation of books that are currently available. The listing that follows shows the publication year and section contents for each book.

Please contact your local National sales office for possible complimentary copies. A listing of sales offices follows this bookshelf.

We are interested in your comments on our technical literature and your suggestions for improvement.

Please send them to:

Technical Communications Dept. M/S 16300 2900 Semiconductor Drive P.O. Box 58090 Santa Clara, CA 95052-8090

ALS/AS LOGIC DATABOOK-1987

Introduction to Bipolar Logic • Advanced Low Power Schottky • Advanced Schottky

ASIC DESIGN MANUAL/GATE ARRAYS & STANDARD CELLS-1987

SSI/MSI Functions • Peripheral Functions • LSI/VLSI Functions • Design Guidelines • Packaging

CMOS LOGIC DATABOOK-1988

CMOS AC Switching Test Circuits and Timing Waveforms • CMOS Application Notes • MM54HC/MM74HC MM54HCT/MM74HCT • CD4XXX • MM54CXXX/MM74CXXX • Surface Mount

DATA COMMUNICATION/LAN/UART DATABOOK—Rev. 1—1988

LAN IEEE 802.3 • High Speed Serial/IBM Data Communications • ISDN Components • UARTs Modems • Transmission Line Drivers/Receivers

DISCRETE SEMICONDUCTOR PRODUCTS DATABOOK-1989

Selection Guide and Cross Reference Guides • Diodes • Bipolar NPN Transistors
Bipolar PNP Transistors • JFET Transistors • Surface Mount Products • Pro-Electron Series
Consumer Series • Power Components • Transistor Datasheets • Process Characteristics

DRAM MANAGEMENT HANDBOOK—1988

Dynamic Memory Control ● Error Detection and Correction ● Microprocessor Applications for the DP8408A/09A/17/18/19/28/29 ● Microprocessor Applications for the DP8420A/21A/22A

F100K DATABOOK—1989

Family Overview • F100K Datasheets • 11C Datasheets • 10K and 100K Memory Datasheets

Design Guide • Circuit Basics • Logic Design • Transmission Line Concepts • System Considerations

Power Distribution and Thermal Considerations • Testing Techniques • Quality Assurance and Reliability

FACTTM ADVANCED CMOS LOGIC DATABOOK—1989

Description and Family Characteristics \bullet Ratings, Specifications and Waveforms Design Considerations \bullet 54AC/74ACXXX \bullet 54ACT/74ACTXXX

FAST® ADVANCED SCHOTTKY TTL LOGIC DATABOOK—1988

Circuit Characteristics • Ratings, Specifications and Waveforms • Design Considerations • 54F/74FXXX

FAST® APPLICATIONS HANDBOOK—REPRINT

Reprint of 1987 Fairchild FAST Applications Handbook

Contains application information on the FAST family: Introduction • Multiplexers • Decoders • Encoders Operators • FIFOs • Counters • TTL Small Scale Integration • Line Driving and System Design FAST Characteristics and Testing • Packaging Characteristics • Index

GRAPHICS DATABOOK—1988

Advanced Graphics Chipset • Application Notes

INTERFACE DATABOOK—1988

Transmission Line Drivers/Receivers • Bus Transceivers • Peripheral Power Drivers • Display Drivers

Memory Support • Microprocessor Support • Level Translators and Buffers • Frequency Synthesis • Hi-Rel Interface

LINEAR APPLICATIONS HANDBOOK-1986

The purpose of this handbook is to provide a fully indexed and cross-referenced collection of linear integrated circuit applications using both monolithic and hybrid circuits from National Semiconductor.

Individual application notes are normally written to explain the operation and use of one particular device or to detail various methods of accomplishing a given function. The organization of this handbook takes advantage of this innate coherence by keeping each application note intact, arranging them in numerical order, and providing a detailed Subject Index.

LINEAR 1 DATABOOK—1988

Voltage Regulators • Operational Amplifiers • Buffers • Voltage Comparators • Instrumentation Amplifiers • Surface Mount

LINEAR 2 DATABOOK-1988

Active Filters • Analog Switches/Multiplexers • Analog-to-Digital • Digital-to-Analog • Sample and Hold Sensors • Voltage References • Surface Mount

LINEAR 3 DATABOOK-1988

Audio Circuits • Radio Circuits • Video Circuits • Motion Control • Special Functions • Surface Mount

LS/S/TTL DATABOOK—1987

Introduction to Bipolar Logic • Low Power Schottky • Schottky • TTL • Low Power

MASS STORAGE HANDBOOK-1988

Winchester Disk Preamplifiers • Winchester Disk Servo Control • Winchester Disk Pulse Detectors Winchester Disk Data Separators/Synchronizers and ENDECs • Winchester Disk Data Controller SCSI Bus Interface Circuits • Floppy Disk Controllers

MEMORY DATABOOK—1988

PROMs, EPROMs • Flash EPROMs and EEPROMs • TTL I/O SRAMs ECL I/O SRAMs • ECL I/O Memory Modules

MICROCONTROLLER DATABOOK—1988

COP400 Family • COP800 Family • COPS Applications • HPC Family • HPC Applications
MICROWIRE and MICROWIRE/PLUS Peripherals • Display/Terminal Management Processor (TMP)
Microcontroller Development Tools

PROGRAMMABLE LOGIC DATABOOK & DESIGN MANUAL—1989

Product Line Overview • Datasheets • Designing with PLDs • PLD Design Methodology • PLD Design Development Tools Fabrication of Programmable Logic • Application Examples

REAL TIME CLOCK HANDBOOK—1989

Real Time Clocks and Timer Clock Peripherals . Application Notes

RELIABILITY HANDBOOK—1986

Reliability and the Die • Internal Construction • Finished Package • MIL-STD-883 • MIL-M-38510

The Specification Development Process • Reliability and the Hybrid Device • VLSI/VHSIC Devices

Radiation Environment • Electrostatic Discharge • Discrete Device • Standardization

Quality Assurance and Reliability Engineering • Reliability and Documentation • Commercial Grade Device

European Reliability Programs • Reliability and the Cost of Semiconductor Ownership

Reliability Testing at National Semiconductor • The Total Military/Aerospace Standardization Program

883B/RETSTM Products • MILS/RETSTM Products • 883/RETSTM Hybrids • MIL-M-38510 Class B Products

Radiation Hardened Technology • Wafer Fabrication • Semiconductor Assembly and Packaging

Semiconductor Packages • Glossary of Terms • Key Government Agencies • AN/ Numbers and Acronyms

Bibliography • MIL-M-38510 and DESC Drawing Cross Listing

SERIES 32000 MICROPROCESSORS DATABOOK—1988

Series 32000 Overview • Central Processing Units • Slave Processors • Peripherals • Board Level Products
Development Systems and Tools • Software Support • Application Notes • NSC800 Family

TELECOMMUNICATIONS—1987

Line Card Components • Integrated Services Digital Network Components • Modems
Analog Telephone Components • Application Notes

NATIONAL SEMICONDUCTOR CORPORATION DISTRIBUTORS

ALABAMA

Huntsville Arrow Electronics (205) 837-6955 **Bell Industries** (205) 837-1074

> Hamilton/Aynet (205) 837-7210 Pioneer Technology

(205) 837-9300

ARIZONA

Chandler Hamilton/Avnet

(602) 231-5100 Phoenix

Arrow Electronics (602) 437-0750

Tempe Anthem Electronics

(602) 966-6600 Rell Industries (602) 966-7800

CALIFORNIA

Agora Hills Zeus Components (818) 889-3838

Anaheim Time Electronics

(714) 934-0911

Chatsworth Anthem Electronics (818) 700-1000

Arrow Electronics (818) 701-7500 Hamilton Electro Sales

(818) 700-6500 Time Electronics

(818) 998-7200 Costa Mesa

Avnet Electronics (714) 754-6050 Hamilton Electro Sales

(714) 641-4159 Garden Grove

Bell Industries (714) 895-7801

Gardena **Bell Industries** (213) 515-1800 Hamilton Electro Sales

(213) 217-6751 Anthem Electronics

(714) 768-4444 Ontario

Hamilton/Avnet (714) 989-4602 Rocklin

Anthem Electronics (916) 922-6800 **Bell Industries**

(916) 969-3100 Sacramento Hamilton/Avnet (916) 925-2216

San Diego Anthem Electronics (619) 453-9005 Arrow Electronics

(619) 565-4800 Hamilton/Avnet (619) 571-7510 Time Electronics

(619) 586-1331 San Jose Anthem Electronics

(408) 453-1200 Pioneer Technology (408) 954-9100 Zeus Components (408) 998-5121

Sunnvvale

Arrow Electronics (408) 745-6600 **Rell Industries** (408) 734-8570 Hamilton/Aynet

(408) 743-3355 Time Electronics (408) 734-9888

Thousand Oaks **Bell Industries** (805) 499-6821 Torrance

Time Electronics (213) 320-0880 Tustin

Arrow Electronics (714) 838-5422 Yorba Linda Zeus Components (714) 921-9000

COLORADO

Englewood Anthem Electronics (303) 790-4500

Arrow Electronics (303) 790-4444 Hamilton/Avnet (303) 799-9998

Wheatridge **Bell Industries** (303) 424-1985

CONNECTICUT

Cheshire Time Electronics (203) 271-3200

Danbury Hamilton/Avnet (203) 797-2800

Meriden Anthem Electronics (203) 237-2282 Norwalk

Pioneer Standard (203) 853-1515 Wallingford

Arrow Electronics (203) 265-7741

FLORIDA

Altamonte Springs Pioneer Technology (407) 834-9090

Clearwater Pioneer Technology (813) 536-0445

Deerfield Beach Arrow Electronics (305) 429-8200 **Bell Industries** (305) 421-1997 Pioneer Technology

(305) 428-8877 Fort Lauderdale Hamilton/Avnet (305) 971-2900

Lake Mary Arrow Electronics (407) 323-9300

Largo Bell Industries (813) 541-4434 Oviedo

Zeus Components (407) 365-3000 St. Petersburg Hamilton/Avnet

(813) 576-3930 Winter Park Hamilton/Avnet (407) 628-3888

GEORGIA

Norcross

Arrow Electronics (404) 449-8252 Rell Industries (404) 662-0923 Hamilton/Avnet (404) 447-7500 Pioneer Technology (404) 448-1711

II I INOIS

Addison Pioneer Standard (312) 437-9680 Rensenville Hamilton/Avnet (312) 860-7780 Elk Grove Village Anthem Electronics (312) 640-6066 **Bell Industries** (312) 640-1910

Itasca Arrow Electronics (312) 250-0500

Urbana **Bell Industries** (217) 328-1077

Wooddale Time Electronics (312) 350-0610

INDIANA Carmel

Hamilton/Aynet (317) 844-9333 Fort Wayne **Bell Industries** (219) 423-3422 Indianapolis Advent Electronics Inc. (317) 872-4910 Arrow Flectronics (317) 243-9353 **Bell Industries** (317) 875-8200

(317) 849-7300 IOWA

Cedar Rapids Advent Electronics (319) 363-0221 Arrow Electronics (319) 395-7230 **Bell Industries** (319) 395-0730 Hamilton/Avnet (319) 362-4757

Pioneer Standard

KANSAS

Leneva Arrow Electronics (913) 541-9542 Overland Park Hamilton/Avnet (913) 888-8900

MARYLAND

Columbia Anthem Electronics (301) 995-6640 Arrow Electronics (301) 995-6002 Hamilton/Avnet (301) 995-3500 Time Electronics (301) 964-3090 Zeus Components (301) 997-1118 Gaithersburg Pioneer Technology

(301) 921-0660

MASSACHUSETTS

Lexington Pioneer Standard (617) 861-9200 Zeus Components (617) 863-8800 Norwood Gerber Electronics

(617) 769-6000 Peabody Hamilton/Avnet (617) 531-7430 Time Electronics (617) 532-6200

Wilmington Anthem Electronics (617) 657-5170 Arrow Electronics (617) 935-5134

MICHIGAN

Ann Arbor Arrow Electronics (313) 971-8220

Bell Industries (313) 971-9093 **Grand Rapids** Arrow Electronics (616) 243-0912

Hamilton/Avnet (616) 243-8805 Pioneer Standard (616) 698-1800

Livonia Hamilton/Avnet (313) 522-4700 Pioneer Standard (313) 525-1800

Wyoming R. M. Electronics, Inc. (616) 531-9300

MINNESOTA

Eden Prairie Anthem Electronics (612) 944-5454 Pioneer Standard (612) 944-3355

Edina Arrow Electronics (612) 830-1800 Minnetonka Hamilton/Avnet (612) 932-0600

MISSOURI

Earth City Hamilton/Aynet (314) 344-1200 St. Louis Arrow Electronics (314) 567-6888 Time Electronics (314) 391-6444

NEW HAMPSHIRE

Hudson Bell Industries (603) 882-1133 Manchester Arrow Electronics (603) 668-6968 Hamilton/Avnet (603) 624-9400

NATIONAL SEMICONDUCTOR CORPORATION DISTRIBUTORS (Continued)

Cherry Hill

Hamilton/Avnet (609) 424-0100

Fairfield Anthem Electronics (201) 227-7960

Hamilton/Avnet (201) 575-3390 Marlton

Arrow Electronics (609) 596-8000 Parsippany

Arrow Electronics (201) 538-0900 Pine Brook

Nu Horizons Electronics (201) 882-8300 Pioneer Standard (201) 575-3510

Time Electronics (201) 882-4611

NEW MEXICO

Albuquerque Alliance Electronics Inc. (505) 292-3360 Arrow Electronics (505) 243-4566 Bell Industries (505) 292-2700 Hamilton/Avnet (505) 765-1500

NEW YORK

Amityville Nu Horizons Electronics (516) 226-6000 Binghamton Pioneer (607) 722-9300 Buffalo Summit Electronics (716) 887-2800

Fairport Pioneer Standard (716) 381-7070 Time Electronics (716) 383-8853

Hauppauge Anthem Electronics (516) 273-1660 Arrow Electronics (516) 231-1000 Hamilton/Avnet

(516) 434-7413 Time Electronics (516) 273-0100

Port Chester Zeus Components (914) 937-7400

Rochester Arrow Electronics (716) 427-0300 Hamilton/Avnet (716) 475-9130

Summit Electronics (716) 334-8110 Ronkonkoma

Zeus Components (516) 737-4500 Syracuse

Hamilton/Avnet (315) 437-2641 Time Electronics

(315) 432-0355 Westbury Hamilton/Aynet (516) 997-6868

Woodbury Pioneer Electronics (516) 921-8700

NORTH CAROLINA

Charlotte Pioneer Technology (704) 527-8188 Time Electronics (704) 522-7600

Durham Pioneer Technology (919) 544-5400 Raleigh

Arrow Electronics (919) 876-3132 Hamilton/Avnet (919) 878-0810

Winston-Salem Arrow Electronics (919) 725-8711

OHIO

Centerville Arrow Electronics (513) 435-5563 Cleveland

Pioneer (216) 587-3600 Dayton Bell Industries (513) 435-8660 Bell Industries-Military (513) 434-8231

Hamilton/Avnet (513) 439-6700 Pioneer Standard (513) 236-9900 Zeus Components (914) 937-7400

Solon Arrow Electronics (216) 248-3990 Hamilton/Avnet

(216) 831-3500 Westerville Hamilton/Avnet (614) 882-7004

OKLAHOMA

Tulsa Arrow Electronics (918) 252-7537 Hamilton/Avnet (918) 252-7297 Radio Inc. (918) 587-9123

OREGON

Beaverton Almac-Stroum Electronics (503) 629-8090 Anthem Electronics (503) 643-1114

Arrow Electronics (503) 645-6456 Hamilton/Avnet (503) 627-0201

Lake Oswego Bell Industries (503) 241-4115

PENNSYLVANIA

Horsham Anthem Electronics (215) 443-5150 Pioneer Technology (215) 674-4000 King of Prussia Time Electronics (215) 337-0900 Monroeville

Arrow Electronics

(412) 856-7000

Pittsburgh Hamilton/Avnet (412) 281-4150 Pioneer

(412) 782-2300

TEXAS Austin

Arrow Electronics (512) 835-4180 Hamilton/Avnet (512) 837-8911 Pioneer Standard (512) 835-4000 Time Electronics

(512) 399-3051 Carrollton **Arrow Electronics** (214) 380-6464 Time Electronics (214) 241-7441

Dallas Pioneer Standard (214) 386-7300

Houston Arrow Electronics (713) 530-4700 Pioneer Standard

(713) 988-5555 Irving Hamilton/Avnet (214) 550-7755

Richardson Anthem Electronics (214) 238-7100 Zeus Components (214) 783-7010

Stafford Hamilton/Avnet (713) 240-7733

UTAH

Midvale Bell Industries (801) 972-6969 Salt Lake City Anthem Electronics (801) 973-8555

(801) 973-6913 Hamilton/Avnet (801) 972-4300 West Valley

Arrow Electronics

Time Electronics (801) 973-8181

WASHINGTON

Bellevue Almac-Stroum Electronics (206) 643-9992

Kent Arrow Electronics (206) 575-4420

Redmond Anthem Electronics (206) 881-0850 Hamilton/Avnet (206) 867-0148

WISCONSIN

Brookfield Arrow Electronics (414) 792-0150 Mequon

Taylor Electric (414) 241-4321 Waukesha Bell Industries (414) 547-8879 Hamilton/Avnet

CANADA

(414) 784-4516 WESTERN PROVINCES Burnaby

Hamilton/Avnet (604) 437-6667 Semad Electronics (604) 420-9889

Calgary Hamilton/Avnet (403) 250-9380 Semad Electronics

(403) 252-5664 Zentronics (403) 272-1021

Edmonton Zentronics (403) 468-9306

Richmond Zentronics (604) 273-5575

Saskatoon Zentronics (306) 955-2207 Winnipeg

Zentronics (204) 694-1957

EASTERN PROVINCES Brampton

Zentronics (416) 451-9600 Mississauga

Hamilton/Avnet (416) 677-7432

Nepean Hamilton/Avnet (613) 226-1700 **Zentronics**

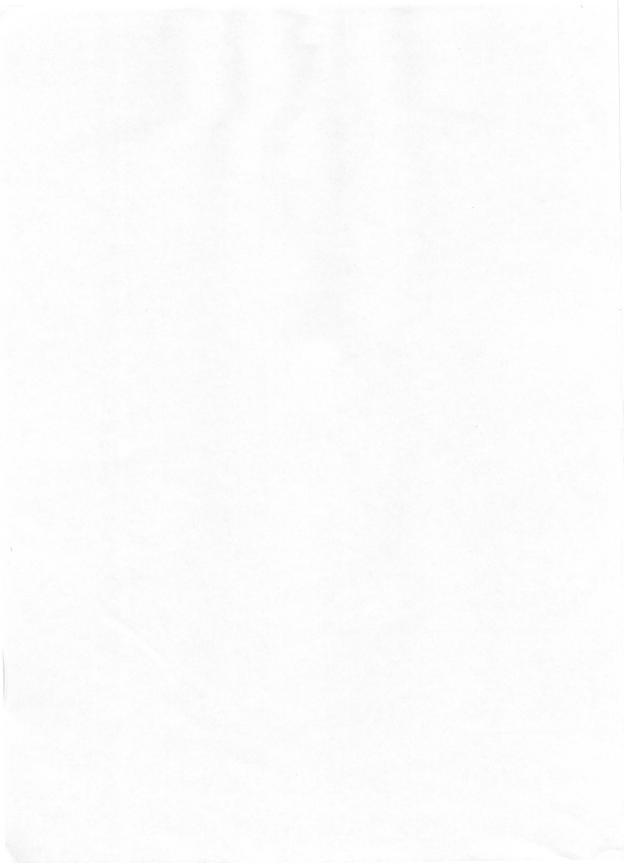
(613) 226-8840 Ottawa Semad Electronics (613) 727-8325

Pointe Claire Semad Electronics (514) 694-0860 St. Laurent

Hamilton/Avnet (514) 335-1000 Zentronics (514) 737-9700

Willowdale ElectroSonic Inc. (416) 494-1666





SALES OFFICES

AL ARAMA

Huntsville (205) 721-9367

ARIZONA

Tempe (602) 966-4563

CALIFORNIA

Inglewood

(213) 645-4226 Roseville

(916) 786-5577

San Diego

(619) 587-0666

Santa Clara (408) 562-5900

Tustin (714) 259-8880

Woodland Hills (818) 888-2602

COLORADO

Boulder

(303) 440-3400 Colorado Springs (303) 578-3319

Englewood (303) 790-8090

CONNECTICUT

Hamden (203) 288-1560 FLORIDA

Boca Raton (407) 997-8133

Orlando

(305) 629-1720

St. Petersburg (813) 577-1380

GEORGIA

Norcross (404) 441-2740

ILLINOIS

Schaumburg (312) 397-8777

INDIANA

Carmel

(317) 843-7160

Fort Wayne (219) 484-0722

IOWA

Cedar Rapids

(319) 395-0090

KANSAS

Overland Park

(913) 451-4402

MARYLAND Hanover

(301) 796-8900

MASSACHUSETTS

Burlington

(617) 273-3170

MICHIGAN

Grand Rapids

(616) 940-0588

W. Bloomfield (313) 855-0166

MINNESOTA

Bloomington

(612) 854-8200

NEW JERSEY

Paramus

(201) 599-0955

NEW MEXICO

Albuquerque

(505) 884-5601

NEW YORK

Fairport

(716) 223-7700

Liverpool

(315) 451-9091

Melville

(516) 351-1000

Wappinger Falls

(914) 298-0680

NORTH CAROLINA

Cary (919) 481-4311

ОНЮ

Dayton

(513) 435-6886

Dublin

(614) 766-3679

Independence (216) 524-5577 ONTARIO

Mississauga

(416) 678-2920

Nepean

(613) 596-0411

OREGON

Portland (503) 639-5442

PENNSYLVANIA

Horsham

(215) 672-6767

PUERTO RICO

Rio Piedias

(809) 758-9211

QUEBEC Lachine

(514) 636-8525

TEXAS

Austin

(512) 346-3990

Houston

(713) 771-3547

Richardson

(214) 234-3811

UTAH

Salt Lake City

(801) 322-4747

WASHINGTON

Bellevue (206) 453-9944

WISCONSIN

Brookfield (414) 782-1818



National Semiconductor

2900 Semiconductor Drive P.O. Box 58090 Santa Clara, CA 95052-8090 Tel: (408) 721-5000 TWX: (910) 339-9240

SALES OFFICES (Continued)

INTERNATIONAL OFFICES

Electronica NSC de Mexico SA

Juventino Rosas No. 118-2 Col Guadalupe Inn Mexico, 01020 D.F. Mexico Tel: 52-5-524-9402

National Semicondutores Do Brasil Ltda.

Av. Brig. Faria Lima, 1383 6.0 Andor-Conj. 62 01451 Sao Paulo, SP, Brasil Tel: (55/11) 212-5066 Pax: (55/11) 211-1181 NSBR BR

National Semiconductor GmbH

Industriestrasse 10 D-8080 Furstenfeldbruck West Germany Tel: (0-81-41) 103-0

National Semiconductor (UK) Ltd.

The Maple, Kembrey Park Swindon, Wiltshire SN2 6UT United Kingdom Tel: (07-93) 61-41-41 Telex: 444-674

National Semiconductor Benelux

Vorsilaan 100 B-1170 Brussels Belgium Tel: (02) 6-61-06-80 Telex: 61007

National Semiconductor (UK) Ltd.

Ringager 4A, 3 DK-2605 Brondby Denmark Tel: (02) 43-32-11 Telex: 15-179 Fax: (02) 43-31-11

National Semiconductor S.A.

Centre d'Affaires-La Boursidiere Bâtiment Champagne, B.P. 90 Route Nationale 186 F-92357 Le Plessis Robinson France Tel: (1) 40-94-88-88 Telex: 631065 Fax: (1) 40-94-88-11

National Semiconductor (UK) Ltd.

Unit 2A Clonskeagh Square Clonskeagh Road Dublin 14 Tel: (01) 69-55-89 Telex: 91047 Fax: (01) 69-55-89

National Semiconductor S.p.A.

Strada 7, Palaz 20089 Rozzano Milanofiori Italy

Tel: (02) 8242046/7/8/9

National Semiconductor (UK) Ltd.

P.O. Box 29 N-1321 Stabekk Norway Tel: (2) 12-53-70 Fax: (2) 12-53-75

National Semiconductor AB

Box 2016
Stensatravagen 13
S-12702 Skarholmen
Sweden
Tel: (08) 970190

National Semiconductor

Calle Agustin de Foxa, 27 28036 Madrid Spain Tel: (01) 733-2958 Telex: 46133

National Semiconductor Switzerland

Alte Winterthurerstrasse 53 Postfach 567 Ch-8304 Wallisellen-Zurich Switzerland Tel: (01) 830-2727 Telex: 828-444

National Semiconductor

Kauppakartanonkatu 7, A/ SF-00930 Helsinki 7 Finland Tel: (90) 33-80-33 Telex: 126116

National Semiconductor

Postbus 90 1380 AB Weesp The Netherlands Tel: (0-29-40) 3-04-48 Telex: 10-956 Fax: (0-29-40) 3-04-30

National Semiconductor Japan Ltd.

Sanseido Bldg. 5F 4-15 Nishi Shinjuku Shinjuku-ku Tokyo 160 Japan Tel: 3-299-7001 Fax: 3-299-7000

National Semiconductor Hong Kong Ltd.

Suite 513, 5th Floor, Chinachem Golden Plaza, 77 Mody Road, Tsimshatsui Eas Kowloon, Hong Kong Tel: 3-7231290 Telex: 52996 NSSEA HX Fax: 3-3112536

National Semiconductor (Australia) PTY, Ltd.

Melbourne, 3004 Victory, Australia Tel: (03) 267-5000 Fax: 61-3-2677458

National Semiconductor (PTE),

Ltd.
200 Cantonment Road 1
Southpoint
Singapore 0208
Tel: 2252226
Telex: BS 33877

National Semiconductor (Far East) Ltd.

Taiwan Branch

P.O. Box 68-332 Taipei 7th Floor, Nan Shan Life Bldg 302 Min Chuan East Road, Taipei, Taiwan R.O.C. Tel: (86) 02-501-7227 Telex: 22837 NSTW Cable: NSTW TAIPEI

National Semiconductor (Far East) Ltd.

Korea Branch

13th Floor, Dai Han Life Insurance 63 Building, 60, Yoido-dong, Youngdeungpo-kt Seoul, Korea 150-763 Tel: (02) 784-8051/3, 785-0696/8 Telex: 24942 NSPKLO Fax: (02) 784-8054